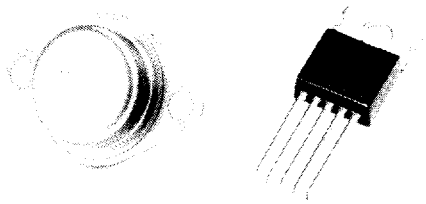
LAS-8100

3 AMP PEAK SWITCHING TRANSISTOR DRIVERS



FEATURES

- Provides simple turn-on and turn-off
- Driver for bipolar and power FETS
- CMOS, NMOS & TTL compatible
- Baker clamp output
- Under voltage lockout

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DESCRIPTION

The LAS 8100 Series switching transistor drivers are designed to drive low gain, high current, switching transistors, Darlingtons or FETs at their maximum switching speeds. This is accomplished by providing optimum turn-on (I_{B1}) and turn-off (I_{B2}) drive.

The LAS 8100 monolithic integrated circuit uses non-saturating high speed logic. The input is a Schmidt trigger with 100mV hysteresis providing noise immunity, and can accept a slow rise time. The output is jitter free. The output switching speed is virtually independent of the input switching speed. Under-voltage lockout assures proper operation during power-up and power-down. The output is designed to use the Baker Clamp for non-saturating high speed switching. The push-pull output stage is capable of sourcing and sinking up to 3 amperes.

The LAS 8100 is a single monolithic driver for switching transistors; it is packaged in a hermetically sealed 4 pin TO-3 configuration. The LAS 8101 contains two monolithic die to drive two switching devices for double ended converters and other drives. The LAS 8100P is a single monolithic driver packaged in a special TO-220 plastic package.

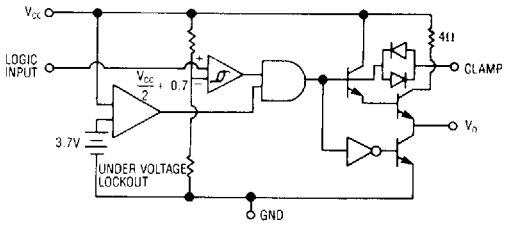
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
Supply Voltage	V_{CC}	26	Volts
Logic Input Voltage	V_{IN}	V_{CC}	Volts
Output Current Source (peak) Source (continuous) Sink (peak and continuous)	I_O	 3 1 3	Amps
Power Dissipation	P_D	15	Watts
Thermal Resistance Junction to Case LAS 8100 LAS 8101 LAS 8100P	θ_{JC}	 3 2 4	°C/Watt
Operating Junction Temperature and Storage Temperature Range LAS 8100, 8101 LAS 8100P	T_J T_{STG}	 −55 to 125 −25 to 125	°C
Lead Temperature LAS 8100, 8101 (Soldering, 60 seconds) LAS 8100P (Soldering, 10 seconds)	T_{LEAD}	 300 260	°C

DEVICE SELECTION GUIDE

DEVICE	PACKAGE	OUTPUT
LAS 8100	TO-3	SINGLE
LAS 8100P	TO-220	SINGLE
LAS 8101	TO-3	DUAL

BLOCK DIAGRAM



3 AMP PEAK SWITCHING TRANSISTOR DRIVERS

LAS-8100

ELECTRICAL CHARACTERISTICS

Test conditions are as follows: V_{CC} = 15V, I_O = 0A, T_J = 25°C

Parameter	Symbol	Test Limits			Units
		Minimum	Typical	Maximum	
Logic Input Threshold	V_T	7.8		8.6	Volts
Under Voltage Lockout		3.5		3.9	Volts
Temperature Coefficient Logic Input Threshold Under Voltage Lockout	T_C		 0.002 0.01	 0.003 0.015	V/°C
Logic Input Current		10	30	100	µA
Quiescent Current	I_Q	10	15	25	mA
Baker Clamp Source Current		3.0	4.5	7.5	mA
SWITCHING CHARACTERISTICS[1]					
Turn On Delay Time	t_d		300	500	ns
Rise Time	t_r		200	300	ns
Turn Off Delay Time	t_s		100	150	ns
Fall Time	t_f		100	150	ns

(1) See test circuit.

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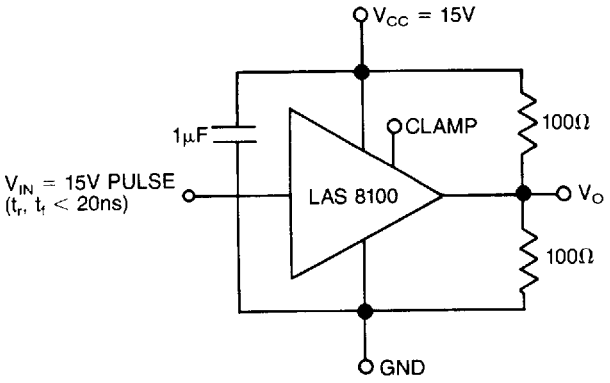
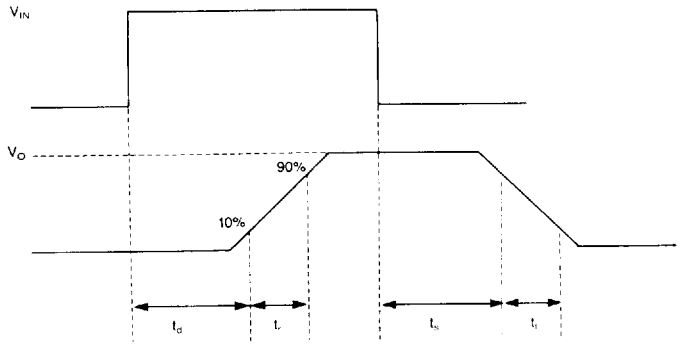
3 AMP PEAK SWITCHING TRANSISTOR DRIVERS

OPERATIONAL DATA

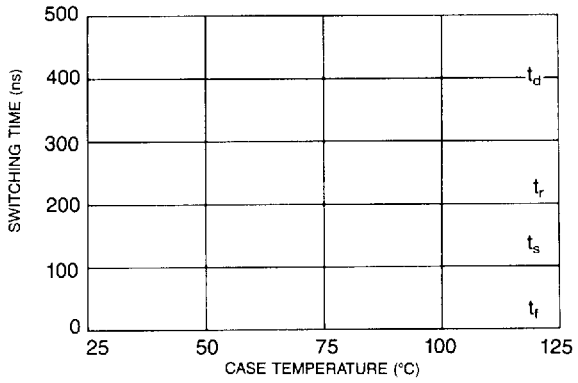
SWITCHING CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES



SWITCHING TIME VS. CASE TEMPERATURE

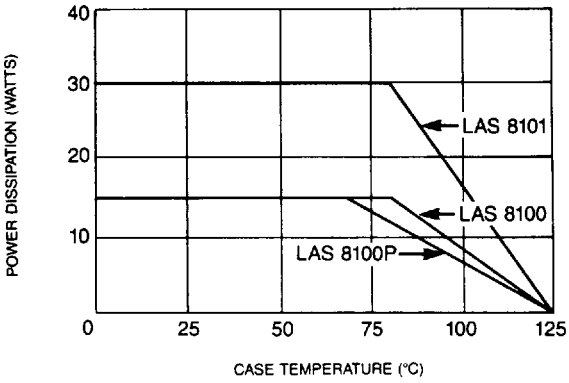


3 AMP PEAK SWITCHING TRANSISTOR DRIVERS

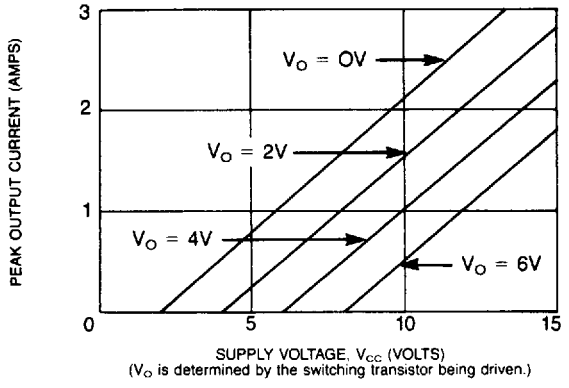
LAS-8100

OPERATIONAL DATA

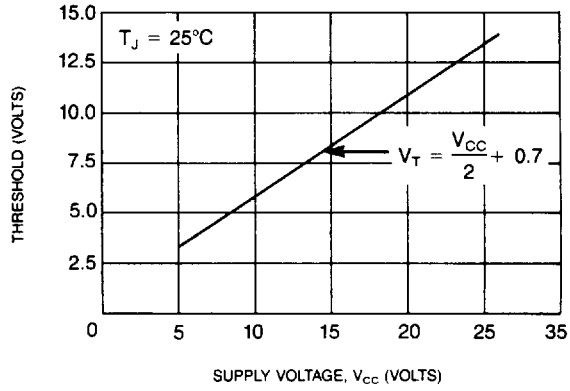
POWER DERATING



PEAK OUTPUT CURRENT VS. SUPPLY VOLTAGE



INPUT LOGIC THRESHOLD



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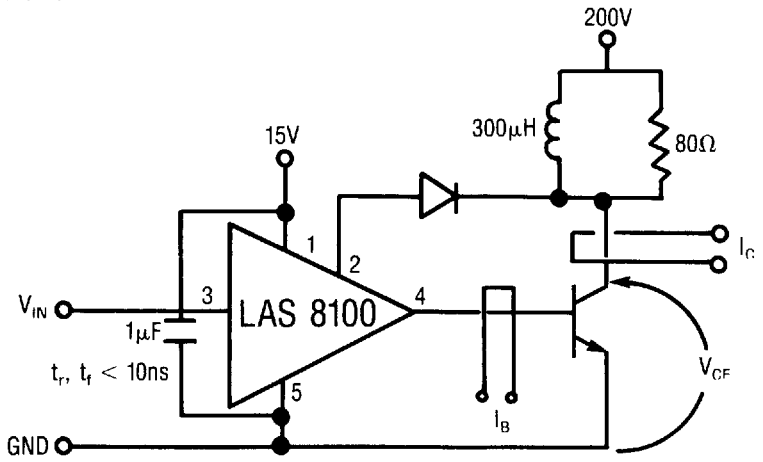
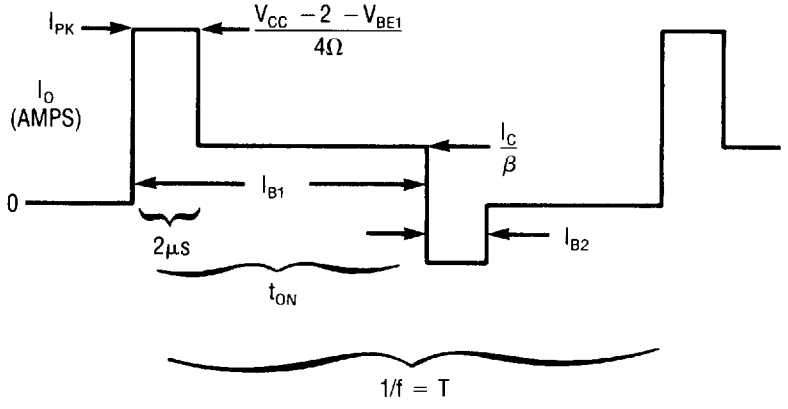
3 AMP PEAK SWITCHING TRANSISTOR DRIVERS

TYPICAL APPLICATION

TRANSISTOR DRIVER



LAS 8100 OUTPUT CURRENT



LAS 8100 AVERAGE POWER DISSIPATION

P_D (avg) = Energy of initial 2μs current pulse + Energy of DC current needed to drive transistor switch

$$= f\left\{\left(\frac{V_{CC} - 2 - V_{BE1}}{4\Omega}\right)(V_{CC} - V_{BE1})(2\mu s) + \frac{I_C}{\beta}(V_{CC} - V_{BE2})\left[(d.c.)(T) - 2\mu s\right]\right\},$$

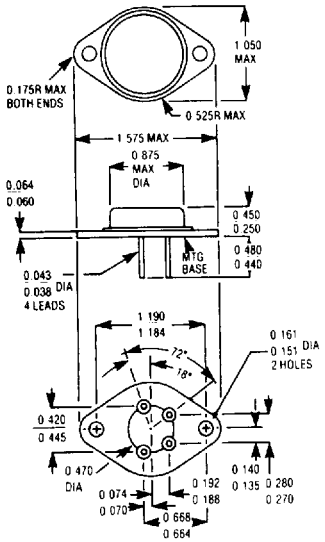
where V_{BE1} = base voltage of switch at turn-on
V_{BE2} = base voltage of switch at steady state
d.c. = $\frac{t_{on}}{T}$, duty cycle

3 AMP PEAK SWITCHING TRANSISTOR DRIVERS

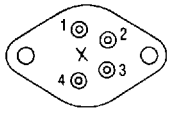
LAS-8100

DEVICE OUTLINE

LAS 8100

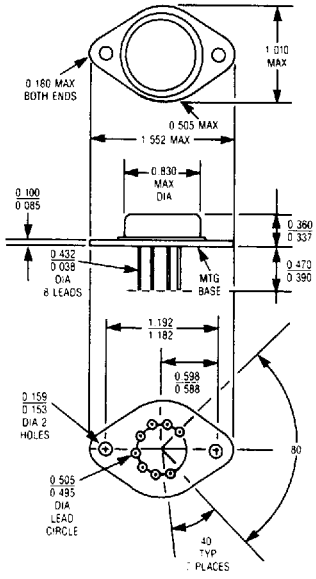


Bottom View

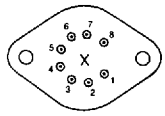


1 – V_{CC}
2 – Clamp
3 – Logic Input
4 – Output
Case is Ground

LAS 8101



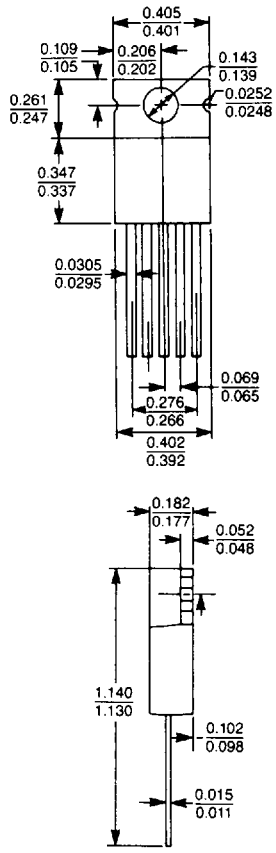
Bottom View



1 – Output 1
2 – V_{CC} 1
3 – Clamp 1
4 – Logic Input 1
5 – Output 2
6 – V_{CC} 2
7 – Clamp 2
8 – Logic Input 2
Case is Ground 1, 2

LAS 8100P

(Front View)



1 – V_{CC}
2 – Clamp
3 – Ground
4 – Logic Input
5 – Output
Tab is Ground

NOTE: All dimensions are in inches.

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