Ordering number : ENA0898

SANYO Semiconductors
DATA SHEET

LA74308LP — Monolithic Linear IC
Audio Interface for DSC

Overview

The LA74308LP is a SPEAKER AMP and MIC AMP built-in audio interface for DSC.
It incorporates an 8/16kHz trap and supports CODECs with a sampling rate of 8kHz or 16kHz.

Features

- Three-wire type SERIAL communication
- MIC AMP
- MIC power supply incorporated (with built-in pull-up resistor)
- ALC AMP
- 4th order LPF + trap (compatible with REC/PB changeover, trap frequency selectable from 8kHz and 16kHz)
- SPEAKER AMP (The BEEP signal can be mixed.), with electronic VOLUME (controlled by serial communication)
- LINE output (with SERIAL MUTE and MUTE transistor)
- STANDBY control

Specifications

Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.0	V
Allowable power dissipation	Pd max	Ta≤85°C *	500	mW
Operating temperature	Topr		-10 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Printed circuit board mounting condition (40mm × 50mm × 0.8mm: glass epoxy) 2S2P (Four layers printed circuit board)

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Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	$V_{CC}A$		3.0	V
	$V_{CC}SP$		3.3	V
Allowable operating voltage range	$V_{CC}Aop$		2.7 to 3.6	V
	$V_{CC}SPop$	Take care not to exceed Pd max.	2.7 to 3.6	V

Electrical Characteristics at Ta=25°C, $V_{CC}A$=3.0V, $V_{CC}SP$=3.3V, f=1kHz, with the VREF capacitance charging circuit in the OFF MODE

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current						
$V_{CC}A$ current dissipation at no signal 1	$I_{CC}A1$	$V_{CC}A$=3.0V:REC BLOCK(MIC/ALC/REC AMP) POWER SAVE MODE	4.9	6.6	8.3	mA
$V_{CC}A$ current dissipation at no signal 2	$I_{CC}A2$	$V_{CC}A$=3.0V, LINE/SP AMP POWER SAVE MODE	6.2	8.3	10.4	mA
$V_{CC}A$ standby current dissipation 1	$I_{CC}AS1$	$V_{CC}A$=3.0V, during standby control V3=0V			1	μA
$V_{CC}A$ standby current dissipation 2	$I_{CC}AS2$	$V_{CC}A$=3.0V, BIAS MODE			800	μA
$V_{CC}SP$ current dissipation at no signal 1	$I_{CC}S1$	$V_{CC}SP$=3.3V, SPK POWER ON MODE	1	2	4	mA
$V_{CC}SP$ current dissipation at no signal 2	$I_{CC}S2$	$V_{CC}SP$=3.3V, SPK POWER SAVE MODE		0.05	0.1	mA
$V_{CC}SP$ standby current dissipation 1	$I_{CC}SS1$	$V_{CC}SP$=3.3V, during standby control (0V applied to pin 3)			9	μA
$V_{CC}SP$ standby current dissipation 2	$I_{CC}SS2$	$V_{CC}SP$=3.3V, BIAS MODE			9	μA
REC output system						
REC reference output LEVEL	VOR	ALC IN, V_{IN}=-53dBV	-11	-9.5	-8	dBV
REC reference output distortion	HDR1	ALC IN, V_{IN}=-53dBV, THD: from 2nd to 5th harmonic		0.1	0.2	%
ALC characteristics	ALM	ALC IN, V_{IN}=-20dBV	-3	-1.8		dBV
ALC distortion	ALMD	ALC IN, V_{IN}=-20dBV, THD: from 2nd to 5th harmonic		0.3	1	%
ALC IN max input level	VINRMX	ALC IN LEVEL at which REC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-7	dBV
REC output noise voltage	VNOR	ALC IN, no input, JIS-A Filter		-70	-60	dBV
LINE output system (LINE load = as measured at the 22kΩ end)						
LINE reference output LEVEL	VOL	PB IN, V_{IN}=-17dBV	-11	-9.5	-8	dBV
LINE reference output distortion	HDL	PB IN, V_{IN}=-17dBV, THD: from 2nd to 5th harmonic		0.1	0.2	%
LINE reference output noise voltage	VNOL	PB IN, no input, JIS-A Filter		-77	-69	dBV
PB IN max input LEVEL	VINPMX	PB IN LEVEL at which LINE output THD (from 2nd to 5th harmonic) becomes 1% or less.			-9	dBV
LINE output frequency characteristics 1	FEQP1	PB IN, V_{IN}=-10dBV, comparison of f=3kHz/1kHz	-3.5	-2		dB
LINE output frequency characteristics 2	FEQP2	PB IN, V_{IN}=-10dBV, comparison of f=4kHz/1kHz		-10	-6	dB
LINE output frequency characteristics 3	FEQP3	PB IN, V_{IN}=-10dBV, comparison of f=8kHz/1kHz		-55	-30	dB
SP output system (SP load = as measured at the 8Ω end)						
SP reference output LEVEL1 (Vol.MAX)	VOSP1	PB IN, V_{IN}=-17dBV, Vol=MAX (EVR DATA=31)	-6	-3	0	dBV
SP reference output distortion	THDSP	PB IN, V_{IN}=-17dBV, Vol=MAX, THD: from 2nd to 5th harmonic		0.4	1	%
SP reference output LEVEL2 (Vol.TYP)	VOSP2	PB IN, V_{IN}=-17dBV, Vol=TYP (EVR DATA=14)	-18	-12	-6	dBV
SP reference output LEVEL3 (Vol.MIN)	VOSP3	PB IN, V_{IN}=-17dBV,Vol=MIN (EVR DATA=0) JIS-A Filter		-80	-70	dBV
SP reference output noise voltage	VNOSP	PB IN no input, Vol=MAX, JIS-A Filter		-70	-64	dBV
SP maximum ratings output	VOMSP	PB IN, Vol=MAX, LEVEL at which THD=10%	200	320		mW

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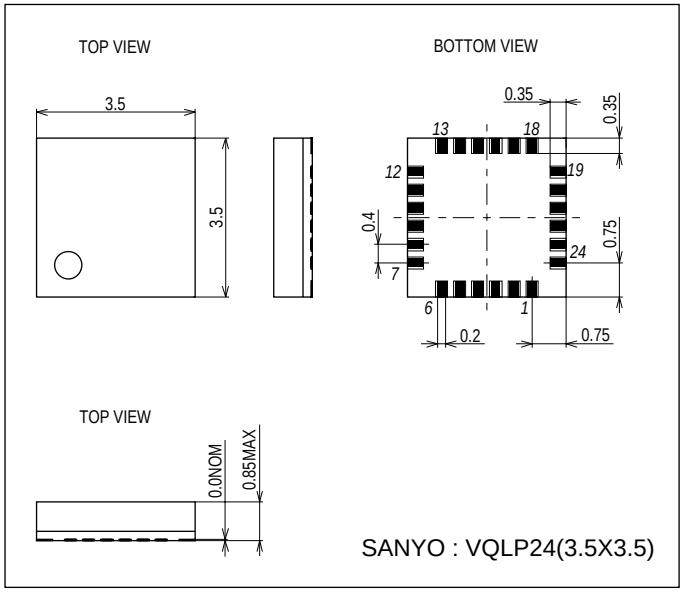
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
MIC output system						
MIC voltage gain	VGMIC	MIC IN, V_{IN}=-36dBV	16	17	18	dB
MIC output distortion	HDMIC	MIC IN, V_{IN}=-36dBV, THD: from 2nd to 5th harmonic		0.05	0.1	%
MIC output noise voltage	VNOMIC	MIC IN, no input, JIS-A Filter		-94	-83	dBV
MIC IN max input level	VINMMX	MIC IN LEVEL at which the MIC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-25	dBV
MIC V_{CC} output voltage	VMIC	At 6.2kΩ load	1.5	1.7	1.9	V
Control system						
Serial CLOCK frequency	FCLK			0.1	1	MHz
Serial input LOW level	SERLO		0		0.7	V
Serial input HIGH level	SERHI		2.3		3.5	V

Package Dimensions

unit : mm (typ)

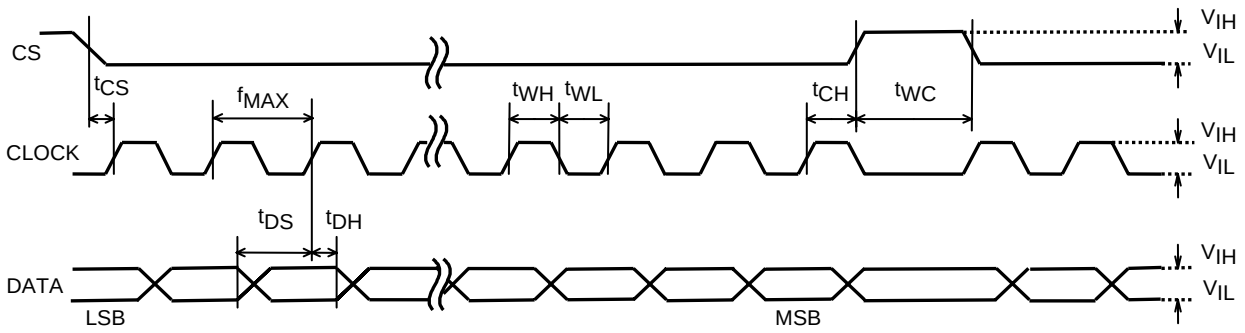
3321



Description of the Content of Serial Communication

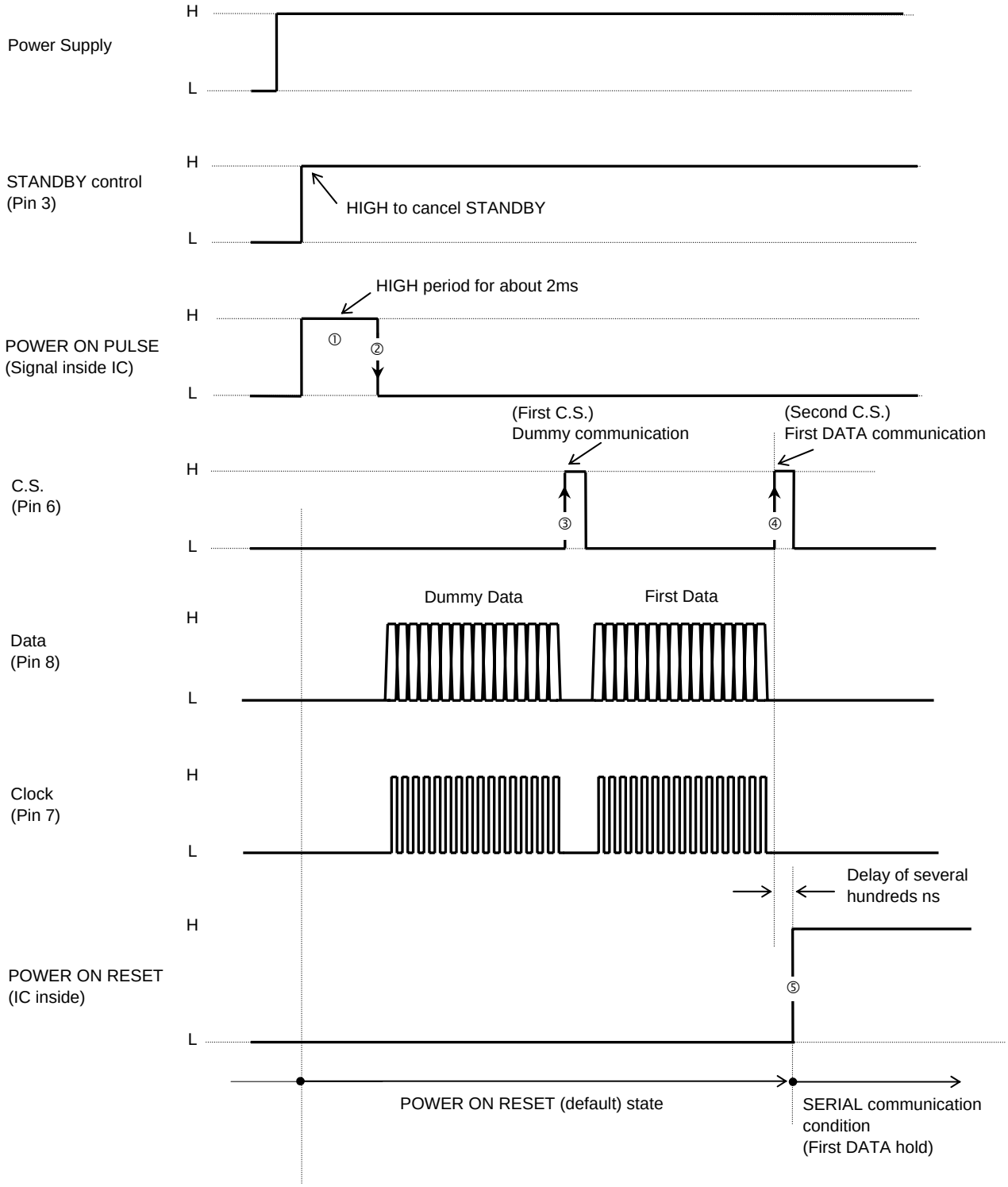
	DATA No.	Parameter		Default
LSB	0	LINE MUTE Tr.	0:OFF, 1:ON	1
	1	VREF capacitance charging circuit SW	0:OFF, 1:ON	1
	2	MIC AMP POWER SW	0:ON, 1:OFF	1
	3	ALC AMP POWER SW	0:ON, 1:OFF	1
	4	REC/PB changeover SW	0:PB, 1:REC	0
	5	LPF characteristics (TRAP) changeover SW	0:16kHz, 1:8kHz	1
	6	REC AMP POWER SW	0:ON, 1:OFF	1
	7	LINE OUT POWER SW	0:ON, 1:OFF	1
	8	LINE MUTE SW	0:OFF, 1:ON	1
	9	SPK POWER SW	0:ON, 1:OFF	1
	10	DATA=1	1 1 1 1 1:VOL MAX	0
	11	DATA=2	≀	0
	12	DATA=4	0 0 0 0 0:VOL MIN (MUTE)	0
	13	DATA=8	* EVR setting (the numeral shown in the left is decimal.	0
	14	DATA=16	For characteristics, see P12.)	0
MSB	15	BIAS MODE	0:ACTIVE MODE, 1:BIAS MODE	0

Serial Transmission Timing



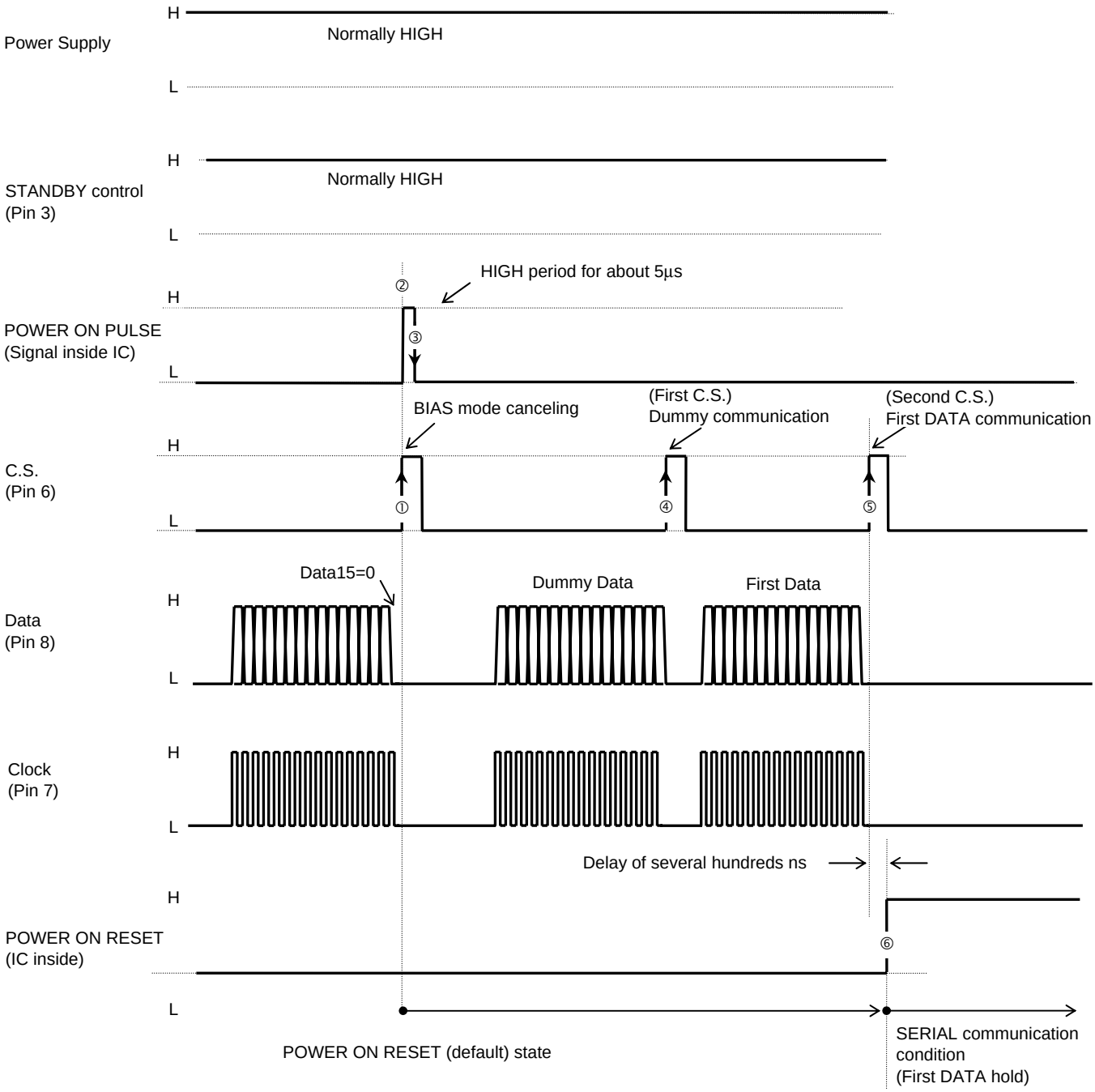
- f_{MAX} (Max clock frequency) 1.0MHz
- t_{WL} (Clock pulse width: Low) 500ns or more
- t_{WH} (Clock pulse width: High) 500ns or more
- t_{CS} (Chip enable setup time) 500ns or more
- t_{CH} (Chip enable hold time) 500ns or more
- t_{DS} (Data setup time) 500ns or more
- t_{DH} (Data hold time) 500ns or more
- t_{WC} (Chip enable pulse width) 500ns or more
- V_{IH} (High voltage lower limit) 2.3V to 3.5V
- V_{IL} (Low voltage upper limit) 0.0V to 0.7V

POWER ON RESET Condition (SERIAL communication)



The POWER ON RESET state covers a period up to the rise ④ of the second C.S. input after fall ② of POWER ON PULSE ① generated inside IC when the power is supplied and the STANDBY control is canceled. ③ is the dummy communication.
Actually, because of delay of several hundreds ns in the IC, the first DATA condition begins in ⑤ and the normal SERIAL communication condition begins after ⑤.

BIAS MODE Canceling State (SERIAL communication)



The POWER ON RESET state from the BIAS MODE covers the period from the rise of C.S ① for communication of canceling of the BIAS MODE to the second rise ⑤ of CS input after the fall ③ of POWER ON PULSE ② generated inside IC. ④ is the dummy communication.

Actually, because of delay of several hundreds ns in the IC, the first DATA condition begins in ⑥ and the normal SERIAL communication condition begins after ⑥.

Electrical Characteristics Measurement Method at Ta=25°C, $V_{CC}A$=3.0V, $V_{CC}SP$=3.3V, f=1kHz with the VREF capacitance charging circuit in the OFF MODE

No.	Symbol	Input			Output		STANDBY pin	Serial control setting																
		Pin	Conditions		Pin	Major conditions (for the serial control setting, see the table in the right)	Voltage applied to pin 3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
								LINE Mute Tr.	VREF charging SW	MIC P SW	ALC P SW	REC /PB SW	LPF TRAP	REC P SW	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	BIAS MODE
								0:OFF 1:ON	0:OFF 1:ON	0:ON 1:OFF	0:ON 1:OFF	0:PB 1:REC	0:16kHz 1:8kHz	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:ACTIVE 1:BIAS
	Circuit current																						
1	I_{CCA1}	T11	$V_{CC}A$=3.0V No input		T11	VREF capacitance charging circuit in the OFF MODE MIC/ALC/REC AMP POWER SAVE MODE	3.3V	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0
2	I_{CCA2}	T11	$V_{CC}A$=3.0V No input		T11	VREF capacitance charging circuit in the OFF MODE LINE/SP AMP POWER SAVE MODE	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
3	I_{CCAS1}	T11	$V_{CC}A$=3.0V No input		T11	With the STANDBY pin V3=0V	0V	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
4	I_{CCAS2}	T11	$V_{CC}A$=3.0V No input		T11	BIAS MODE	3.3V	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1
5	I_{CCS1}	T22	$V_{CC}SP$=3.3V No input		T22	VREF capacitance charging circuit in the OFF MODE SPK POWER ON MODE	3.3V	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0
6	I_{CCS2}	T22	$V_{CC}SP$=3.3V No input		T22	VREF capacitance charging circuit in the OFF MODE SPK POWER SAVE MODE	3.3V	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	0
7	I_{CCSS1}	T22	$V_{CC}SP$=3.3V No input		T22	With the STANDBY pin V3=0V	0V	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0
8	I_{CCSS2}	T22	$V_{CC}SP$=3.3V No input		T22	BIAS MODE	3.3V	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	1
	REC output system																						
9	VOR	T14	V_{IN}=-53dBV f=1kHz		T12	400 to 20kHz LPF used SW14=A, SW16=B	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
10	HDR1	T14	V_{IN}=-53dBV f=1kHz		T12	400 to 20kHz LPF used, SW14=A SW16=B, THD: from 2nd to 5th harmonic	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
11	ALM	T14	V_{IN}=-20dBV f=1kHz		T12	400 to 20kHz LPF used, SW14=A, SW16=B	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
12	ALMD	T14	V_{IN}=-20dBV f=1kHz		T12	400 to 20kHz LPF used, SW14=A SW16=B, THD: from 2nd to 5th harmonic	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
13	VINRMX	T14	f=1kHz		T12	400 to 20kHz LPF used, SW16=B Pin 14 level at which pin 12 becomes THD = 3% from 2nd to 5th harmonic)	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
14	VNOR	T14	No input		T12	JIS-A FILTER used SW14=B, SW16=B	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0

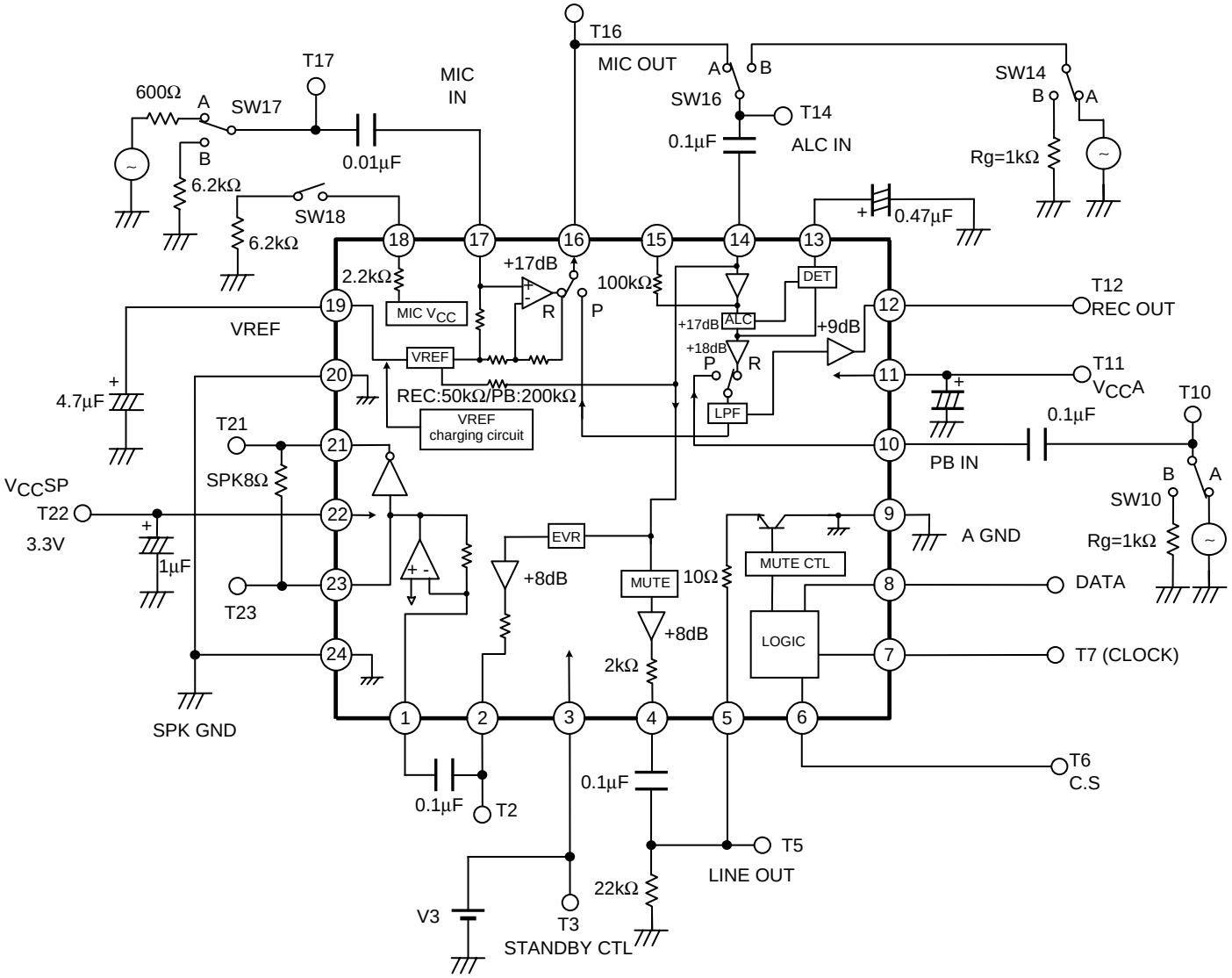
No.	Symbol	Input		Output		STANDBY pin	Serial control setting														
		Pin	Conditions	Pin	Major conditions (for the serial control setting, see the table in the right)	Voltage applied to pin 3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
							LINE Mute Tr.	VREF charging SW	MIC P SW	ALC P SW	REC /PB SW	LPF TRAP	REC P SW	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	BIAS MODE
							0:OFF 1:ON	0:OFF 1:ON	0:ON 1:OFF	0:ON 1:OFF	0:PB 1:REC	0:16kHz 1:8kHz	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:ACTIVE 1:BIAS
LINE output system																					
15	VOL1	T10	V_{IN}=-17dBV f=1kHz	T5	400 to 20kHz LPF used SW10=A, SW16=A	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
16	HDL	T10	V_{IN}=-17dBV f=1kHz	T5	400 to 20kHz LPF used, SW10=A SW16=A, THD: from 2nd to 5th harmonic	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
17	VNOL	T10	No input	T5	JIS-A FILTER used, SW10=B, SW16=A	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
18	VINPMX	T10	f=1kHz	T5	400 to 20kHz LPF used, SW10=A, Pin 10 level at which pin 5 becomes THD = 3% (from 2nd to 5th harmonic)	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
19	FEQP1	T10	V_{IN}=-10dBV f=3kHz	T5	f=3kHz/1kHz level ratio SW10=A, SW16=A	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
20	FEQP2	T10	V_{IN}=-10dBV f=4kHz	T5	f=4kHz/1kHz level ratio SW10=A, SW16=A	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
21	FEQP3	T10	V_{IN}=-10dBV f=8kHz	T5	f=8kHz/1kHz level ratio SW10=A, SW16=A	3.3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
SPK output system (SPK end: measured with 8Ω)																					
22	VOSP1	T10	V_{IN}=-17dBV f=1kHz	T21 T23	400 to 20kHz LPF used Vol.=MAX (EVR DATA=31)	3.3V	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1	0
23	THDSP	T10	V_{IN}=-17dBV f=1kHz	T21 T23	400 to 20kHz LPF used, Vol.=MAX THD: from 2nd to 5th harmonic	3.3V	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1	0
24	VOSP2	T10	V_{IN}=-17dBV f=1kHz	T21 T23	400 to 20kHz LPF used Vol.=TYP (EVR DATA=14)	3.3V	0	0	1	1	0	1	1	1	1	0	0	1	1	1	0	0
25	VOSP3	T10	V_{IN}=-17dBV f=1kHz	T21 T23	JIS-A FILTER used Vol.=MIN (EVR DATA=0)	3.3V	0	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0
26	VNOSP	T10	No input	T21 T23	JIS-A FILTER used Vol.=MAX (EVR DATA=31)	3.3V	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1	0
27	VOSSP	T10	f=1kHz	T21 T23	400 to 20kHz LPF used Vol.=MAX (EVR DATA=31) Level at which Vol.=MAX and THD=10% (from 2nd to 5th harmonic)	3.3V	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1	0

No.	Symbol	Input		Output		STANDBY pin	Serial control setting													
		Pin	Conditions	Pin	Major conditions (for the serial control setting, see the table in the right)	Voltage applied to pin 3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
							LINE Mute Tr.	VREF charging SW	MIC P SW	ALC P SW	REC /PB SW	LPF TRAP	REC P SW	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	BIAS MODE
							0:OFF 1:ON	0:OFF 1:ON	0:ON 1:OFF	0:ON 1:OFF	0:PB 1:REC	0:16kHz 1:8kHz	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:ACTIVE 1:BIAS
MIC Output system																						
28	VGMIC	T17	V_{IN}=-36dBV f=1kHz	T16	400 to 20kHz LPF used, SW17=A	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
29	HDMIC	T17	V_{IN}=-36dBV f=1kHz	T16	400 to 20kHz LPF used, SW17=A THD: from 2nd to 5th harmonic	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
30	VNOMIC	T17	No input	T16	JIS-A FILTER used, SW17=B	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
31	VINMMX	T17	f=1kHz	T16	400 to 20kHz LPF used, SW17=A Pin 17 level at which pin 16 becomes THD = 3% (from 2nd to 5th harmonic)	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0
32	VMIC	T17	No input	T18	Pin 18 Measurement of output voltage (under 6.2kΩ load) SW18=ON	3.3V	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0

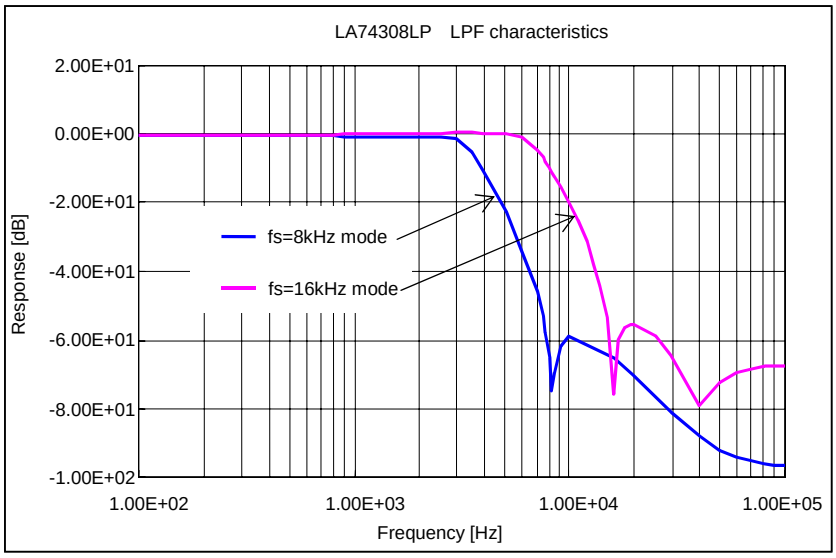
Description of Pin Functions

Pin No.	Pin Description
1	Speaker input
2	EVR output
3	STANDBY control
4	LINE output
5	LINE MUTE Tr. output
6	C.S. input
7	CLOCK input
8	DATA input
9	GND
10	PB input
11	$V_{CC}A$
12	REC output
13	ALC detection
14	ALC input
15	2nd order HPF
16	MIC output
17	MIC input
18	INT power supply for MIC
19	Ripple rejection for VREFL
20	SPK GND
21	Speaker positive-phase output
22	$V_{CC}SP$
23	Speaker negative-phase output
24	SPK GND

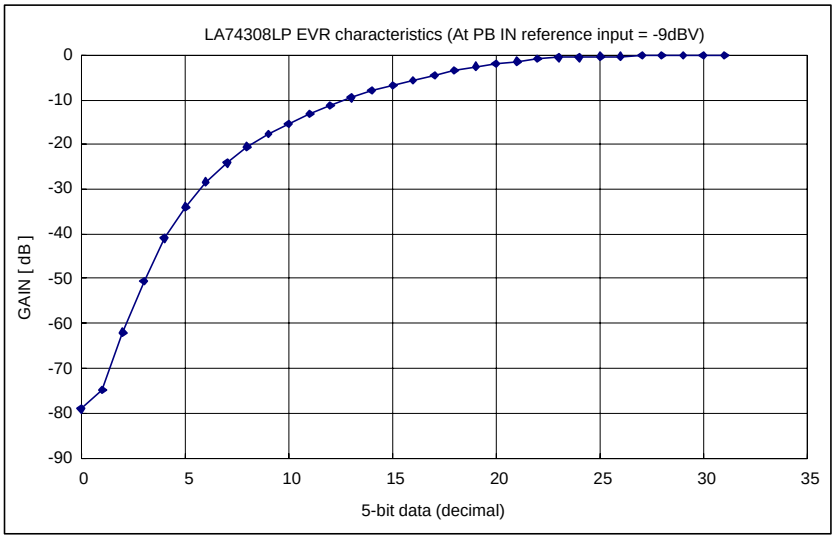
Block Diagram



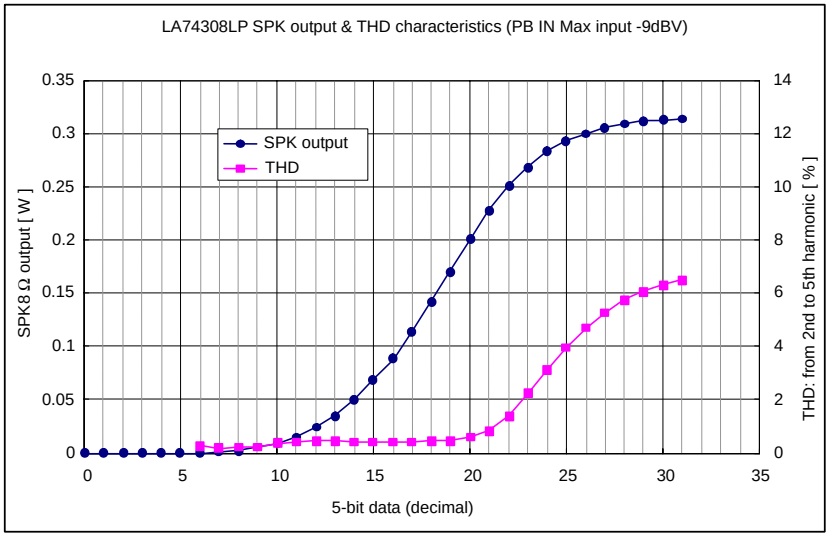
LPF Characteristics



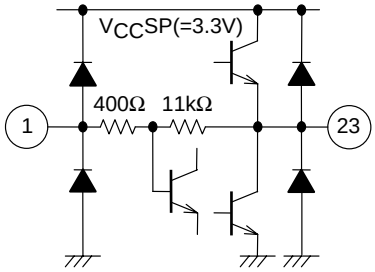
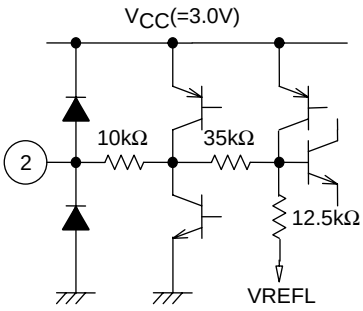
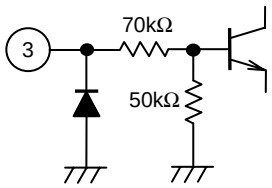
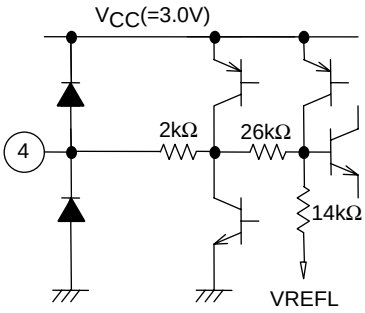
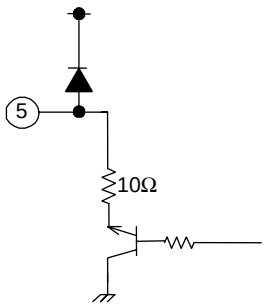
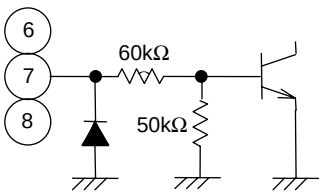
EVR Characteristics



SPK Output Level & Distortion Rate



LA74308LP Input/output Pattern Table

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
1	SP IN	1.27V	At PB reference input Output level = -9dBV (EVR MAX)	Speaker input pin	
23	SPK OUT-	1.27V	At PB reference input Output level = -9dBV (EVR MAX)	Speaker negative-phase output pin	
2	EVR OUT	1.5V		EVR output pin	
3	STANDBY L			STANDBY control pin 2V or more: STANDBY canceled	
4	LINE OUT			LINE output pin	
5	LINE MUTE	1.5V	At PB reference input Output level = -9dBV	LINE output mute transistor	
6 7 8	CS CLOCK DATA			CS input pin CLOCK input pin DATA input pin	

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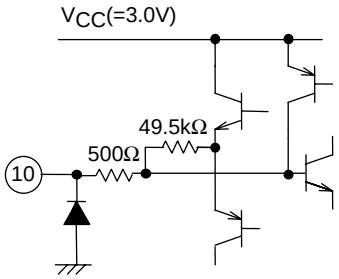
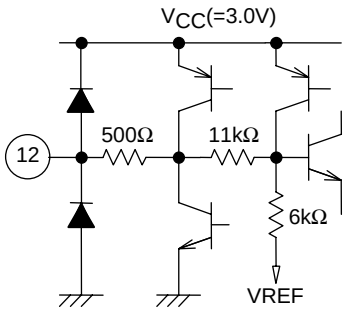
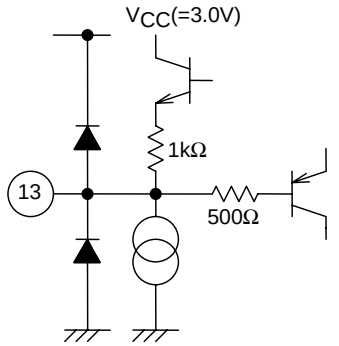
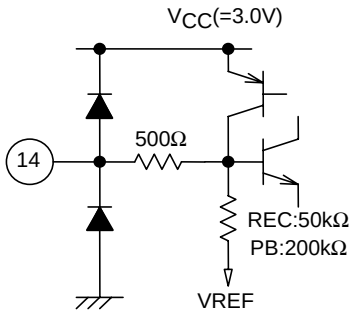
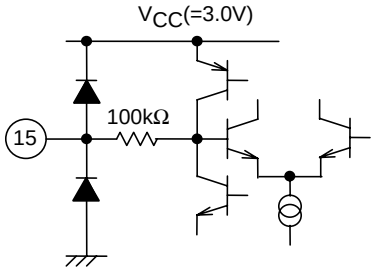
PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
9	GND	0V		GND pin	
10	PB IN	1.5V	Reference input level =-17dBV	PB input pin	
11	V_{CC}	3V		Power supply pin	
12	REC OUT	1.5V	Reference input level =-9dBV	R output pin	
13	ALC DET			ALC detection pin	
14	ALC IN (REC)	1.5V	Reference input level =-53dBV Max input level =-8dBV	ALC input pin	
	EVR IN (PB)	1.5V		EVR input pin	
15	HPF	1.5V		Used when forming the 2nd order HPF	

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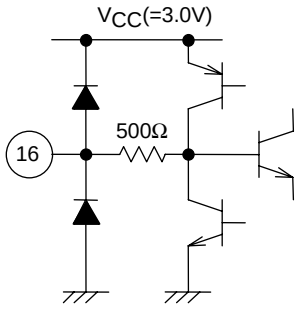
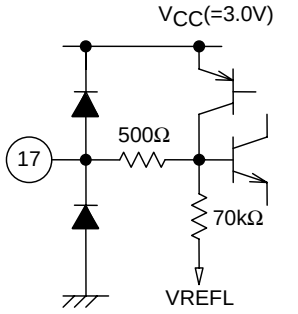
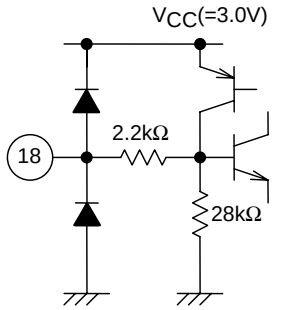
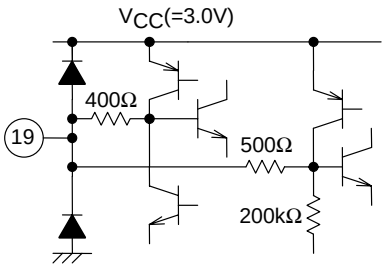
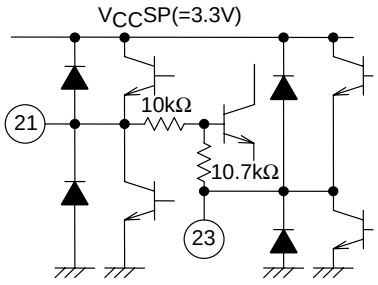
PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
16	MIC OUT (REC)	1.5V		MIC output pin (for REC mode)	
	LPF OUT (PB)			LPF output pin (for PB mode)	
17	MIC IN	1.5V	Reference input level =-70dBV Max input level =-25dBV	MIC input pin	
18	MIC V_{CC}	2.30V		MIC power pin	
19	VREFL	2.30V		MIC V_{CC} and VREFL ripple rejection pin	
20 24	SP GND	0V		Speaker GND pin	
21	SPK OUT+	1.27V	At PB reference input Output level = -9dBV (EVR MAX)	Speaker positive-phase output pin	
22	V_{CC}SP	3.3V		Speaker power pin	

Application Circuit