



SANYO Semiconductors

DATA SHEET

LA6575H — Monolithic Digital IC

Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

Overview

The LA6575H is a five-channel motor driver IC for MD and CD players with four BTL channels and one H bridge channel for the loading motor. It features a built-in 5 V regulator circuit.

Functions and Features

- Four power amplifier channels plus one H bridge channel
- I_O max: 700 mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- One muting circuit system (output on/off control): applies to the BTL amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 5 V regulator

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	P_{dmax}	Independent IC	0.82	W
		* Mounted on a board.	2.0	
Maximum output current	I_O max	Each channel for CH1 to CH5	0.7	A
Maximum input voltage	VINB		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	T_{opr}		-30 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to $+150$	$^\circ\text{C}$

Note *: Mounted on a board (76.1 × 114.3 × 1.6 mm) Material: glass epoxy

Recommended Operating Conditions

 at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

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LA6575H

Electrical Characteristics (Unless specified otherwise, the conditions are $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{ V}$, $V_{REF} = 1.65\text{ V}$)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall Characteristics]						
No load current drain - ICC on	I _{CC-ON}	All outputs on, FWD = REV = 0 V *1		30	50	mA
No load current drain - ICC off	I _{CC-OFF}	All outputs off, FWD = REV = 0 V *1		10	20	mA
VREF input voltage range	VREF-IN		1		V _{CC} -1.5	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	BTL amplifiers, the voltage difference across each channel's output	-50		+50	mV
Input voltage range	V _{IN}	Input voltage range	0		V _{CC}	V
Output voltage	V _O	The voltage between each of the V _O +/V _O - pairs when R _L is 8 Ω. *2	4	5		V
Closed loop voltage gain	VG	Gain from input to output	3.5	4	4.5	Multi-plier
Slew rate	SR	With the amplifier operating independently, twice the value measured between outputs *4		0.5		V/μs
Mute on voltage	VMUTE-ON	Each Mute *3			0.5	V
Mute off voltage	VMUTE-OFF	Each Mute *3	2			V
[H Bridge Block]						
Output voltage	V _{O-LOAD}	The voltage between each of the V _O +/V _O - pairs when R _L is 8 Ω. *2	5.6	6		V
Low-level input voltage	V _{IN-L}				1	V
High-level input voltage	V _{IN-H}		2			V
[Regulator Block]						
Output voltage	Vreg	I _L = 100 mA	4.75	5	5.25	V
Load regulation	ΔVRL	I _L = 0 to 200 mA	-50	0	+10	mV
Line regulation	ΔVVCC	V _{CC} = 6 to 12 V, I _I = 100 mA	-15	+21	+60	mV

Note *1: The total current drain for V_{CC1} and V_{CC2} with no load.

*2: Voltage difference across the load ($8\ \Omega$). With the outputs in the saturated state.

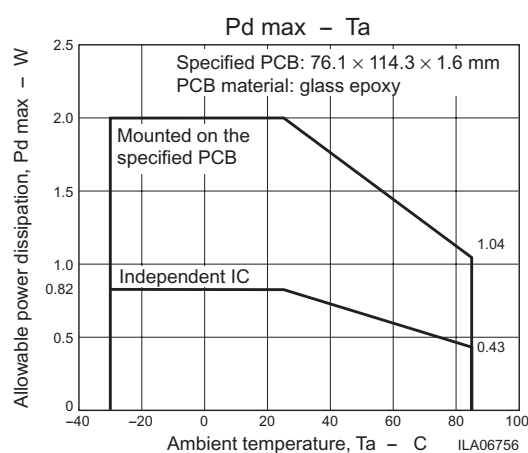
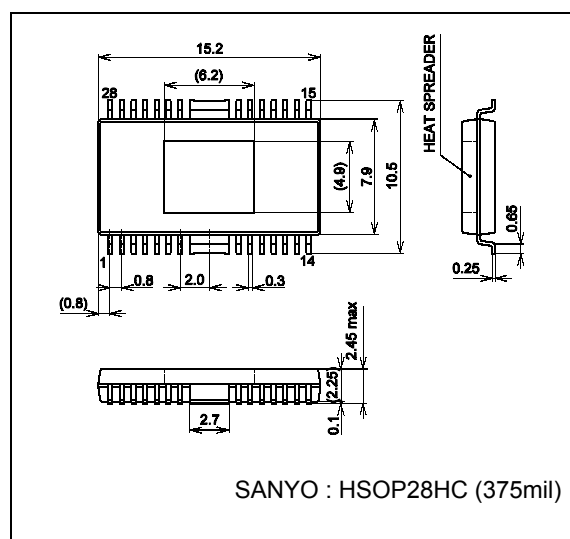
*3: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off (high-impedance state).

*4: Design guarantee value

Package Dimensions

unit: mm

3234B



Pin Functions

Pin No.	Symbol	Pin descriptions
1	V _{CC2}	Channel 5 power supply
2	V _{O5-}	Loading output (-)
3	V _{O5+}	Loading output (+)
4	V _{O4+}	Channel 4 output (+)
5	V _{O4-}	Channel 4 output (-)
6	V _{O3+}	Channel 3 output (+)
7	V _{O3-}	Channel 3 output (-)
8	V _{O2+}	Channel 2 output (+)
9	V _{O2-}	Channel 2 output (-)
10	V _{O1+}	Channel 1 output (+)
11	V _{O1-}	Channel 1 output (-)
12	V _{CC1}	Channels 1 to 4 (BTL) power supply (This pin must be shorted to V _{CC-S})
13	V _{IN1}	Channel 1 input
14	V _{IN1G}	Channel 1 input (gain adjustment input)
15	V _{IN2}	Channel 2 input
16	V _{IN2G}	Channel 2 input (gain adjustment input)
17	V _{IN3}	Channel 3 input
18	V _{IN3G}	Channel 3 input (gain adjustment input)
19	REG-IN	Regulator input (external pnp transistor base)
20	REG-OUT	Regulator output (external pnp transistor collector)
21	VREF-IN	Reference voltage input
22	V _{CC-S}	Signal system power supply (This pin must be shorted to V _{CC1} .)
23	V _{IN4G}	Channel 4 input (gain adjustment input)
24	V _{IN4}	Channel 4 input
25	MUTE	Channels 1 to 4 (BTL amplifiers) output on/off control
26	S-GND	Signal system ground
27	FWD	Channel 5 (VLO) output switching (FWD); loading block logic input
28	REV	Channel 5 (VLO) output switching (REV); loading block logic input

Note: • The center frame (FR) is used as the power system ground. Along with the signal system ground (S-GND), this level must be the lowest potential in the system.

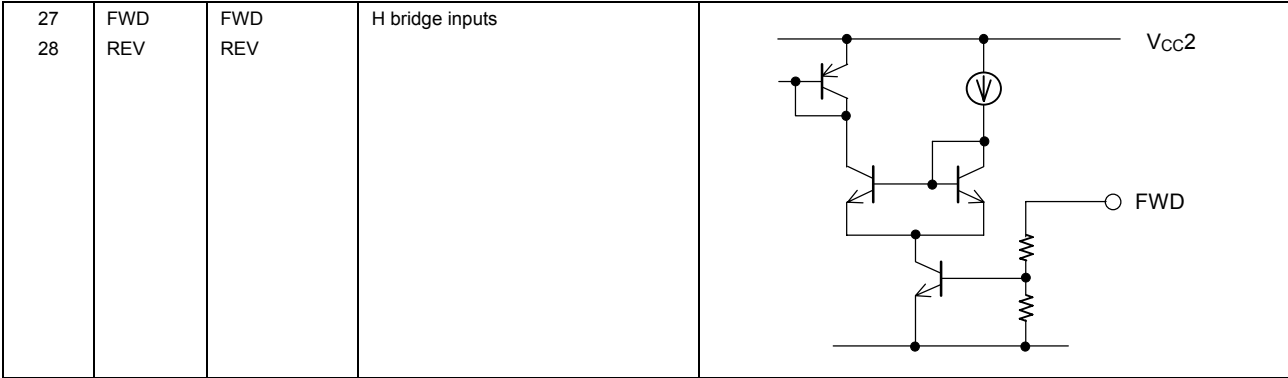
• The three power supply pins V_{CC-S}, V_{CC1}, and V_{CC2} must be shorted together externally.

Pin Functions

Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
13 14 15 16 17 18 23 24	V_{IN}	Inputs	Inputs	
4 5 6 7 8 9 10 11	V_O	Outputs	Outputs	
25	MUTE	Mute	ON/OFF each output MUTE: H output ON MUTE: L output OFF	
2 3	V_{O5+} V_{O5-}	V_{O5}	H bridge outputs	

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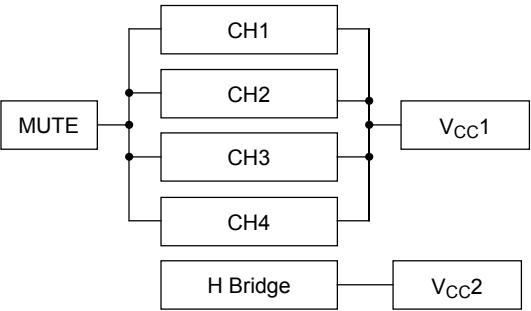


H Bridge Block

FWD	REV	V _{O5+}	V _{O5-}	Mode
L	L	OFF	OFF	Open *1
L	H	H	L	Forward
H	L	L	H	Reverse
H	H	L	L	Brake *2

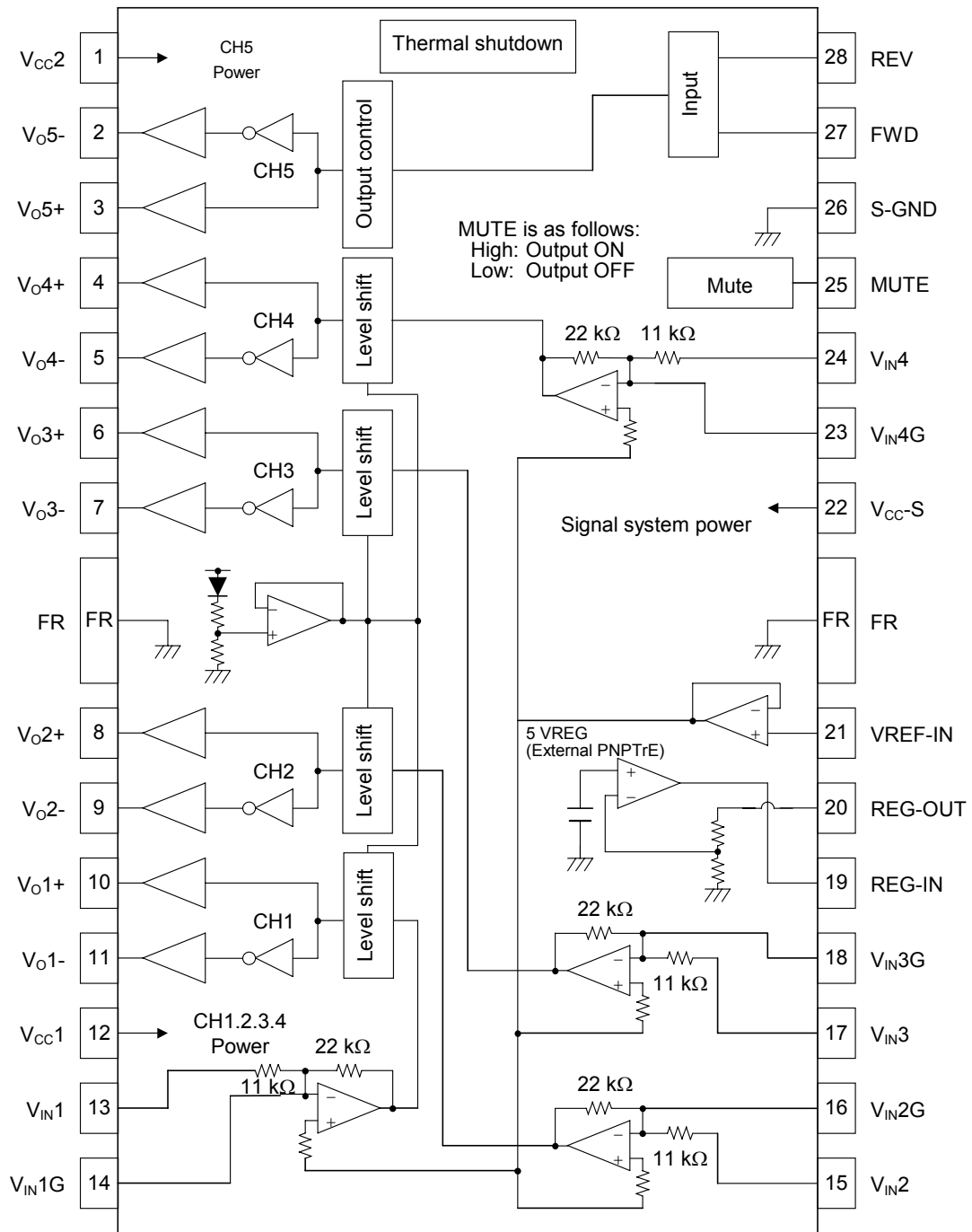
Note *1: The output are in the high-impedance state in this mode
*2: In brake mode, the sink side transistors are on (short-circuit braking). The VLO+ and VLO- levels go to a level essentially the same as the ground level.

Relationship between the MUTE pin and the power supplies (V_{CC}*)

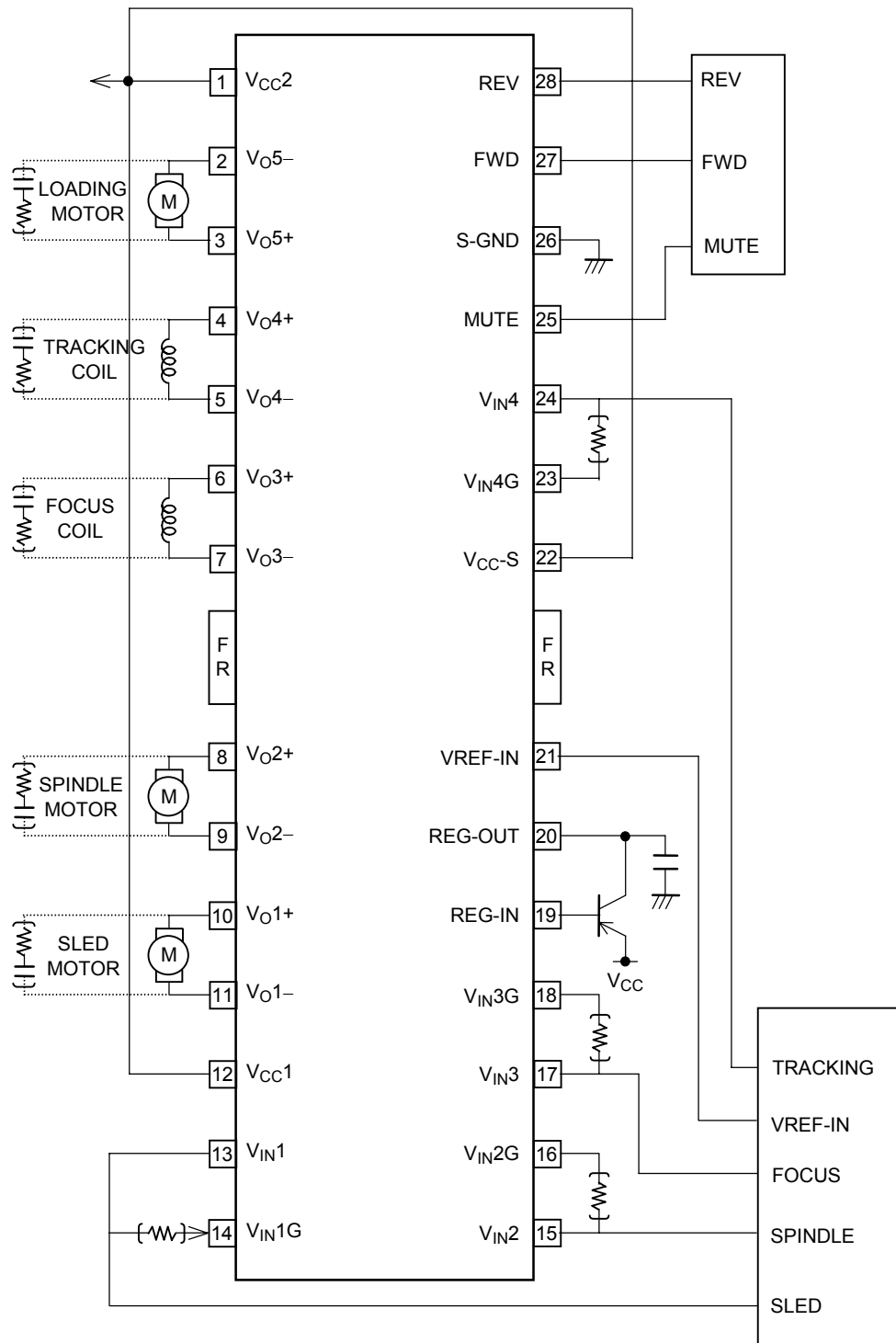


LA6575H

Block Diagram



Sample Application Circuit



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