

SANYO Semiconductors DATA SHEET

LA5643 — Monolithic Linear IC Multi-Power Supply System Regulator

Overview

The LA5643 is a multi-power supply IC that provides one 3.3V regulator circuits as well as two 5V regulator circuits. The LA5643 is optimal for MD players and other applications.

Functions

- 3.5V regulator circuit incorporated (I_O=150mA)
- Two 5V regulator circuits incorporated (I_O=1A,100mA)
- With power-down detector circuit
- Reset circuit operating on the VBAK voltage
- Small current dissipation of reset circuit (3.5µA typ during backup)
- Conversion of a 3.5V regulator into a 3.3V regulator through short-circuiting of ADJ pin with SYS3.5 pin

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage 1	V _{CC} 1 max		14	V
Input voltage 2	V _{CC} 2 max		14	V
AC input voltage	VAC max		14	V
Reset circuit input voltage	VBAK max		5	V
Allowable power dissipation	Pd max	Independent IC	2	W
Operating Temperature	Topr		-20 to +80	°C
Storage Temperature	Tstg		-55 to +150	°C

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LA5643

Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage 1	V _{CC} 1		7.75 to 12	V
Input voltage 2	V _{CC} ²		3.97 to 12	V
Reset circuit input voltage	VBAK		1.4 to 4	V
PH5 output current	IPH5		0 to 1	Α
ANA5 output current	IANA5		0 to 100	mA
SYS3.5 output current	ISYS3.3		0 to 150	mA
S.RESET sink current	ISINK_S		0 to 0.2	mA
P.DOWN sink current	ISINK_P		0 to 1	mA

Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			1.1
	Symbol	Conditions	min	typ	max	Unit
[All circuits (V _{CC} 1=10V, V _{CC} 2=	=5V, VBAK=3.1V))]				
V _{CC} 1 current dissipation 1	lcc1	IPH5=0mA, IANA5=0mA		3.5	5	mA
V _{CC} 2 current dissipation 2	I _{CC} 2	ISYS3.5=0mA, AC terminal=5V		3.5	5	mA
VBAK current dissipation 1	I _{IN} 1_VBAK	VBAK=3.1V (S.RESET terminal at "Hi" input)		3.5	5	μΑ
VBAK current dissipation 2	I _{IN} 2_VBAK	VBAK=1.8V (S.RESET terminal at "Low" input)		0.24		mA
[PH5 regulator block (V _{CC} 1=10)V, IPH5=1A)]					
Output voltage	V _O _PH5		4.75	5	5.25	V
Dropout voltage	VDROP_PH5			2	2.5	V
Line regulation	ΔVOLN_PH5	V _{CC} 1=7.75V to 12V			200	mV
Load regulation	∆VOLD_PH5	IPH5=5mA to 1A			200	mV
Peak output current	IOP_PH5		1	1.4		Α
Output short-circuit current	losc_PH5			0.4	1	Α
[ANA5 regulator block (V _{CC} 1=	10V, IANA5=100n	nA)]				
Output voltage	V _O _ANA5		4.75	5	5.25	V
Dropout voltage	VDROP_ANA5			2	2.5	V
Line regulation	ΔVOLN_ANA5	V _{CC} 1=7.75V to 12V			200	mV
Load regulation	ΔVOLD_ANA5	IANA5=5 to 100mA			200	mV
Peak output current	IOP_ANA5		100	140		mA
Output short-circuit current	losc_ANA5			40	100	mA
Output noise voltage	VNO_ANA	10Hz ≤ f ≤ 100kHz		120		μV
[SYS3.5 regulator block (V _{CC} 2	=5V, ISYS3.5=15	0mA)]				
Output voltage 1	V _O _SYS3.5		3.43	3.5	3.57	V
Output voltage 2	V _O _SYS3.5/3.3	SYS3.5 pin and ADJ pin short-circuited	3.23	3.3	3.37	V
Dropout voltage	VDROP_SYS3.5			0.25	0.4	V
Line regulation	∆VOLN_SYS3.5	V _{CC} 2=3.97V to 12V			200	mV
Load regulation	ΔVOLD_SYS3.5	ISYS3.3=5 to 150mA			200	mV
Peak output current	IOP_SYS3.5		150	210		mA
Output short-circuit current	losc_SYS3.5			75	150	mA
[P.DOWN detection circuit (V _C						
P.DOWN threshold voltage 1	Vth1_P.DOWN		2.7	2.78	2.86	V
P.DOWN threshold voltage 2	Vth2_P.DOWN	SYS3.5 pin and ADJ pin short-circuited				
P.DOWN hysteresis width	Vhys_P.DOWN		90	100	110	mV
P.DOWN residual voltage	Vsat_P.DOWN	cd1 terminal=Short P.DOWN terminal=1mA			200	mV
P.DOWN delay time	Td1	cd1=1μF	75	100	125	ms

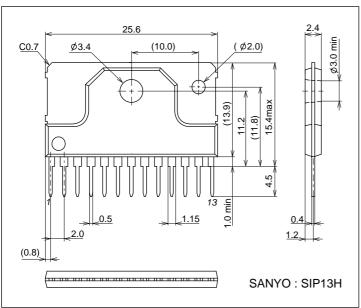
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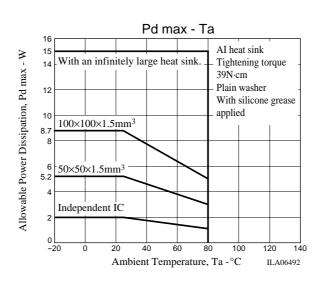
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Parameter	Symbol	Conditions	Ratings			I In it	
			min	typ	max	Unit	
[AC detection circuit (V _{CC} 2=5V	[AC detection circuit (V _{CC} 2=5V)]						
AC threshold voltage	Vth_AC		0.87	0.9	0.93	V	
AC hysteresis width	Vhys_AC		0.5	0.6	0.7	V	
AC pin drain current	IB_AC	VAC=0.8V		1.6		μΑ	
[S.RESET circuit (VBAK=3.3V)]							
S.RESET threshold voltage 1	Vth1_S.RESET		2.7	2.78	2.86	V	
S.RESET threshold voltage 2	Vth2_S.RESET		1.9	2.0	2.1	V	
Reset output undefined voltage	VUNS_S.RESET				1.4	V	
S.RESET residual voltage	Vsat_S.RESET	cd2 terminal=Short S.RESET termianl=0.2mA			200	mV	
S.RESET delay time	Td2	cd2=1μF	75	100	125	ms	

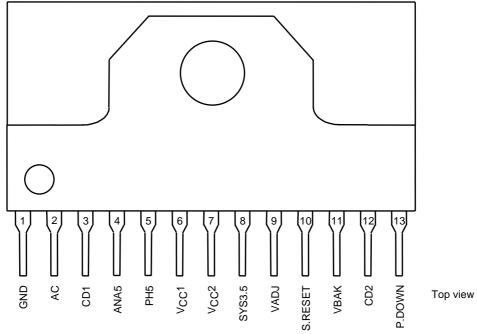
Package Dimensions

unit : mm 3170B

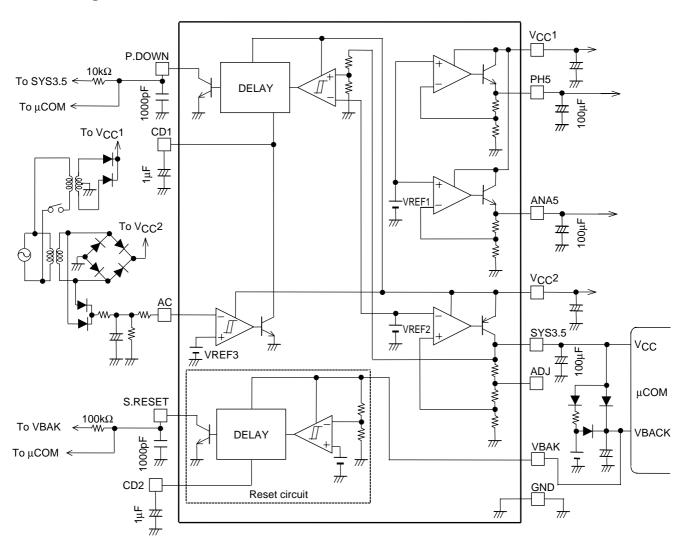




Pin Assignment

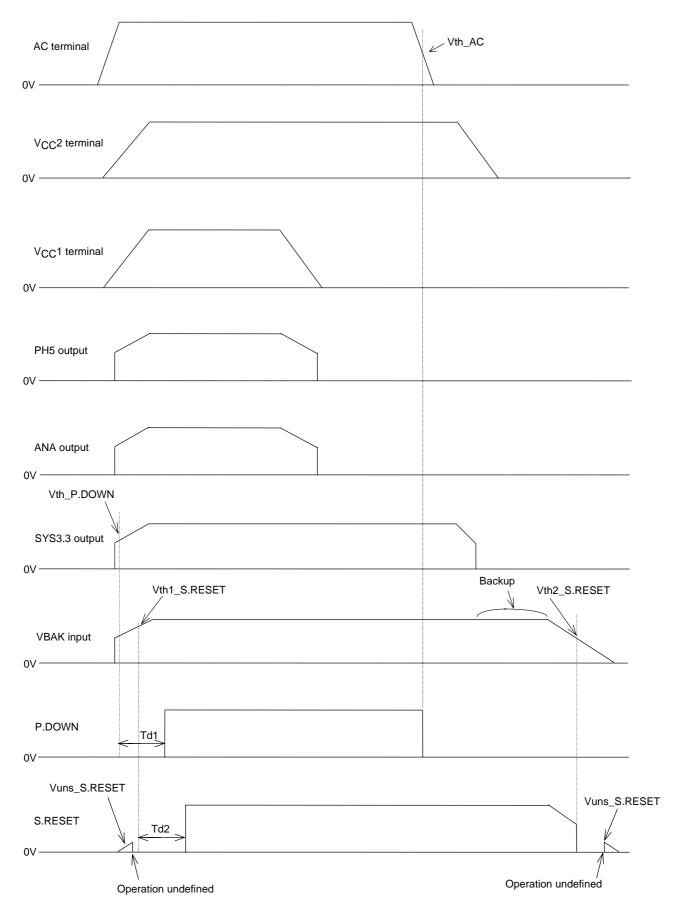


Block Diagram



Note) Use capacitors that develop less capacity fluctuation due to temperature.

Timing Chart



Note: S.RESET output is in the operation-undefined condition.

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