Ordering number:ENN3222A

Monolithic Linear IC

LA5601

Low Saturation Regulator with Reset

Overview

The LA5601 is a voltage regulator with a low-voltage detector and reset controller for use in microprocessor-based systems. It generates a reset signal for low power supply voltage. It also features a low 0.25V (typ.) saturation voltage for reduced power dissipation and power supply size. Applications include microprocessor-controlled consumer electronic equipment such as CD players, tuners and receivers, and preamplifiers.

Functions

- Low saturation regulator with 250mA and 5.2V output.
- Power supply reset generator function.
- Supports on-off control of 5.2V using equipped enable pin (high active).
- Built-in Darlington driver (120mA).
- Built-in auxiliary regulator (5.2V, 250mA).

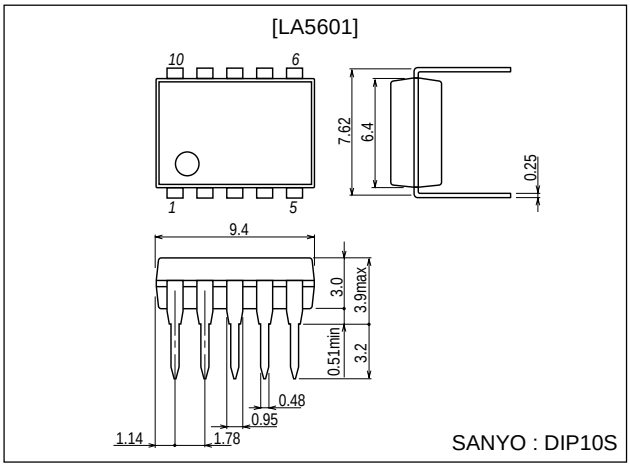
Features

- Low minimum input-output voltage difference (0.3V typ).
- Supports setting of reset output delay time using external capacitor.
- Built-in fold-back current limiting circuit and excessive heat protection circuit.
- Reset output using active pull-up for simpler noise reduction and use with internal pull-down logic circuits.
- Error amplifier noise filter pin.
- Auxiliary regulator with reverse current protection.

Package Dimensions

unit:mm

3098B-DIP10S



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Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN} max		15	V
Enable pin voltage	V_{EN} max		V_{IN} max	V
Reset output pin voltage	$V_{\overline{RES}}$ max		15	V
Driver output voltage	V_{OD} max		15	V
Driver input voltage	V_{ID} max		15	V
Allowable power dissipation	Pd max		1	W
Operating temperature	Topr		–30 to +80	˚C
Storage temperature	Tstg		–55 to +150	˚C

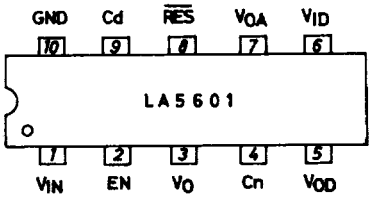
Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN}		5.9 to 14	V
Output current	I_{OUT}		0 to 250	mA
H-level reset output current	$I_{\overline{ORH}}$		0 to 200	µA
L-level reset output current	$I_{\overline{ORL}}$		0 to 2	mA
Auxiliary regulator output current	I_{OA}		0 to 10	mA
Driver output voltage	V_{OD} max		14	V
L-level driver output current	I_{ODL} max		120	mA
H-level driver input voltage	V_{IDH}	I_{ODL}=120mA	3 to 14	V
L-level driver input voltage	V_{IDL}	I_{ODL}≤100µA	–0.3 to +0.3	V

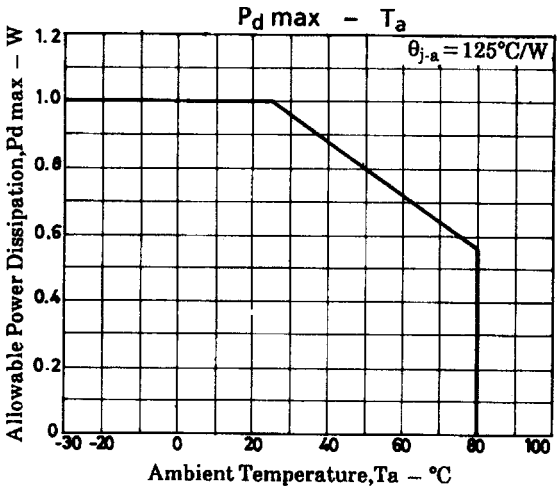
Operating Characteristics at Tj = 25˚C, V_{IN}=6V, I_{OUT}=200mA, See specified Test Circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Main regulator : Output ON-state, V_{EN}='H' or open]						
Output voltage	V_O		5.0	5.2	5.4	V
Dropout voltage	V_{DROP}	I_{OUT}=250mA		0.25	0.5	V
Line regulation	$\Delta V_{OLN}1$	5.5V≤V_{IN}≤14V		30	80	mV
	$\Delta V_{OLN}2$	6V≤V_{IN}≤14V		20	40	mV
Load regulation	$\Delta V_{OLD}1$	5mA≤I_{OUT}≤250mA		40	100	mV
	$\Delta V_{OLD}2$	5mA≤I_{OUT}≤100mA		14	50	mV
Peak output current	I_{OP}		250	500		mA
Output short current	I_{OSC}			80	300	mA
Current drain	I_Q1	I_{OUT}=0		2.2	6	mA
	I_Q2			10	30	mA
Output noise voltage	V_{NO}	10Hz≤f≤100kHz		70		µVrms
Temperature coefficient of output voltage	$\Delta V_O/\Delta Tj$	Tj=25 to 80°C		–0.7		mV/˚C
Ripple rejection	Rrej	f=120Hz, 7V≤V_{IN}≤13V		74		dB
Output ON-state control voltage	V_{ENH}	Main regulator, driver ON	2.6		V_{IN}	V
[Main regulator : Output OFF-state, V_{EN}='L']						
L-level output voltage	$V_{O\ OFF}$	V_{EN}=0		50	200	mV
Quiescent current	$I_{Q\ OFF}$	V_{EN}=0		1.5	4	mA
Output OFF-state control voltage	V_{ENL}	Main regulator, driver OFF			1.0	V
[Reset circuit]						
H-level reset output voltage	$V_{\overline{ORH}}$	$I_{\overline{ORH}}$=200µA	4.97	5.17	5.37	V
L-level reset output voltage	$V_{\overline{ORL}}$	$I_{\overline{ORL}}$=2mA, V_{IN}=3.7V		90	200	mV
Reset threshold voltage	V_{RT}	I_{OUT}=5mA	3.7	3.9	4.1	V
Reset hysteresis voltage	Vhys	I_{OUT}=5mA	50	150	300	mV
Reset output delay time	t_d	Cd=0.1µF	7.5	10	12.5	ms
[Auxiliary regulator]						
Output voltage	V_{OA}	I_{OA}=5mA	3.2	3.4	3.6	V
Line regulation	$\Delta V_{OA\ LN}$	6V≤V_{IN}≤14V, I_{OA}=5mA		15	40	mV
Load regulation	$\Delta V_{OA\ LD}$	2mA≤I_{OA}≤10mA		130	200	mV
Output short current	I_{OASC}		10	30		mA
Output pin leakage current	$I_{OA\ LEAK}$	V_{IN}=0, V_{OA}=6V			2	µA
[Darlington driver]						
L-level driver output voltage	$V_{ODL}1$	I_{ODL}=80mA, V_{ID}=3V		1.1	1.6	V
	$V_{ODL}2$	I_{ODL}=120mA, V_{ID}=3V		1.2	1.8	V
H-level driver input current	I_{IDH}	I_{ODL}=120mA, V_{ID}=3V		0.4	1	mA
Output pin leakage current	I_{ODH}	V_{IH}=14V, V_{OD}=14V, V_{ID}=0.3V			50	µA

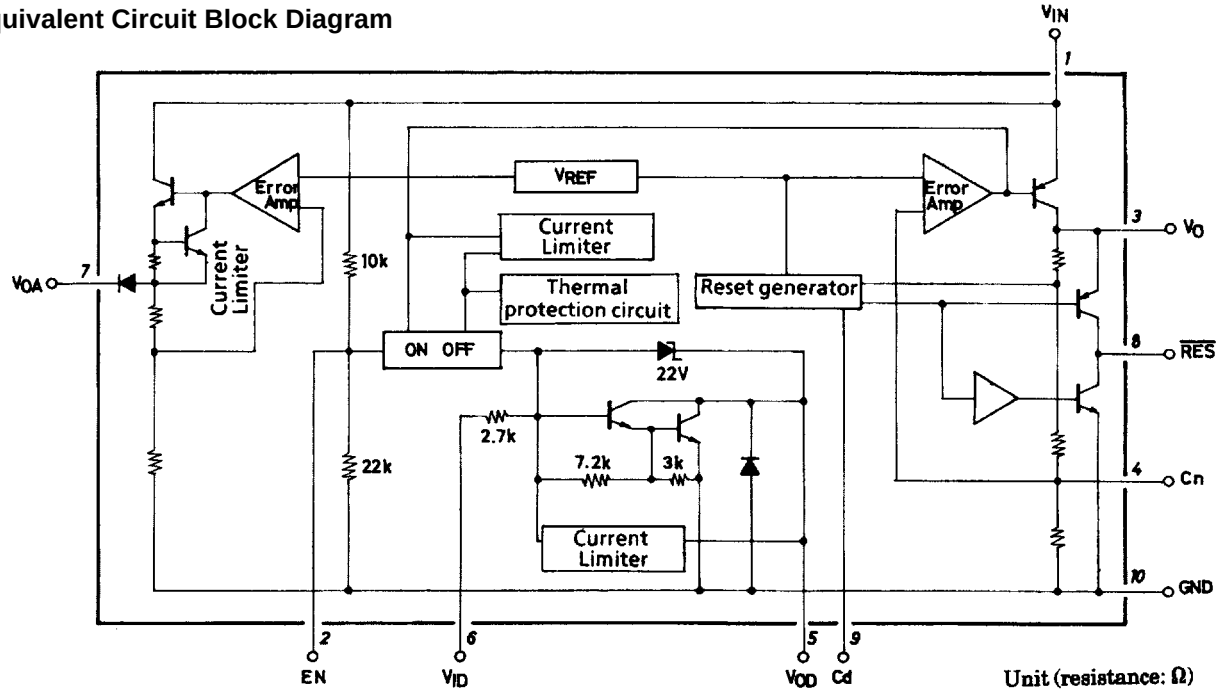
Pin Assignment



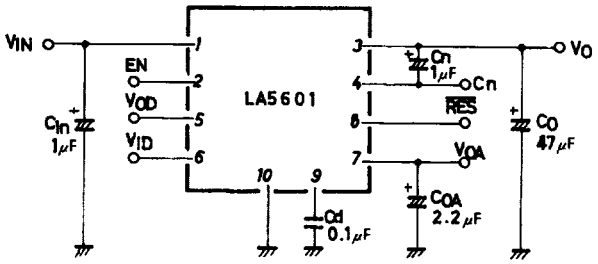
Top view



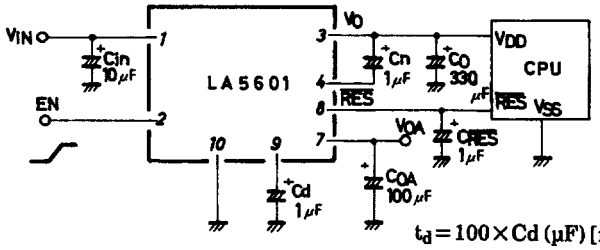
Equivalent Circuit Block Diagram



Specified Test Circuit



Sample Application Circuit 1



Note) 1. Capacitors C_n and C_{RES} are only required if problems are experienced with noise from external sources.

2. If capacitor C_n is present, ensure that C_o is at least more than one-third of the value of C_{in} in order to prevent output noise at power-down due to capacitor discharge timing.

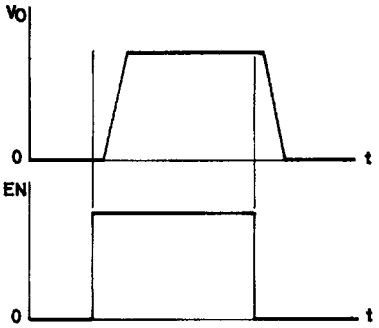
3. The minimum recommended value of output capacitor C_o is 47μF.

4. Use low temperature coefficient capacitor for the delay time capacitor C_d.

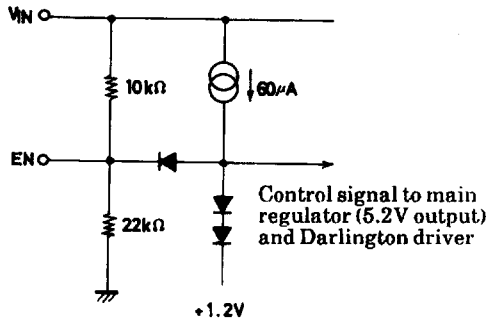
Function Table

V_{EN}	V_O	Driver
L	L	OFF
H	H	ON

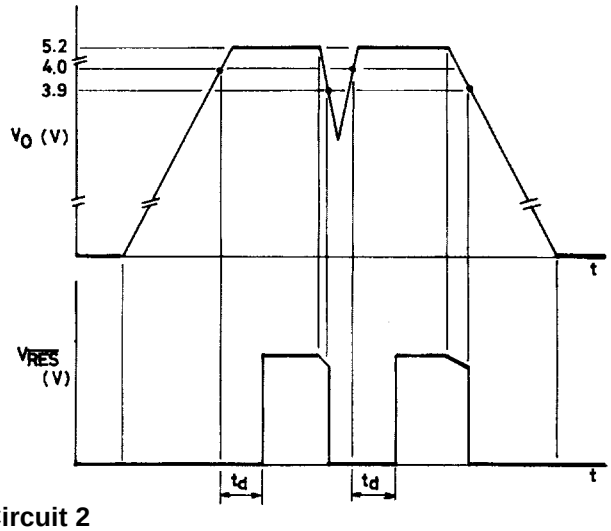
V_{EN}='H' or open.



Enable Circuit

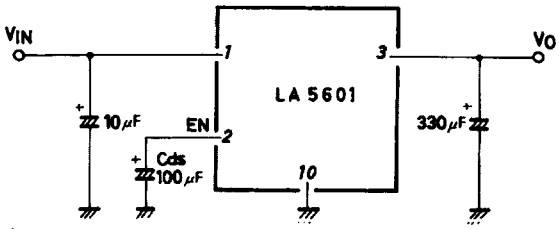


Reset Operation



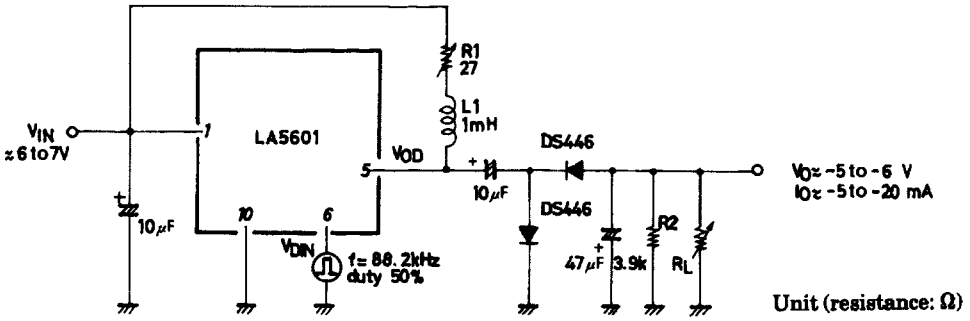
Sample Application Circuit 2

(Delay start regulator)



Sample Application Circuit 3

(Positive-to-negative DC converter)

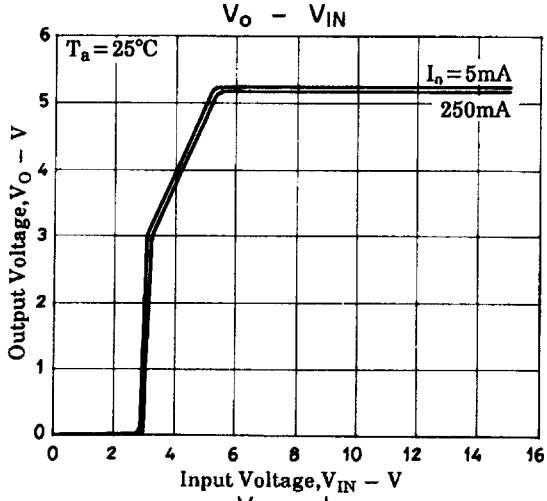


Note) 1. The output voltage can be fine-trimmed by adjusting R1. To protect the output transistor against overvoltage, ensure that either R1 is non zero or use a low-Q coil for L1.

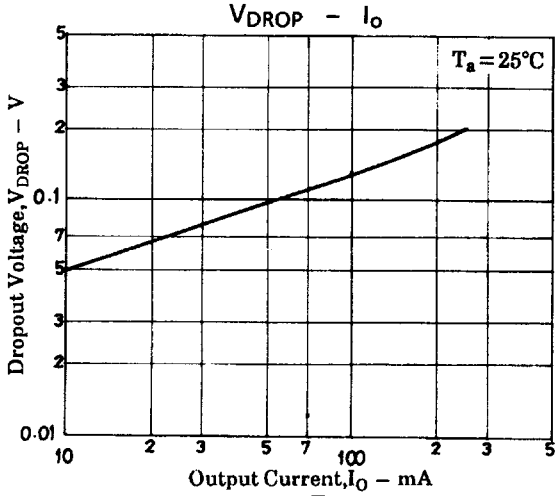
2. A load must always be present on power-up. To safeguard against excessive output voltages that occur when the circuit is powered up without a load, a dummy load resistor is recommended. This is shown on the circuit as R2.

3. Select V_{IN}, R1 and L1 so that V_{OD}<14V, and I_{ODL}<120mA. The component values shown reguire that V_{IN} never exceeds 9V.

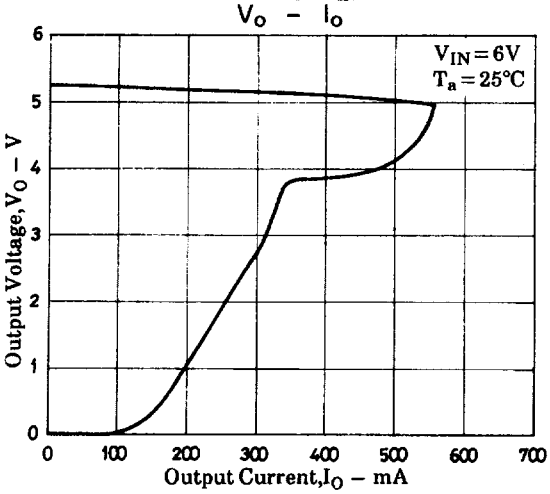
$V_O - V_{IN}$



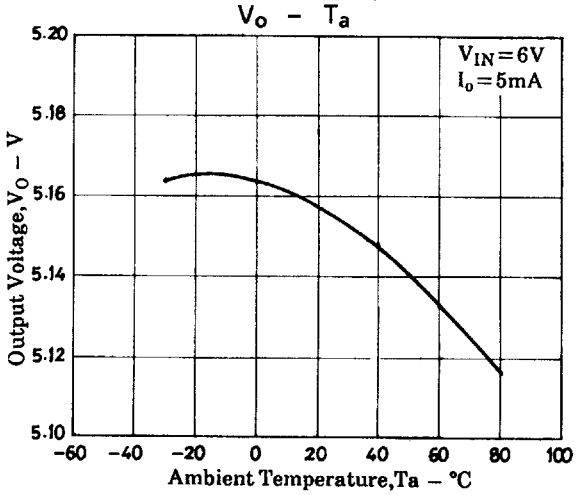
$V_{DROP} - I_O$



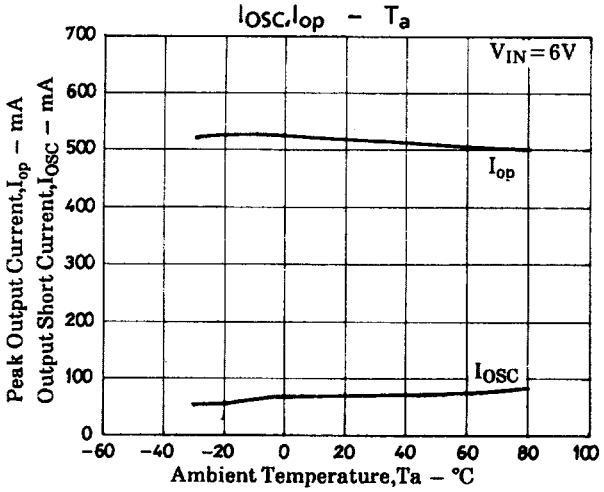
$V_O - I_O$



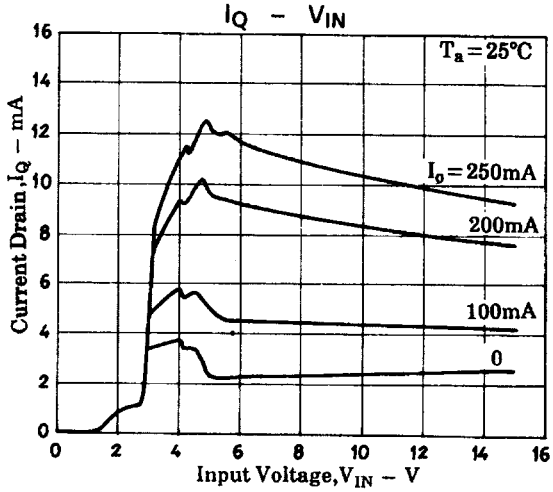
$V_O - T_a$



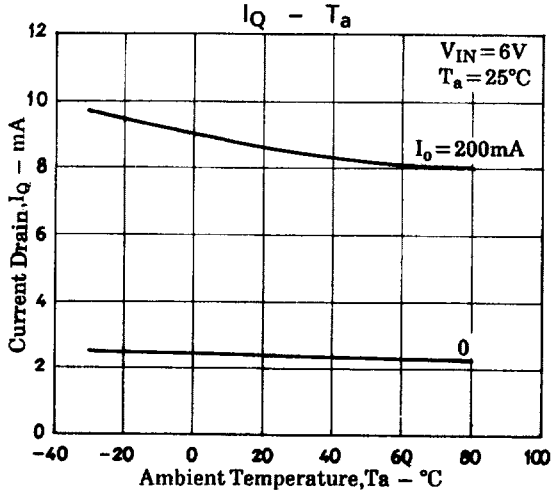
$I_{OSC}, I_{op} - T_a$



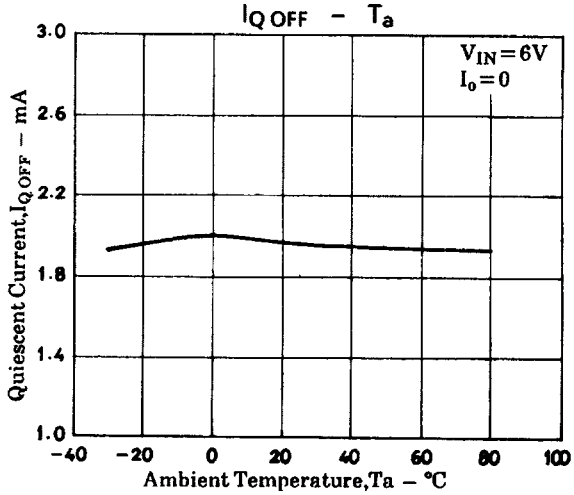
$I_Q - V_{IN}$



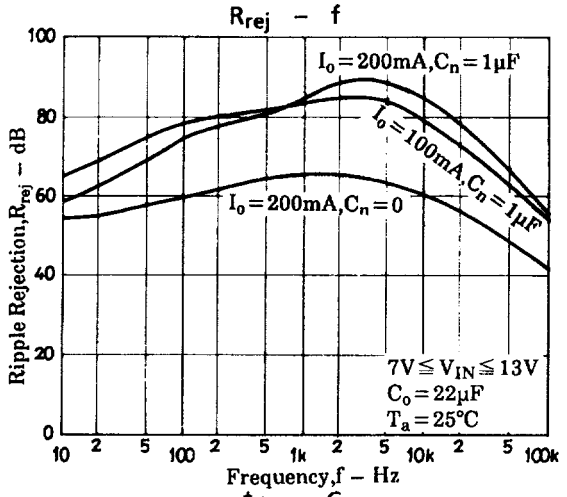
$I_Q - T_a$



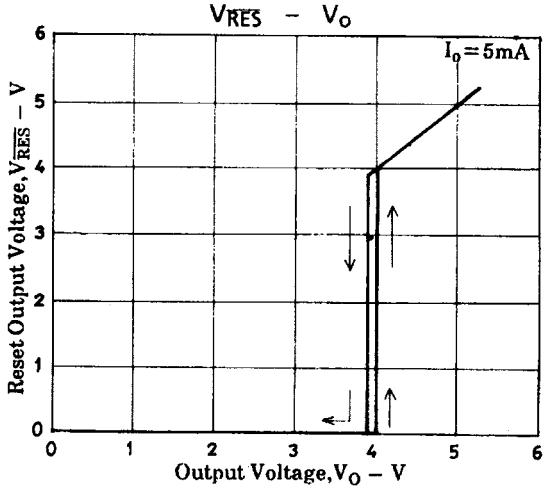
$I_{Q\,OFF} - T_a$



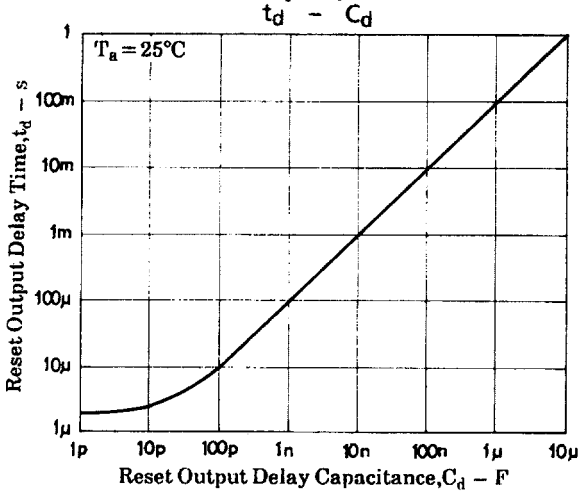
R_{rej} – f



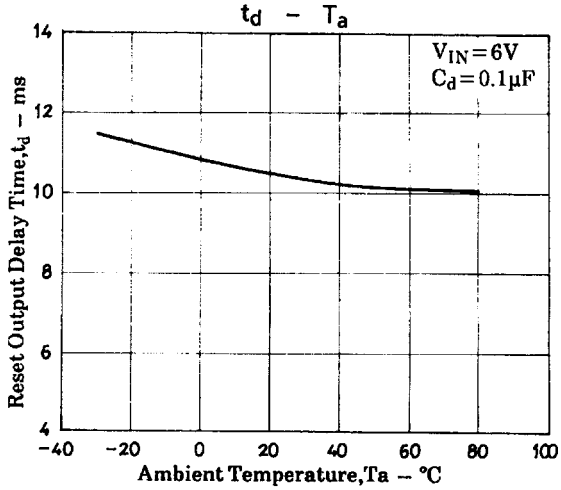
$V_{\overline{RES}}$ – V_O



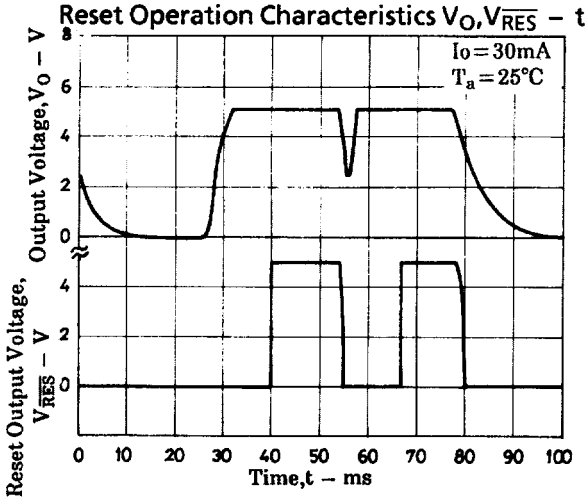
t_d – C_d



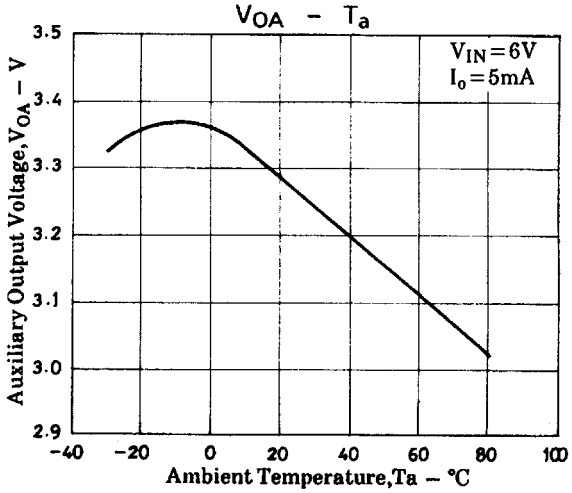
t_d – T_a



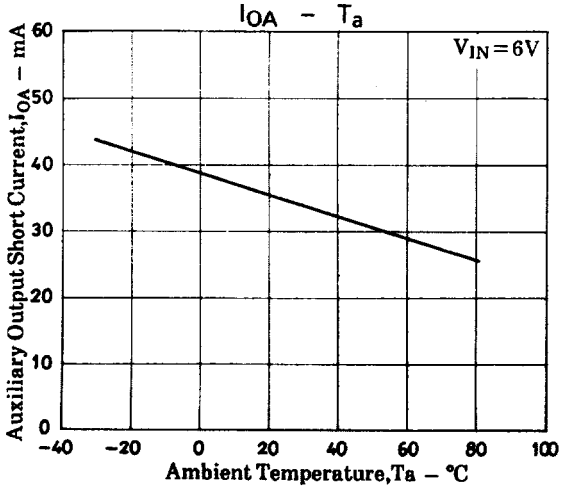
Reset Operation Characteristics V_O, $V_{\overline{RES}}$ – t



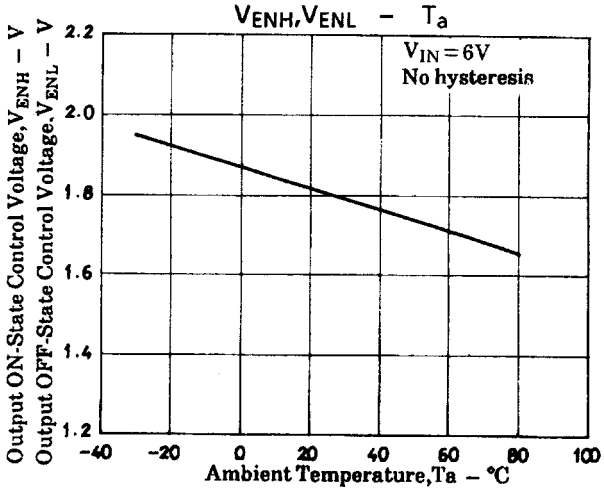
V_{OA} – T_a



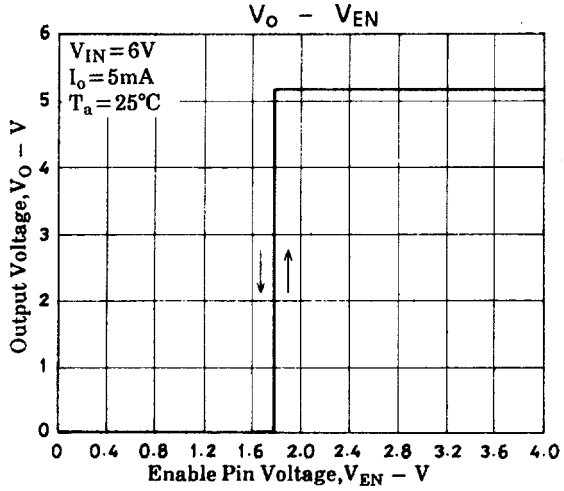
I_{OA} – T_a



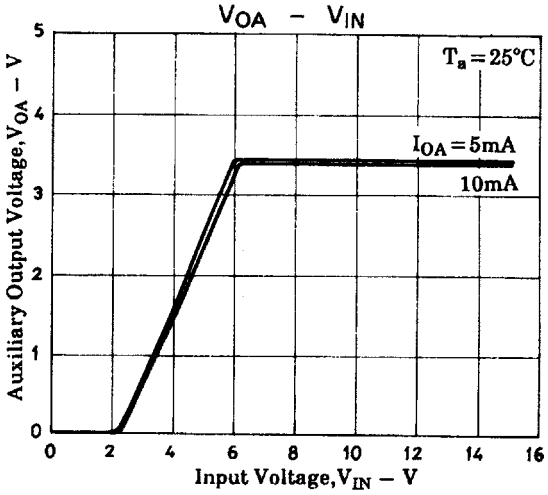
V_{ENH}, V_{ENL} – T_a



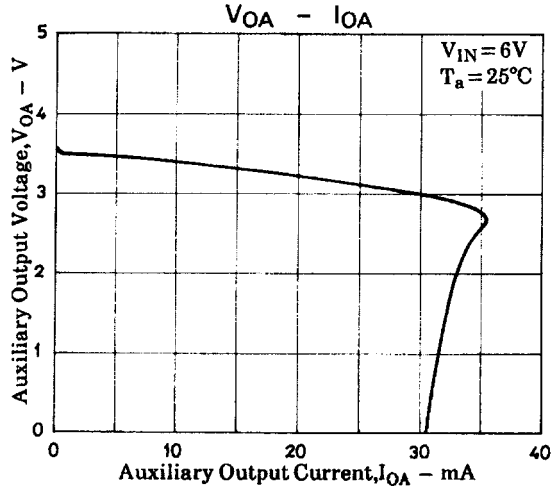
$V_O - V_{EN}$



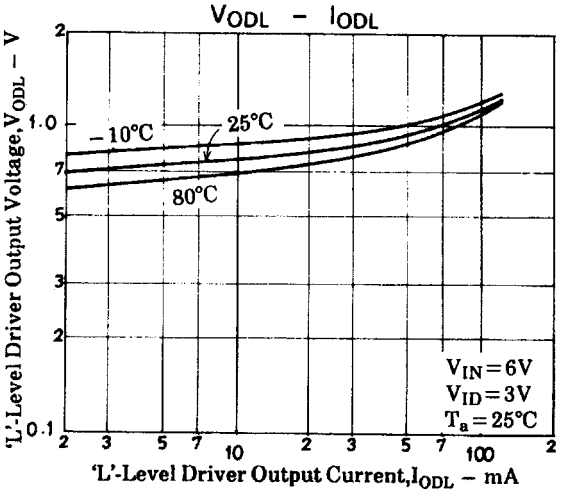
$V_{OA} - V_{IN}$



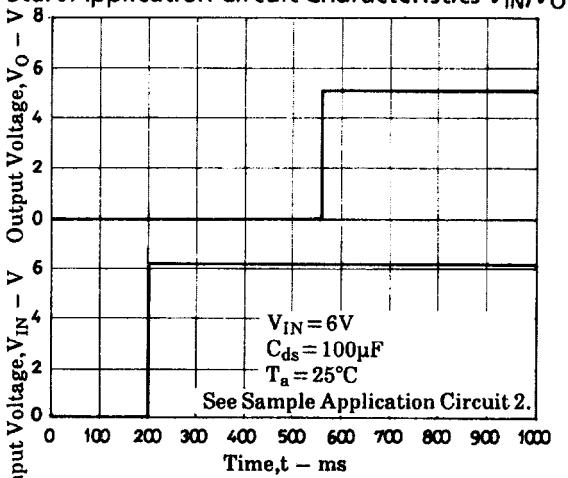
$V_{OA} - I_{OA}$



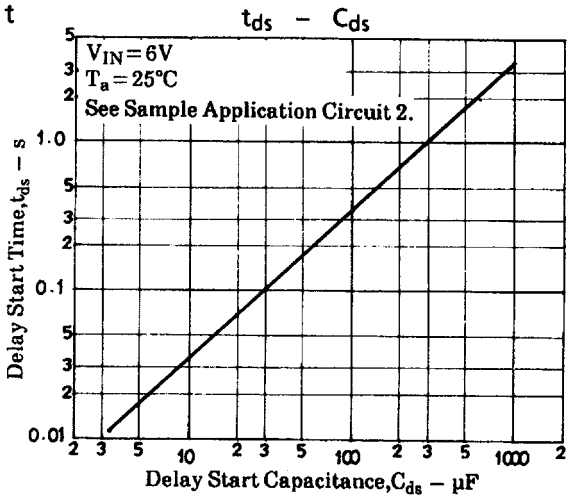
$V_{ODL} - I_{ODL}$



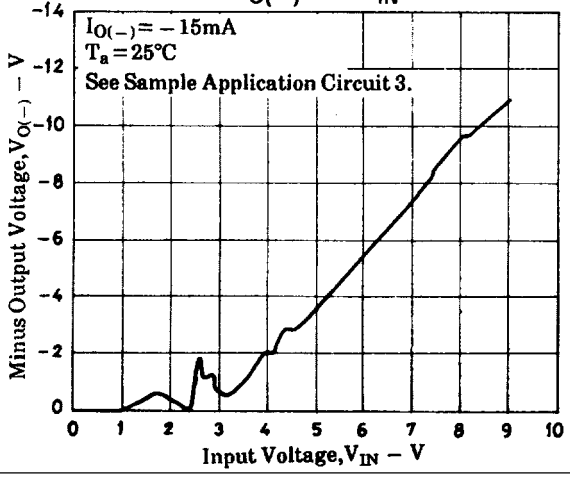
Delay Start Application Circuit Characteristics $V_{IN}, V_O - t$



$t_{ds} - C_{ds}$



$V_{O(-)} - V_{IN}$



$V_{O(-)} - I_{O(-)}$