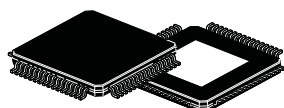


## Automotive engine management control IC for small engines



TQFP64 exposed pad down

GADG1606171506PS

### Features



- AEC-Q100 qualified
- Supply voltage from 6 V to 18 V
  - Basic functionality guaranteed down to 3.9 V
- 5 V regulator up to 300 mA with thermal shutdown protection in current limitation condition
- 5 V tracking regulator up to 40 mA and short to battery protection
- 5 V standby regulator up to 2.5 mA
- 2 channels injectors drivers
  - Parallel and serial driving
  - Output internally clamped to 60 V
  - Minimum overcurrent at 2.8 A
  - Ron 0.6  $\Omega$  worst case (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- 3 relay drivers
  - 2 with parallel and serial driving, 1 with serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 1 A
  - Ron 1.5  $\Omega$  worst case (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- Tachometer driver
  - Parallel and serial driving
  - Minimum guaranteed output current 25 mA
  - Ron 5  $\Omega$  worst case (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- Current limited low side driver (LSD)
  - Serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 1 A (2 A during in-rush)
  - Ron 1.5  $\Omega$  worst case (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- Stepper motor driver
  - Parallel driving
  - Minimum guaranteed output current 500 mA - full step
  - Ron 2.6  $\Omega$  worst case on the diagonal (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- O2 sensor heater
  - Parallel and serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 3 A
  - Ron 0.5  $\Omega$  worst case (at  $T_j = 150\text{ }^{\circ}\text{C}$ )
- Protected high side driver
  - 100 mA min. current limitation threshold
- Full diagnosis by SPI
  - Injector driver: OL, STG, OC
  - Relay and current limited LSD drivers: OL, STG, OC

#### Product status link

[L9177A](#)

#### Product summary

| Order code | Package                             | Packing       |
|------------|-------------------------------------|---------------|
| L9177A     | TQFP64 (10x10 mm), exposed pad down | Tray          |
| L9177ATR   | (7.5x7.5 mm)                        | Tape and reel |

- O2 sensor heater: OL, STG, OC
- Tachometer: OL, STG, OC
- Stepper motor driver: OL, STG, STB, OC
- general diagnostic: over-temperature
- Protection for STB, STG (for stepper motor drivers and tracking regulator)
- Self configuring variable reluctance sensor interface
- K-line transceiver
- Microcontroller reset logic
- Small Factor form package TQFP64 10 x 10 mm exposed pad down

## Description

L9177A is a device realized in ST BCD proprietary technology, able to provide the full set of power supplies and signal preprocessing peripherals needed to control a 2 Cylinder internal combustion Engine for Low End Application (e.g. small motorcycle, K-car, nautical engines, etc.).

L9177A integrates a 5 V 300 mA main voltage regulator, a 5 V 40 mA tracking regulator for sensor supply and a 2.5 mA 5 V standby regulator.

The two channels injector drivers, the O2 sensor heater and two relay drivers can be controlled both with parallel input and with SPI interface. One additional relay driver and the current limited low side driver are controlled by SPI. The stepper motor driver is designed for a double winding coil motor, used for engine idle speed control.

Low side drivers implement SR control to minimize emission.

A protected 50 mA high side driver is provided.

A Variable Reluctance Sensor interface allows the connection to a commercial magnetic pick-up, allowing the indirect measurement of internal combustion engine crank angle. A K-line (standard ISO-9141 compatible) is provided as data communication interface.

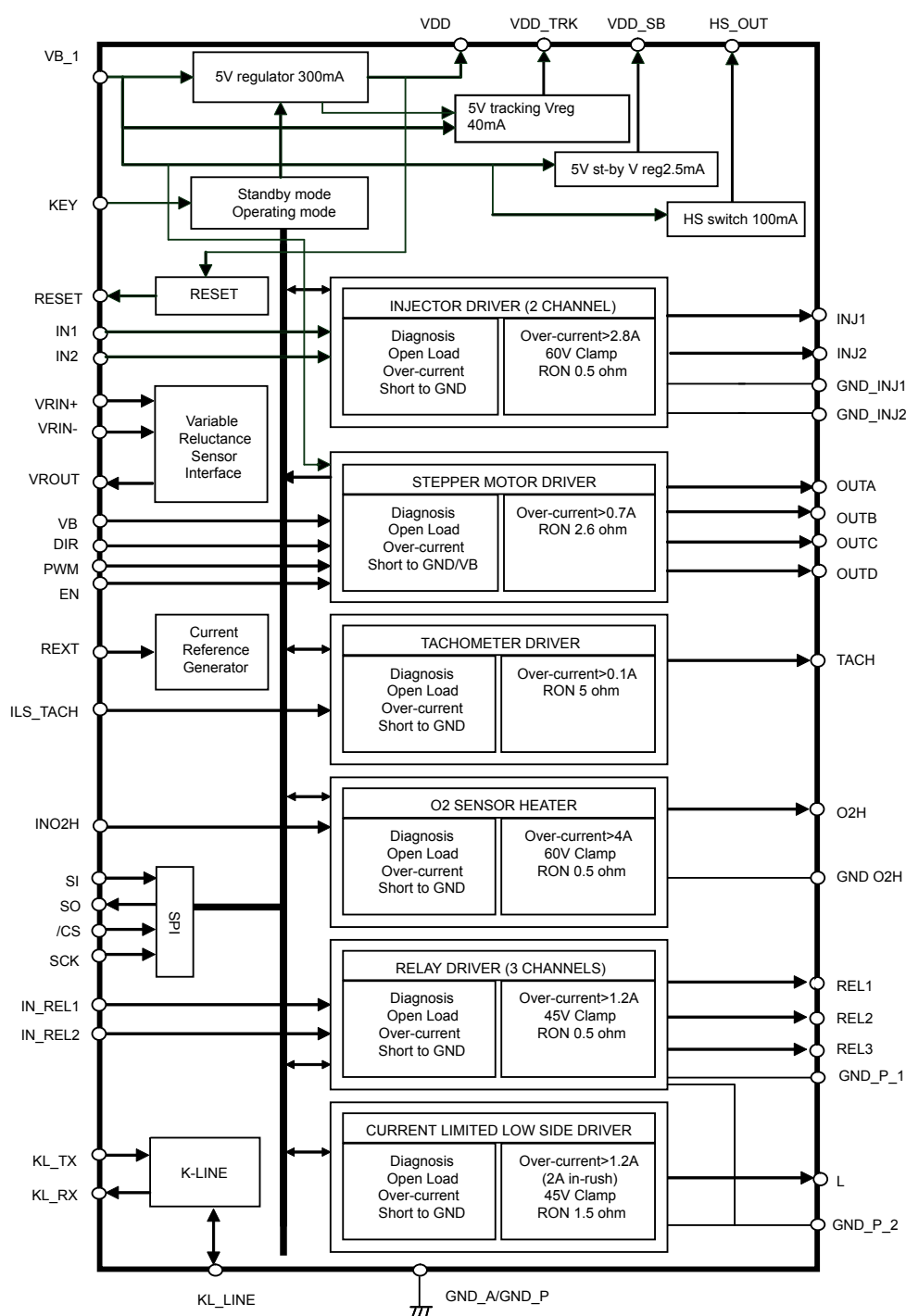
All functionalities are fully protected and provide complete diagnostics via a 24-bit SPI interface. An overall protection against over temperature is provided as well.

The device is available in TQFP64 10x10 mm package with exposed pad for power dissipation optimization.

# 1 Block diagram and pin description

## 1.1 Block diagram

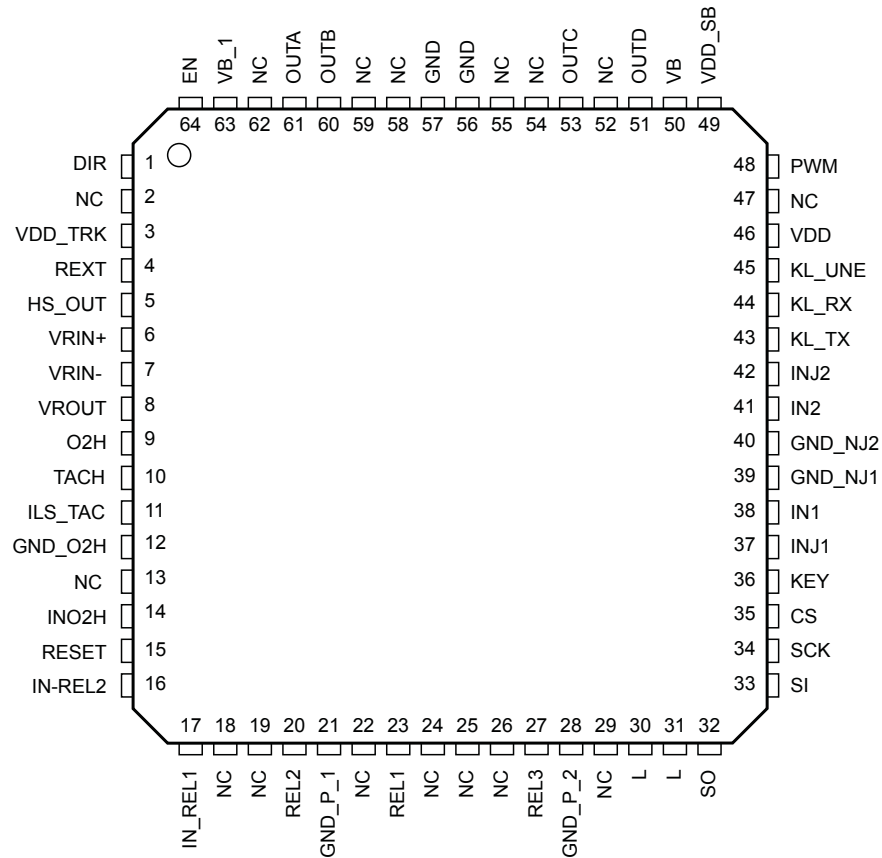
Figure 1. Block diagram



GAPGPS00585

## 1.2 Pin description

**Figure 2. Pin connection (top view)**



GAPG0403151617PS

**Table 1. Pin function**

| Pin # | Pin name | Description                                       | I/O type | Class  |
|-------|----------|---------------------------------------------------|----------|--------|
| 1     | DIR      | Logic input to set stepper motor direction        | I        | SIGNAL |
| 2     | NC       | Not connected                                     | -        | -      |
| 3     | VDD_TRK  | Tracking voltage regulator output                 | O        | PWR    |
| 4     | REXT     | External resistor for precision current reference | I        | SIGNAL |
| 5     | HS_OUT   | High side switch output                           | O        | PWR    |
| 6     | VRIN+    | VRS positive differential input                   | I        | SIGNAL |
| 7     | VRIN-    | VRS negative differential input                   | I        | SIGNAL |
| 8     | VROUT    | VRS output                                        | O        | SIGNAL |
| 9     | O2H      | O2 sensor heater output                           | O        | PWR    |
| 10    | TACH     | Tachometer driver output                          | O        | PWR    |
| 11    | ILS_TACH | Tachometer driver input                           | I        | SIGNAL |
| 12    | GND_O2H  | O2 sensor heater ground                           | GND      | PWR    |
| 13    | NC       | Not connected                                     | -        | -      |
| 14    | INO2H    | O2 sensor heater input                            | I        | SIGNAL |

| Pin # | Pin name | Description                            | I/O type | Class  |
|-------|----------|----------------------------------------|----------|--------|
| 15    | RESET    | Reset signal to the micro              | O        | SIGNAL |
| 16    | IN_REL2  | Relay 2 parallel control input         | I        | SIGNAL |
| 17    | IN_REL1  | Relay 1 parallel control input         | I        | SIGNAL |
| 18    | NC       | Not connected                          | -        | -      |
| 19    | NC       | Not connected                          | -        | -      |
| 20    | REL2     | Relay 2 driver output                  | O        | PWR    |
| 21    | GND_P_1  | Power ground relay 1-2                 | O        | PWR    |
| 22    | NC       | Not connected                          | -        | -      |
| 23    | REL1     | Relay 1 driver output                  | O        | PWR    |
| 24    | NC       | Not connected                          | -        | -      |
| 25    | NC       | Not connected                          | -        | -      |
| 26    | NC       | Not connected                          | -        | -      |
| 27    | REL3     | Relay 3 driver output                  | O        | PWR    |
| 28    | GND_P_2  | Power ground for current limited LSD   | GND      | PWR    |
| 29    | NC       | Not connected                          | -        | -      |
| 30    | L        | Current limited LSD driver output      | O        | PWR    |
| 31    | L        | Current limited LSD driver output      | O        | PWR    |
| 32    | SO       | SPI data out                           | O        | SIGNAL |
| 33    | SI       | SPI data in                            | I        | SIGNAL |
| 34    | SCK      | SPI serial clock                       | I        | SIGNAL |
| 35    | CS       | SPI chip select                        | I        | SIGNAL |
| 36    | KEY      | Key signal                             | I        | SIGNAL |
| 37    | INJ1     | Injector 1 driver power output         | O        | PWR    |
| 38    | IN1      | Injector 1 driver input command        | I        | SIGNAL |
| 39    | GND_INJ1 | Injector 1 ground                      | GND      | PWR    |
| 40    | GND_INJ2 | Injector 2 ground                      | GND      | PWR    |
| 41    | IN2      | Injector 2 driver input command        | I        | SIGNAL |
| 42    | INJ2     | Injector 2 driver power output         | O        | PWR    |
| 43    | KL_TX    | K-Line TX digital IN                   | I        | SIGNAL |
| 44    | KL_RX    | K-Line RX digital OUT                  | O        | SIGNAL |
| 45    | KL_LINE  | K-Line                                 | I/O      | PWR    |
| 46    | VDD      | 5 V voltage regulator output           | O        | PWR    |
| 47    | NC       | Not connected                          | -        | -      |
| 48    | PWM      | Logic Input to set Stepper Motor Speed | I        | SIGNAL |
| 49    | VDD_SB   | 5 V standby voltage regulator output   | O        | PWR    |
| 50    | VB       | Battery line to bridge 2               | I        | PWR    |
| 51    | OUTD     | Output bridge 2                        | O        | PWR    |
| 52    | NC       | Not connected                          | -        | -      |
| 53    | OUTC     | Output bridge 2                        | O        | PWR    |
| 54    | NC       | Not connected                          | -        | -      |

| Pin # | Pin name | Description                         | I/O type | Class  |
|-------|----------|-------------------------------------|----------|--------|
| 55    | NC       | Not connected                       | -        | -      |
| 56    | GND      | Analog and power ground             | GND      | PWR    |
| 57    | GND      | Analog and power ground             | GND      | PWR    |
| 58    | NC       | Not connected                       | -        | -      |
| 59    | NC       | Not connected                       | -        | -      |
| 60    | OUTB     | Output bridge 1                     | O        | PWR    |
| 61    | OUTA     | Output bridge 1                     | O        | PWR    |
| 62    | NC       | Not connected                       | -        | -      |
| 63    | VB_1     | Battery line to bridge1             | I        | PWR    |
| 64    | EN       | Logic input to enable stepper motor | I        | SIGNAL |
| -     | Pad      | Exposed pad                         | GND      | PWR    |

## 2 Electrical specifications

### 2.1 Operating range

The device may not operate properly if maximum operating conditions are exceeded.

**Table 2. Operating conditions**

| Parameter               | Value                  | Unit |
|-------------------------|------------------------|------|
| VB, VB_1 supply voltage | 6 to 18 <sup>(1)</sup> | V    |
| I/O logic               | 0 to VDD               | V    |
| Stepper motor outputs   | -0.3 to VB, VB_1       | V    |
| Low side outputs        | -0.3 to clamp voltage  | V    |

1. See [Section 2.1.1](#).

#### 2.1.1 Supply voltage

- Below 3.9 V the device is in a safety state (internal circuitries are on but all the outputs are off).
- From 3.9 V to 5.5 V (Functionalities during Crank phase):
  - Reset function;  $V_{DD} > 3.3$  V (rds-on state)  $I_{VDD} = 100$  mA;  $3.3$  V  $< V_{DD\_TRK} < V_{DD}$  (rds-on state);
  - Low-sides, K-Line, H-Bridge OFF if Reset = 0; SPI not available, internal registers resetted if Reset = 0;
  - All Diagnosis disabled if Reset = 0; VRS function limited ( $V_{diff\ max} = 1000$  mV)
- From 5.5 V to 6 V (low battery):
  - All the functions are granted with the following degraded parameters;  $V_{DD} > 4.510$  V; Tracking error  $< 100$  mV ( $I_{load} = 40$  mA, rds-on state).
- From 6 V to 18 V: normal operating range
- From 18 V to  $V_{B\_off}$ :
  - All the functions are granted with increased power dissipation and no reset is asserted during transient.
- From  $V_{B\_off}$  to 40 V (internal circuitries are on but all the outputs are off):
  - The device is on and in a safety state.

### 2.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

**Table 3. Absolute maximum ratings**

| Parameter                                   | Condition   | Min  | Max           | Unit |
|---------------------------------------------|-------------|------|---------------|------|
| DC supply voltage                           | pin VB/VB_1 | -0.3 | 40            | V    |
| I/O low voltage pins <sup>(1)</sup>         | -           | -0.3 | 7             | V    |
| I/O low voltage digital pins <sup>(2)</sup> | -           | -0.3 | VDD+0.3       | V    |
| I/O power pins voltage range <sup>(3)</sup> | -           | -0.3 | Clamp voltage | V    |
| TACH pin                                    | -           | -0.3 | 40            | V    |
| OUTA-D                                      | -           | -0.3 | VB +0.3       | V    |

| Parameter                                                                                                              | Condition                                                                                                                                                                     | Min  | Max       | Unit |
|------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------|------|
| KEY pin                                                                                                                | To be protected with R <sub>key</sub> to limit sourced/<br>sunked current to $\pm 5$ mA in dc conditions<br>and $\pm 20$ mA during transients<br>(ISO-pulses on battery line) | -0.3 | 10        | V    |
| VRIN- / VRIN+                                                                                                          | Max current [20 mA] to be limited with<br>external resistors                                                                                                                  | -0.3 | VDD + 0.3 | V    |
| VDD_TRK pin                                                                                                            | -                                                                                                                                                                             | -2   | 40        | V    |
| KL_LINE pin                                                                                                            | -                                                                                                                                                                             | -16  | 40        | V    |
| Maximum voltage shift between GND pins                                                                                 | PIN GND, GND_O2H, GND_P_1,2,<br>GND_INJ1,2, GNDA, GNDP                                                                                                                        | -0.3 | 0.3       | V    |
| I/O power pins <sup>(3)</sup> maximum energy (single pulse,<br>max. current)                                           | Injector drivers                                                                                                                                                              | -    | 50        | mJ   |
|                                                                                                                        | O2 sensor heater                                                                                                                                                              | -    | 60        | mJ   |
|                                                                                                                        | Relay/current limited drivers                                                                                                                                                 | -    | 25        | mJ   |
| I/O power pins <sup>(3)</sup> maximum energy (continuous<br>pulse, max. current, 36 million pulses with T = 100<br>ms) | Injector drivers                                                                                                                                                              | -    | 18        | mJ   |
|                                                                                                                        | O2 sensor heater                                                                                                                                                              | -    | 22        | mJ   |
|                                                                                                                        | Relay/current limited drivers                                                                                                                                                 | -    | 8         | mJ   |
| Reverse current through O2H output without supply<br>voltage <sup>(4)</sup>                                            | Static (room temperature, max reverse<br>diode voltage 1.5 V)                                                                                                                 | -    | 2.5       | A    |
|                                                                                                                        | Dynamic (guarantee by iso-pulse test<br>immunity on application board)                                                                                                        | -    | -         |      |
| Reverse current through INJx outputs without supply<br>voltage <sup>(4)</sup>                                          | Static (room temperature, max reverse<br>diode voltage 1.5 V)                                                                                                                 | -    | 2.2       | A    |
|                                                                                                                        | Dynamic (guarantee by iso-pulse test<br>immunity on application board)                                                                                                        | -    | -         |      |
| Reverse current through L output without supply<br>voltage <sup>(4)</sup>                                              | Static (room temperature, max reverse<br>diode voltage 1.5 V)                                                                                                                 | -    | 1.2       | A    |
|                                                                                                                        | Dynamic (guarantee by iso-pulse test<br>immunity on application board)                                                                                                        | -    | -         |      |
| Reverse current through RLYx outputs without<br>supply voltage <sup>(4)</sup>                                          | Static (room temperature, max reverse<br>diode voltage 1.5 V)                                                                                                                 | -    | 1.5       | A    |
|                                                                                                                        | Dynamic (guarantee by iso-pulse test<br>immunity on application board)                                                                                                        | -    | -         |      |
| Reverse current through TACH output without supply<br>voltage <sup>(4)</sup>                                           | Static (room temperature, max reverse<br>diode voltage 1.5 V)                                                                                                                 | -    | 0.5       | A    |
|                                                                                                                        | Dynamic (guarantee by iso-pulse test<br>immunity on application board)                                                                                                        | -    | -         |      |

1. Pins are VDD, VDD\_SB, REXT, DIR

2. Pins are CS, SCK, SI, SO, VROUT, RESET, PWM, EN, INO2H, ILS\_TACH, IN, KL\_TX, KL\_RX

3. Pins are O2H, L, INJ1-2, REL1-2-3

4. Reverse battery connection, parameter not tested for info only

**Table 4. ESD protection**

| Item                       | Condition                                | Min           | Max         | Unit |
|----------------------------|------------------------------------------|---------------|-------------|------|
| All pins <sup>(1)(2)</sup> | HBM                                      | -2            | 2           | kV   |
| All pins                   | MM                                       | -200          | 200         | V    |
| All pins                   | CDM (values for corner pins in brackets) | -500 / (-750) | 500 / (750) | V    |

| Item                             | Condition | Min | Max | Unit |
|----------------------------------|-----------|-----|-----|------|
| Pins to connector <sup>(3)</sup> | HBM       | -4  | 4   | kV   |

1. OUTA-D, TACH, O2H, L, INJ1-2, REL1-2-3 vs. GNDP2, GNDO2: -1.5 / 1.5 kV
2. OUTA-D, TACH, O2H, L, INJ1-2, REL1-2-3 vs. GNDP1: -1 / 1 kV
3. Pins are OUTA-D, TACH, O2H, L, INJ1-2, KEY, REL1-2-3, VB, KL\_LINE, VDD\_TRK all GND connected together. The device is AEC-Q100 compliant.

## 2.3 Latch-up test

According to JEDEC 78 class 2 level A.

## 2.4 Temperature ranges and thermal data

**Table 5. Temperature ranges and thermal data**

| Symbol                 | Parameter                                             | Min | Max | Unit |
|------------------------|-------------------------------------------------------|-----|-----|------|
| T <sub>amb</sub>       | Operating temperature (ECU environment)               | -40 | 125 | °C   |
| T <sub>j</sub>         | Operating junction temperature                        | -40 | 150 | °C   |
| T <sub>stg</sub>       | Storage temperature                                   | -40 | 150 | °C   |
| T <sub>ot</sub>        | Thermal shut-down temperature                         | 155 | 200 | °C   |
| O <sub>Thys</sub>      | Thermal shut-down temperature hysteresis              | 10  |     | °C   |
| R <sub>Th j-amb</sub>  | Thermal resistance junction-to-ambient <sup>(1)</sup> |     | 20  | °C/W |
| R <sub>Th j-case</sub> | Thermal resistance junction-to-case                   |     | 2   | °C/W |

1. with 2s2p PCB thermally enhanced.

## 2.5 Electrical characteristics

V<sub>B</sub> = 6 V to 18 V, T<sub>amb</sub> = -40 °C to 125 °C.

### 2.5.1 Supply

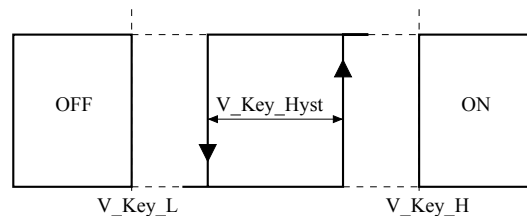
**Table 6. Supply electrical characteristics**

| Symbol               | Parameter                             | Condition                                      | Min  | Typ  | Max  | Unit |
|----------------------|---------------------------------------|------------------------------------------------|------|------|------|------|
| V <sub>B</sub>       | Operating supply voltage range        | -                                              | 6    | -    | 18   | V    |
| V <sub>B_off</sub>   | Vbat switch off threshold voltage     | -                                              | 30   | 32   | 34   | V    |
| V <sub>B_OVh</sub>   | Overvoltage threshold hysteresis      | -                                              | 0.5  | -    | -    | V    |
| V <sub>B_UVL</sub>   | Undervoltage disable LOW threshold    | -                                              | 3.5  | 3.7  | 3.9  | V    |
| V <sub>B_UVh</sub>   | Undervoltage threshold hysteresis     | -                                              | 0.3  | -    | 1    | V    |
| I <sub>VB(dis)</sub> | Standby current from VB, VB_1         | VB = VB_1 = 13 V, device disabled, KEY < 0.7 V | -    | -    | 120  | µA   |
| I <sub>VB</sub>      | Quiescent current                     | VB = VB_1 = 13 V, outputs floating             | -    | -    | 20   | mA   |
| V <sub>rext</sub>    | ASIC Bias reference                   | Application info                               | -    | 1.22 | -    | V    |
| f <sub>int_clk</sub> | Internal clock reference              | Application info                               | -    | 5.6  | -    | MHz  |
| Tdgc_VB_OV           | VB overvoltage shut-down filter time  | Guaranteed by scan                             | 22.5 | 30   | 37.5 | µs   |
| Tdgc_VB_UV           | VB undervoltage shut-down filter time | Guaranteed by scan                             | 0.8  | 1    | 1.2  | µs   |

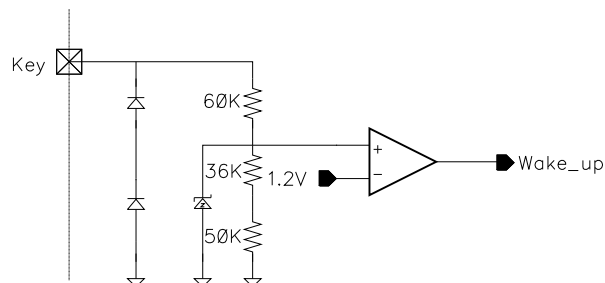
## 2.5.2 Key

**Table 7. Key electrical characteristics**

| Symbol         | Parameter                                       | Condition                                        | Min | Typ | Max | Unit |
|----------------|-------------------------------------------------|--------------------------------------------------|-----|-----|-----|------|
| V_Key_L        | Input level low                                 | -                                                | -   | -   | 1.5 | V    |
| V_Key_H        | Input level high                                | -                                                | 3.3 | -   | -   | V    |
| V_Key_Hyst     | Input voltage hysteresis                        | -                                                | 0.5 | -   | 1.8 | V    |
| R_Key          | Internal pull down                              | -                                                | 50  | 150 | 300 | kΩ   |
| T_key_deglitch | Key input filter time                           | Guaranteed by scan                               | 26  | -   | 40  | μs   |
| T_key_delay    | Maximum delay time from Key to regulator enable | Time from key rising edge to 20% VDD rising edge | -   | -   | 200 | μs   |

**Figure 3. Input threshold**


GADG1911180723PS

**Figure 4. Key block diagram**


GAPGPS00588

## 2.5.3 Digital pins

**Table 8. Digital pins characteristics**

| Symbol                 | Parameter                                       | Condition | Min     | Typ | Max     | Unit |
|------------------------|-------------------------------------------------|-----------|---------|-----|---------|------|
| V <sub>in_L</sub>      | Input level low                                 | -         | -       | -   | 0.3*VDD | V    |
| V <sub>in_H</sub>      | Input level high                                | -         | 0.7*VDD | -   | -       | V    |
| V <sub>h in</sub>      | Input voltage hysteresis                        | -         | 0.1     | -   | -       | V    |
| R <sub>pull</sub>      | Internal pull-down/pull-up <sup>(1)(2)(3)</sup> | -         | 50      | 150 | 250     | kΩ   |
| I <sub>pull_down</sub> | Active pull-down                                | -         | 10      | -   | 100     | μA   |

1. Pins with active pull-down: DIR.
2. Pins with pull-down: EN, PWM, ISL-TACH, INO2H, IN\_REL1-2, IN1-2;
3. Pins with pull-up: SI, SCK, CS, KL-TX;

## 2.5.4 Digital output pins

**Table 9. Digital output pins characteristics**

| Symbol | Parameter         | Condition                                          | Min     | Typ | Max | Unit |
|--------|-------------------|----------------------------------------------------|---------|-----|-----|------|
|        | Output level low  | $I_{\text{sink}} = 2\text{mA}$                     | -       | -   | 0.4 | V    |
|        | Output level high | $I_{\text{source}} = 2\text{mA}$ <sup>(1)(2)</sup> | VDD-0.5 | -   | -   | V    |

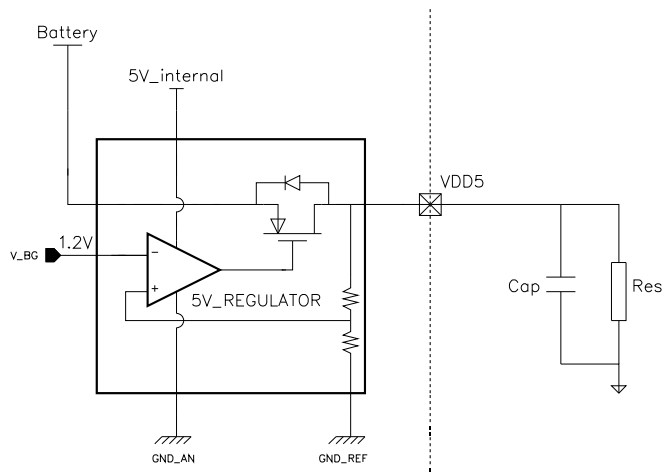
1. Pins with push-pull stage and tri-state condition: SDO

2. Pins with open drain output: RESET, VROUT;

## 2.5.5 5 V voltage regulator

**Table 10. VDD output electrical characteristics**

| Symbol              | Parameter                                             | Condition                                                                                      | Min  | Typ | Max  | Unit          |
|---------------------|-------------------------------------------------------|------------------------------------------------------------------------------------------------|------|-----|------|---------------|
| VDD                 | Output voltage                                        | -                                                                                              | 4.9  | 5   | 5.1  | V             |
| Ln_vdd              | Line regulation                                       | $V_B = 6\text{ V to }18\text{ V}$<br>$I_{\text{load}} = 150\text{ mA}$                         | -25  | -   | 25   | mV            |
| Ld_vdd              | Load regulation                                       | $V_B = 13\text{ V}$<br>$I_{\text{load}} = 5\text{ mA to }300\text{ mA}$                        | -25  | -   | 25   | mV            |
| V <sub>dd_OS</sub>  | Max overshoot                                         | Recovery from ISO pulse stimuli on battery line (guaranteed by design)                         | -    | -   | 5.5  | V             |
| V <sub>dd_SR</sub>  | Voltage slew-rate at power-on                         | $C_{\text{load}} = 4.7\text{ }\mu\text{F}$                                                     | 2    | -   | 25   | V/ms          |
| I <sub>dd</sub>     | Load current                                          | -                                                                                              | 5    | -   | 300  | mA            |
| I <sub>dd_max</sub> | Current limitation                                    | Output short to 4 V                                                                            | 350  | -   | 600  | mA            |
| I <sub>dd_STG</sub> | Short to ground current limitation                    | Output shorted to GND                                                                          | 350  | -   | 700  | mA            |
| PSRR                | Power supply rejection ratio                          | Sin wave @ 1 kHz 1 Vpp; $V_B = 13\text{ V}$ ; $I_{\text{load}} = 5\text{ mA to }300\text{ mA}$ | 40   | -   | -    | dB            |
| V <sub>dr5</sub>    | $V_B - V_{\text{dd}} - V_{\text{dd dropout voltage}}$ | $V_B = 5\text{ V}$ ; $I_{\text{load}} = 300\text{ mA}$                                         | 0.30 | -   | 0.75 | V             |
| Tdcg_VDD            | VDD thermal shutdown filter time                      | Guaranteed by scan                                                                             | 22.5 | 30  | 37.5 | $\mu\text{s}$ |

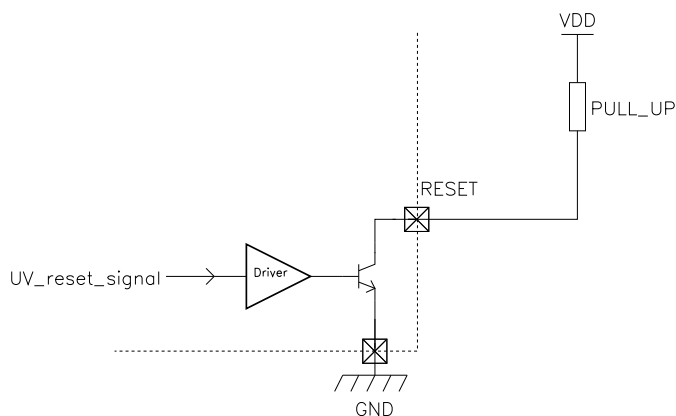
**Figure 5. 5 V main regulator block diagram**


GADG0412171216PS

## 2.5.6 Reset

**Table 11. Reset function electrical characteristics**

| Symbol            | Parameter                        | Condition                                            | Min | Typ | Max                    | Unit          |
|-------------------|----------------------------------|------------------------------------------------------|-----|-----|------------------------|---------------|
| VUV_LO            | Output low voltage               | $1 < VDD < V_{th\_UV}$ , $I_{reset} = 2 \text{ mA}$  | -   | -   | 0.6                    | V             |
| IUV_LO            | Reset current capability         | $1 < VDD < V_{th\_UV}$ , $V_{reset} = 0.6 \text{ V}$ | 2   | -   | -                      | mA            |
| $I_{lk}$          | Leakage current                  | $VUV\_reset = 4.5 \text{ V}$                         | -   | -   | 1                      | $\mu\text{A}$ |
| $V_{th\_UV}$      | VDD under voltage low threshold  | $V_B = 13.5 \text{ V}$                               | 4.5 | -   | $VDD - 150 \text{ mV}$ | V             |
| $V_{th\_UV\_Th}$  | VDD under voltage high threshold | -                                                    | 4.5 | -   | $VDD - 50 \text{ mV}$  | V             |
| $V_{th\_UV\_HYS}$ | VDD under voltage hysteresis     | -                                                    | 50  | -   | -                      | mV            |
| $Td\_UV\_rst$     | Power on UV reset delay          | -                                                    | 17  | 22  | 30                     | ms            |
| $TfUV\_reset$     | UV reset filter                  | $VDD < V_{th\_UV}$                                   | 25  | 50  | 75                     | $\mu\text{s}$ |

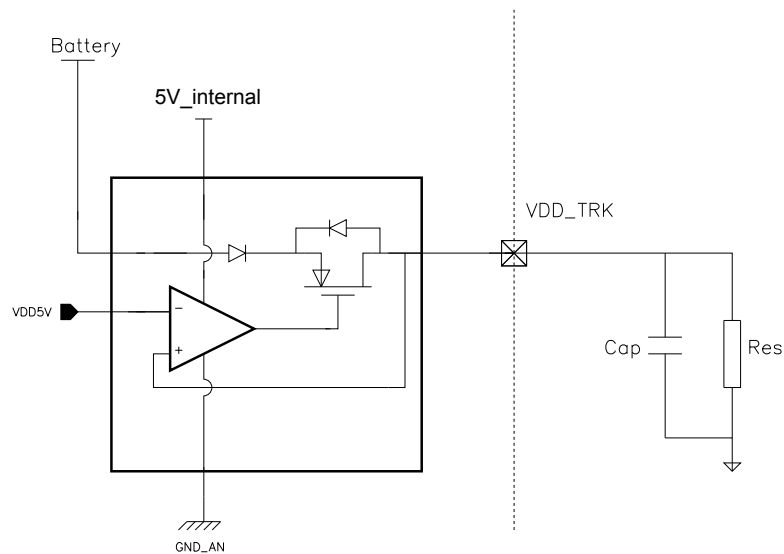
**Figure 6. Reset**


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## 2.5.7 5 V tracking voltage regulator

**Table 12. VDD\_TRK output electrical characteristics**

| Symbol         | Parameter                                                  | Condition                                                                             | Min | Typ | Max   | Unit |
|----------------|------------------------------------------------------------|---------------------------------------------------------------------------------------|-----|-----|-------|------|
| $DV_{ddtrk}$   | Output voltage tracking error                              | $V_B = 6\text{ V}$ ,<br>$I_{trk} = 1\text{ to }40\text{ mA}$                          | -15 | -   | 15    | mV   |
| $V_{short}$    | Tracking output short circuit voltage range                | -                                                                                     | -2  | -   | $V_B$ | V    |
| $I_{trk\_max}$ | Output current limitation                                  | Output short to 4 V                                                                   | 50  | -   | 100   | mA   |
| $I_{trk\_sb}$  | Tracking output reverse current (limited by the regulator) | Output shorted to $V_B = 16\text{ V}$                                                 | -   | -   | 10    | mA   |
| $I_{dd}$       | Load current                                               | -                                                                                     | 1   | -   | 40    | mA   |
| $Ln\_vdd\_trk$ | Line regulation                                            | $V_B = 6\text{ V to }18\text{ V}$ - $I_{load} = 40\text{ mA}$                         | -15 | -   | 15    | mV   |
| $Ld\_vdd\_trk$ | Load regulation                                            | $V_B = 13\text{ V}$ $I_{load} = 1\text{ to }40\text{ mA}$                             | -15 | -   | 15    | mV   |
| PSRR           | Power supply rejection ratio                               | Sin wave @ 1 kHz 1 Vpp<br>$V_B = 13\text{ V}$ , $I_{load} = 1\text{ to }40\text{ mA}$ | 40  | -   | -     | dB   |

**Figure 7. 5 V tracking regulator block diagram**


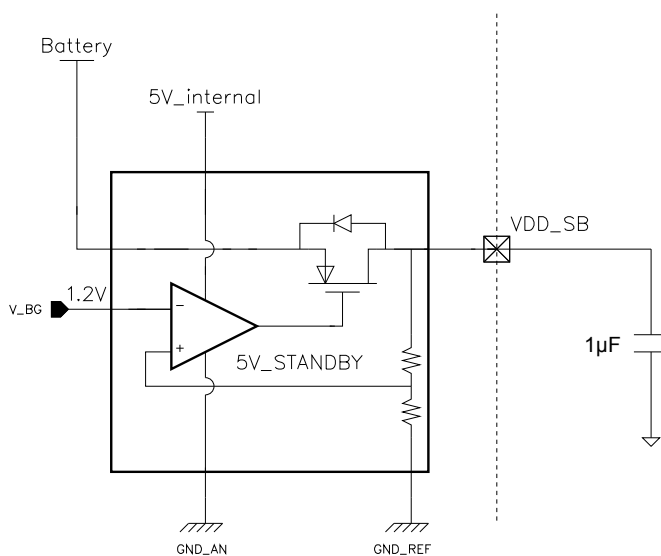
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## 2.5.8 Standby regulator

**Table 13. VDD\_SB output electrical characteristics**

| Symbol       | Parameter       | Condition                                                          | Min  | Typ | Max  | Unit |
|--------------|-----------------|--------------------------------------------------------------------|------|-----|------|------|
| $V_{ddsb}$   | Output voltage  | -                                                                  | 4.75 | 5   | 5.25 | V    |
| $Ln\_vsb$    | Line regulation | $V_B = 6\text{ V to }18\text{ V}$<br>$I_{load} = 1\text{ mA}$      | -25  | -   | 25   | mV   |
| $Ld\_vsb$    | Load regulation | $V_B = 13\text{ V}$<br>$I_{load} = 0.1\text{ mA to }2.5\text{ mA}$ | -25  | -   | 25   | mV   |
| $V_{dd\_OS}$ | Max overshoot   | -                                                                  | -    | -   | 5.5  | V    |
| $I_{dd}$     | Load current    | -                                                                  | 0.1  | -   | 2.5  | mA   |

| Symbol        | Parameter                     | Condition                                                            | Min | Typ | Max | Unit |
|---------------|-------------------------------|----------------------------------------------------------------------|-----|-----|-----|------|
| $I_{sb\_max}$ | Current limitation            | Output short to 4 V                                                  | 5   | -   | 50  | mA   |
| $V_{sb\_SR}$  | Voltage slew-rate at power on | $C_{load} = 1 \mu F$                                                 | 2   | -   | 30  | V/ms |
| PSRR          | Power supply rejection ratio  | Sin wave @ 1 kHz 1 Vpp<br>$V_B = 13 V$<br>$I_{load} = 0.1$ to $1 mA$ | 40  | -   | -   | dB   |

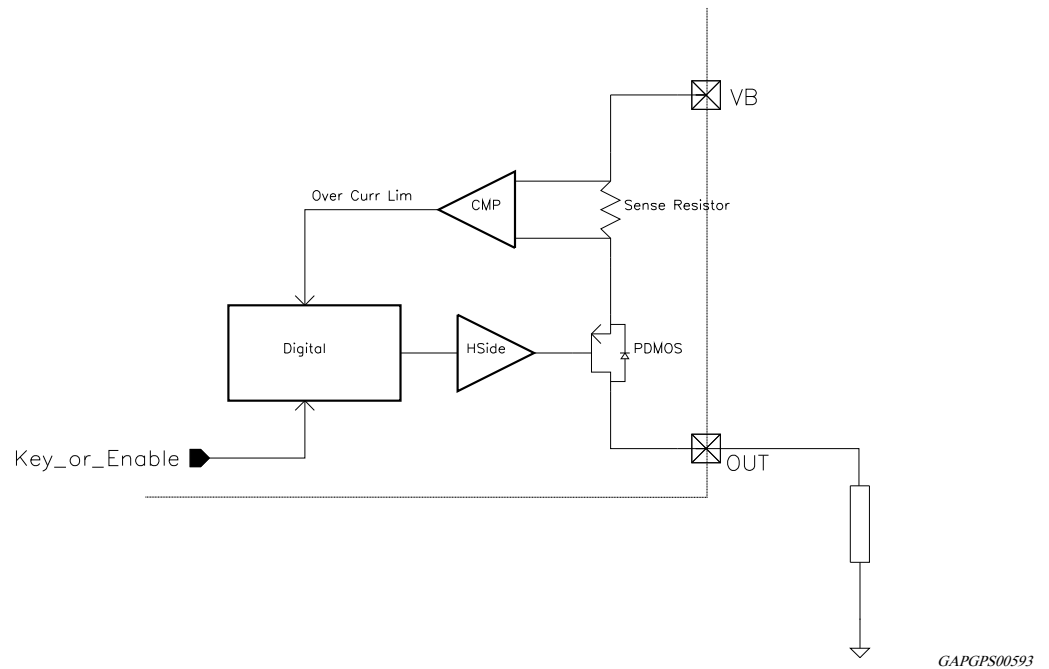
**Figure 8. 5 V standby regulator block diagram**


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### 2.5.9 High side switch

**Table 14. HS\_OUT output electrical characteristics**

| Symbol        | Parameter          | Condition        | Min | Typ | Max | Unit     |
|---------------|--------------------|------------------|-----|-----|-----|----------|
| $R_{on\_hs}$  | $R_{on}$           | $I_{hs} = 50 mA$ | -   | -   | 14  | $\Omega$ |
| $I_{hs\_max}$ | Current limitation | $V_B = 13.5 V$   | 100 | -   | 400 | mA       |

**Figure 9. High-side driver block diagram**


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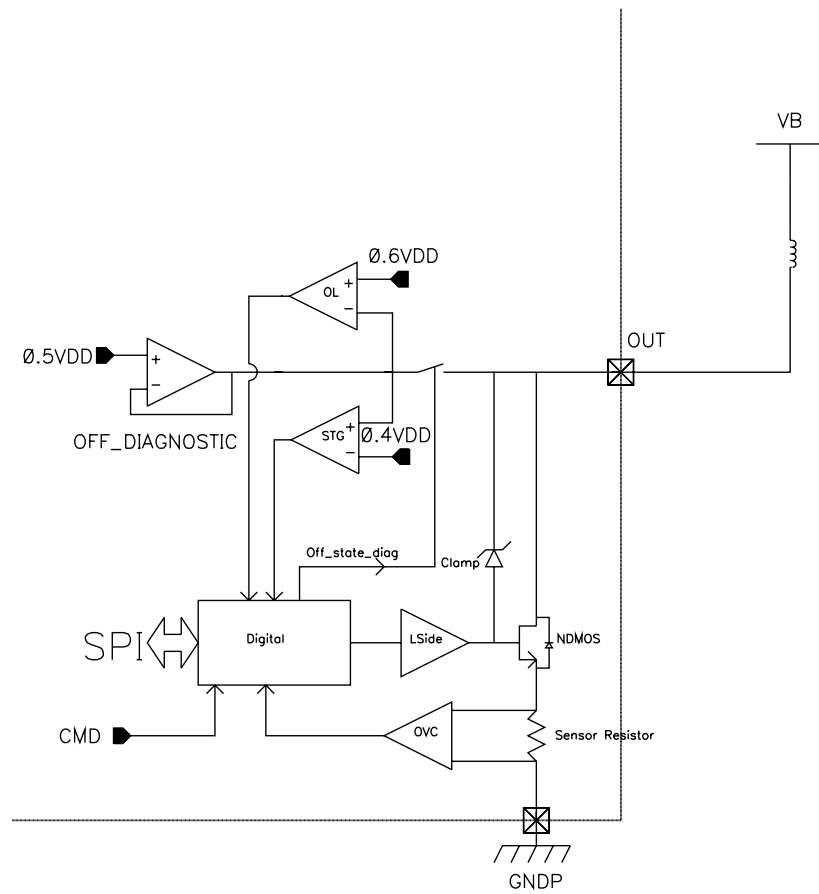
The High side switch is intended as a protected battery and is directly controlled by key input (see [Figure 21](#)).

### 2.5.10 Injector driver

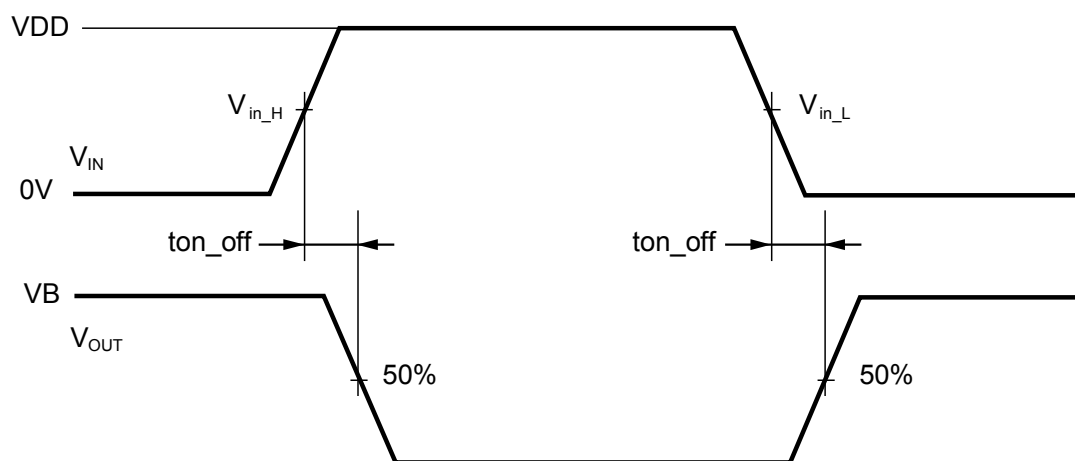
**Table 15. Injector driver electrical characteristic**

| Symbol              | Parameter                           | Condition                                          | Min                 | Typ                | Max                 | Unit          |
|---------------------|-------------------------------------|----------------------------------------------------|---------------------|--------------------|---------------------|---------------|
| $I_{max}$           | Output current                      | -                                                  | -                   | -                  | 2.2                 | A             |
| $I_{oc}$            | Overcurrent threshold               | -                                                  | 2.8                 | -                  | 5                   | A             |
| $V_{DS}$            | Output clamping voltage             | $I = 2.2 \text{ A}$                                | 55                  | -                  | 65                  | V             |
| $R_{on}$            | On resistance                       | $I = 2.2 \text{ A}$                                | -                   | -                  | 0.6                 | $\Omega$      |
| $I_{lk\_off}$       | Leakage current                     | $V_{out} = 18 \text{ V}, \text{Key} = 0 \text{ V}$ | -                   | -                  | 10                  | $\mu\text{A}$ |
| $I_{lk\_on}$        | Pull-Down diagnosis current         | $V_{out} = 18 \text{ V}, \text{Key} = 5 \text{ V}$ | -                   | -                  | 100                 | $\mu\text{A}$ |
| $t_{on-off}$        | Turn on-off delay                   | from CMD edge to 50% output variation              | -                   | -                  | 6                   | $\mu\text{s}$ |
| $V_{OL}$            | Open load output voltage            | Driver in OFF condition                            | $0.46 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V             |
| $V_{diag\_H}^{(1)}$ | Diagnostic high threshold           | Driver in OFF condition                            | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V             |
| $V_{diag\_L}^{(1)}$ | Diagnostic low threshold            | Driver in OFF condition                            | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V             |
| $T_{mask}$          | OFF diagnostic masking time         | Guaranteed by scan                                 | 0.75                | 1                  | 1.25                | ms            |
| $T_{dcg\_noise}$    | OFF diagnostic Deglitch filter time | Guaranteed by scan                                 | 2.16                | 3.6                | 5.04                | $\mu\text{s}$ |
| $T_{dcg}$           | ON diagnostic Deglitch filter time  | Guaranteed by scan                                 | 15                  | 20                 | 25                  | $\mu\text{s}$ |

1.  $V_{diag\_L} < V_{out} < V_{diag\_H} \rightarrow \text{Open Load}; V_{out} < V_{diag\_L} \rightarrow \text{Short to GND}$

**Figure 10. Low-side driver block diagram**


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**Figure 11. Low-side timing diagram (injectors, relays, current limited LSD, tach, O2H)**


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## 2.5.11 Relay drivers

**Table 16. Relay driver characteristics**

| Symbol               | Parameter                           | Condition                                 | Min                 | Typ                | Max                 | Unit          |
|----------------------|-------------------------------------|-------------------------------------------|---------------------|--------------------|---------------------|---------------|
| $I_{max}$            | Output current                      | -                                         | -                   | -                  | 1                   | A             |
| $I_{oc}$             | Overcurrent threshold               | -                                         | 1.2                 | -                  | 2.5                 | A             |
| $V_{DS}$             | Output clamping voltage             | $I = 1\text{ A}$                          | 40                  | -                  | 50                  | V             |
| $R_{on}$             | On resistance                       | $I = 1\text{ A}$                          | -                   | -                  | 1.5                 | $\Omega$      |
| $I_{lk\_off}$        | Leakage current                     | $V_{out} = 18\text{ V}$ , Key = 0 V       | -                   | -                  | 10                  | $\mu\text{A}$ |
| $I_{lk\_on}$         | Pull-Down diagnosis current         | $V_{out} = 18\text{ V}$ , Key = 5 V       | -                   | -                  | 100                 | $\mu\text{A}$ |
| $t_{on\_off}$        | Turn on-off delay                   | From CMD (serial or parallel) rising edge | -                   | -                  | 6                   | $\mu\text{s}$ |
| $V_{OL}$             | Open load output voltage            | Driver in OFF condition                   | $0.46 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V             |
| $V_{diagH\_H}^{(1)}$ | Diagnostic high threshold           | Driver in OFF condition                   | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V             |
| $V_{diagH\_L}^{(1)}$ | Diagnostic low threshold            | Driver in OFF condition                   | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V             |
| Tmask                | OFF diagnostic masking time         | Guaranteed by scan                        | 2.63                | 3.5                | 4.38                | ms            |
| Tdcg_noise           | OFF diagnostic Deglitch filter time | Guaranteed by scan                        | 2.16                | 3.6                | 5.04                | $\mu\text{s}$ |
| Tdcg                 | ON diagnostic Deglitch filter time  | Guaranteed by scan                        | 15                  | 20                 | 25                  | $\mu\text{s}$ |

1.  $V_{diagH\_L} < V_{out} < V_{diagH\_H} \rightarrow$  Open Load;  $V_{out} < V_{diagH\_L} \rightarrow$  Short to GND

## 2.5.12 Current limited low side driver (LSD)

**Table 17. Current limited LSD driver characteristics**

| Symbol               | Parameter                               | Condition                                               | Min                 | Typ                | Max                 | unit          |
|----------------------|-----------------------------------------|---------------------------------------------------------|---------------------|--------------------|---------------------|---------------|
| $I_{LI}$             | Linear current limitation               | $V_B = 18\text{ V}$ , settling time = 300 $\mu\text{s}$ | 2                   | -                  | 2.45                | A             |
| $I_{oc}$             | Overcurrent threshold                   | Masked for driver during in-rush                        | 1.2                 | -                  | 1.95                | A             |
| $t_{dgmsk}$          | Diagnosis masking time in OFF condition | Guaranteed by scan                                      | 2                   | -                  | 5                   | ms            |
| $V_{DS}$             | Output clamping voltage                 | $I = 200\text{ mA}$                                     | 40                  | -                  | 50                  | V             |
| $R_{on}$             | On resistance                           | $I = 200\text{ mA}$                                     | -                   | -                  | 1.5                 | $\Omega$      |
| $I_{lk\_off}$        | Leakage current                         | $V_{out} = 18\text{ V}$ , Key = 0 V                     | -                   | -                  | 10                  | $\mu\text{A}$ |
| $I_{lk\_on}$         | Pull-Down diagnosis current             | $V_{out} = 18\text{ V}$ , Key = 5 V                     | -                   | -                  | 100                 | $\mu\text{A}$ |
| $t_{on\_off}$        | Turn on-off delay                       | From SPI CS rising edge                                 | -                   | -                  | 6                   | $\mu\text{s}$ |
| $V_{OL}$             | Open load output voltage                | Driver in OFF condition                                 | $0.46 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V             |
| $V_{diagH\_H}^{(1)}$ | Diagnostic high threshold               | Driver in OFF condition                                 | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V             |
| $V_{diagH\_L}^{(1)}$ | Diagnostic low threshold                | Driver in OFF condition                                 | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V             |
| Tmask                | OFF diagnostic masking time             | Guaranteed by scan                                      | 2.63                | 3.5                | 4.38                | ms            |
| Tdcg_noise           | OFF diagnostic Deglitch filter time     | Guaranteed by scan                                      | 2.16                | 3.6                | 5.04                | $\mu\text{s}$ |
| Tdcg                 | ON diagnostic Deglitch filter time      | Guaranteed by scan                                      | 15                  | 20                 | 25                  | $\mu\text{s}$ |
| Tmask_rush           | ON diagnostic inrush current mask time  | Guaranteed by scan                                      | 252                 | 336                | 420                 | $\mu\text{s}$ |

1.  $V_{diag\_L} < V_{out} < V_{diag\_H} \rightarrow$  Open Load;  $V_{out} < V_{diag\_L} \rightarrow$  Short to GND

## 2.5.13 Tachometer driver

**Table 18. Tachometer driver electrical characteristics**

| Symbol              | Parameter                           | Condition                                 | Min                 | Typ                | Max                 | Unit     |
|---------------------|-------------------------------------|-------------------------------------------|---------------------|--------------------|---------------------|----------|
| $I_{oc}$            | Overcurrent threshold               | -                                         | 100                 | -                  | 500                 | mA       |
| $R_{on}$            | On resistance                       | $I = 25$ mA                               | -                   | -                  | 5                   | $\Omega$ |
| $I_{lk\_off}$       | Leakage current                     | $V_{out} = 18$ V, Key = 0 V               | -                   | -                  | 10                  | $\mu$ A  |
| $I_{lk\_on}$        | Pull-Down diagnosis current         | $V_{out} = 18$ V, Key = 5 V               | -                   | -                  | 100                 | $\mu$ A  |
| $t_{on\_off}$       | Turn on-off delay                   | From CMD (serial or parallel) rising edge | -                   | -                  | 6                   | $\mu$ s  |
| $V_{OL}$            | Open load output voltage            | driver in OFF condition                   | $0.46 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V        |
| $V_{diag\_H}^{(1)}$ | Diagnostic high threshold           | Driver in OFF condition                   | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V        |
| $V_{diag\_L}^{(1)}$ | Diagnostic low threshold            | Driver in OFF condition                   | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V        |
| Tmask               | OFF diagnostic masking time         | Guaranteed by scan                        | 0.75                | 1                  | 1.25                | ms       |
| Tdcg_noise          | OFF diagnostic Deglitch filter time | Guaranteed by scan                        | 2.16                | 3.6                | 5.04                | $\mu$ s  |
| Tdcg                | ON diagnostic Deglitch filter time  | Guaranteed by scan                        | 15                  | 20                 | 25                  | $\mu$ s  |

1.  $V_{diag\_L} < V_{out} < V_{diag\_H} \rightarrow$  Open Load;  $V_{out} < V_{diag\_L} \rightarrow$  Short to GND

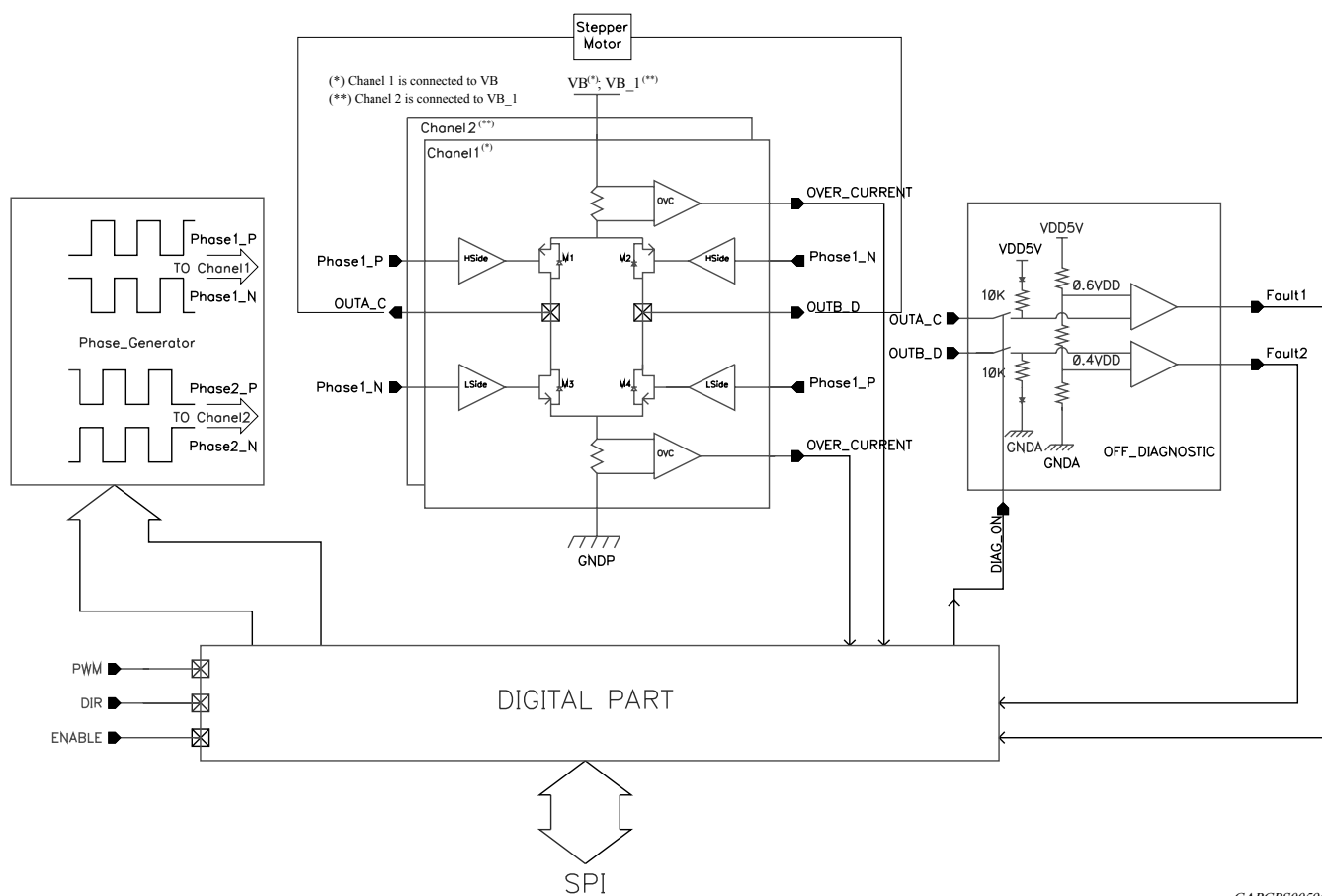
## 2.5.14 Stepper motor driver

**Table 19. Stepper motor driver electrical characteristics**

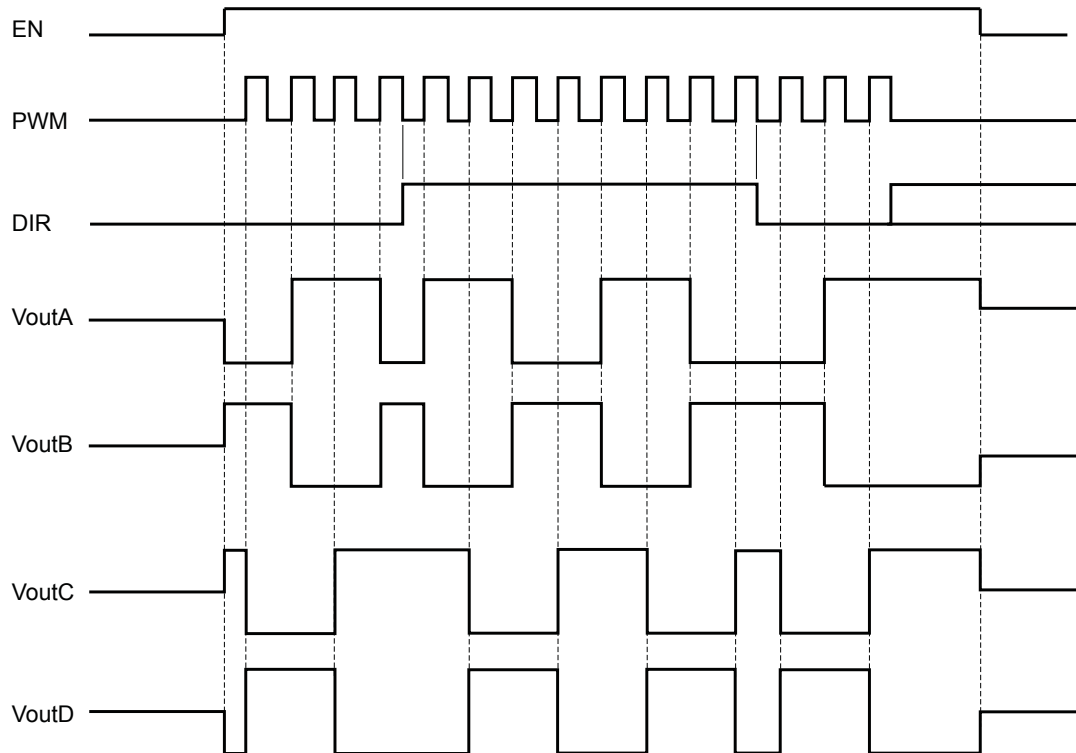
| Symbol                     | Parameter                    | Condition                                                         | Min                 | Typ                | Max                 | Unit     |
|----------------------------|------------------------------|-------------------------------------------------------------------|---------------------|--------------------|---------------------|----------|
| $I_{oc}$                   | Overcurrent threshold        | ON condition                                                      | 0.85                | -                  | 2                   | A        |
| $R_{dsON}$                 | On resistance HS+LS          | $I_{out} = 0.5$ A,<br>$T_j = 150$ °C, $V_B = 14$ V                | -                   | -                  | 2.6                 | $\Omega$ |
| $f_{stepper}$              | Working frequency            | Application info                                                  | -                   | -                  | 20                  | kHz      |
| $V_{out\_off}^{(1)(2)(3)}$ | OUTA_B_C_D output voltage    | OUTA short to OUTB; OUTC short to OUTD;<br>Stepper driver disable | $0.44 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V        |
| $V_{diag\_H}$              | Diagnostic high threshold    | Driver in OFF condition                                           | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V        |
| $V_{diag\_L}$              | Diagnostic low threshold     | Driver in OFF condition                                           | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V        |
| $I_{DSS\_OUT}$             | Output leakage current       | Driver in OFF condition                                           | -                   | -                  | 10                  | $\mu$ A  |
| $t_{scvb}$                 | Over current switch_off time | Guaranteed by scan                                                | -                   | -                  | 25                  | $\mu$ s  |
| $t_{rb}$                   | Rise output time             | $V_B = 12$ V, $R_l = 39$ $\Omega$                                 | -                   | -                  | 15                  | $\mu$ s  |
| $t_{fb}$                   | Fall output time             | $V_B = 12$ V, $R_l = 39$ $\Omega$                                 | -                   | -                  | 15                  | $\mu$ s  |
| $t_{rb-a}$                 | Rise output time             | $T_{amb} = 25$ °C,                                                | -                   | -                  | 10                  | $\mu$ s  |
| $t_{fb-a}$                 | Fall output time             | $V_B = 12$ V, $R_l = 39$ $\Omega$                                 | -                   | -                  | 10                  | $\mu$ s  |
| $t_{pHLb}$                 | Turn-off in/out delay time   | $V_B = 12$ V, $R_l = 39$ $\Omega$                                 | -                   | -                  | 15                  | $\mu$ s  |
| $t_{pLHb}$                 | Turn-off in/out delay time   |                                                                   | -                   | -                  | 15                  | $\mu$ s  |
| $V_{reverse\_HS}$          | Reverse HS diode drop        | Driver in OFF condition $I_{injected} = 0.5$ A                    | -                   | -                  | 1.5                 | V        |
| $V_{reverse\_LS}$          | Reverse LS diode drop        | Driver in OFF condition $I_{sourced} = 0.5$ A                     | -                   | -                  | -1.5                | V        |

| Symbol        | Parameter                           | Condition          | Min  | Typ | Max   | Unit |
|---------------|-------------------------------------|--------------------|------|-----|-------|------|
| Tdgc_step_OFF | OFF Diagnostic Deglitch filter time | Guaranteed by scan | 93.8 | 125 | 156.3 | µs   |
| Tmask         | Masking time                        | Guaranteed by scan | 0.75 | 1   | 1.25  | ms   |
| Tdgc_step_ON  | ON Diagnostic Deglitch filter time  | Guaranteed by scan | 15   | 20  | 25    | µs   |

1.  $V_{outA} < V_{diagth\_H}$  and  $V_{outB} > V_{diagth\_L}$  or  $V_{outC} < V_{diagth\_H}$  and  $V_{outD} > V_{diagth\_L} \rightarrow$  No Fault
2.  $V_{outA\_B\_C\_D} < V_{diagth\_L} \rightarrow$  Short to GND
3.  $V_{outA} > V_{diagth\_H}$  and  $V_{outB} < V_{diagth\_L}$  or  $V_{outC} > V_{diagth\_H}$  and  $V_{outD} < V_{diagth\_L} \rightarrow$  Open load  
 $V_{outA\_B\_C\_D} > V_{diagth\_H} \rightarrow$  Short to Battery

**Figure 12. Stepper motor driver block diagram**


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**Figure 13. Stepper motor operations**


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## 2.5.15 O2 sensor heater driver

**Table 20. O2 sensor heater driver characteristics**

| Symbol               | Parameter                           | Condition                                        | Min                 | Typ                | Max                 | Unit          |
|----------------------|-------------------------------------|--------------------------------------------------|---------------------|--------------------|---------------------|---------------|
| $R_{dsON}$           | On resistance                       | $I_{out} = 3\text{ A}$                           | -                   | -                  | 0.5                 | $\Omega$      |
| $V_C$                | Output clamping voltage             | $I_{out} = 3\text{ A}$                           | 40                  | -                  | 50                  | V             |
| $I_{lk\_off}$        | Leakage current                     | $V_{out} = 18\text{ V}, \text{Key} = 0\text{ V}$ | -                   | -                  | 10                  | $\mu\text{A}$ |
| $I_{lk\_on}$         | Pull-Down diagnosis current         | $V_{out} = 18\text{ V}, \text{Key} = 5\text{ V}$ | -                   | -                  | 100                 | $\mu\text{A}$ |
| $t_{on\_off}$        | Turn on-off delay                   | From CMD (serial or parallel) rising edge        | -                   | -                  | 6                   | $\mu\text{s}$ |
| $V_{OL}$             | Open load output voltage            | Driver in OFF condition                          | $0.46 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.54 \cdot V_{DD}$ | V             |
| $I_{OC}$             | Overcurrent threshold               |                                                  | 3.8                 | -                  | 5                   | A             |
| $V_{diagH\_H}^{(1)}$ | Diagnostic high threshold           | Driver in OFF condition                          | $0.54 \cdot V_{DD}$ | $0.6 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | V             |
| $V_{diagH\_L}^{(1)}$ | Diagnostic low threshold            | Driver in OFF condition                          | $0.36 \cdot V_{DD}$ | $0.4 \cdot V_{DD}$ | $0.44 \cdot V_{DD}$ | V             |
| Tmask                | OFF diagnostic masking time         | Guaranteed by scan                               | 0.75                | 1                  | 1.25                | ms            |
| Tdcg_noise           | OFF diagnostic Deglitch filter time | Guaranteed by scan                               | 2.16                | 3.6                | 5.04                | $\mu\text{s}$ |
| Tdcg                 | ON diagnostic Deglitch filter time  | Guaranteed by scan                               | 15                  | 20                 | 25                  | $\mu\text{s}$ |

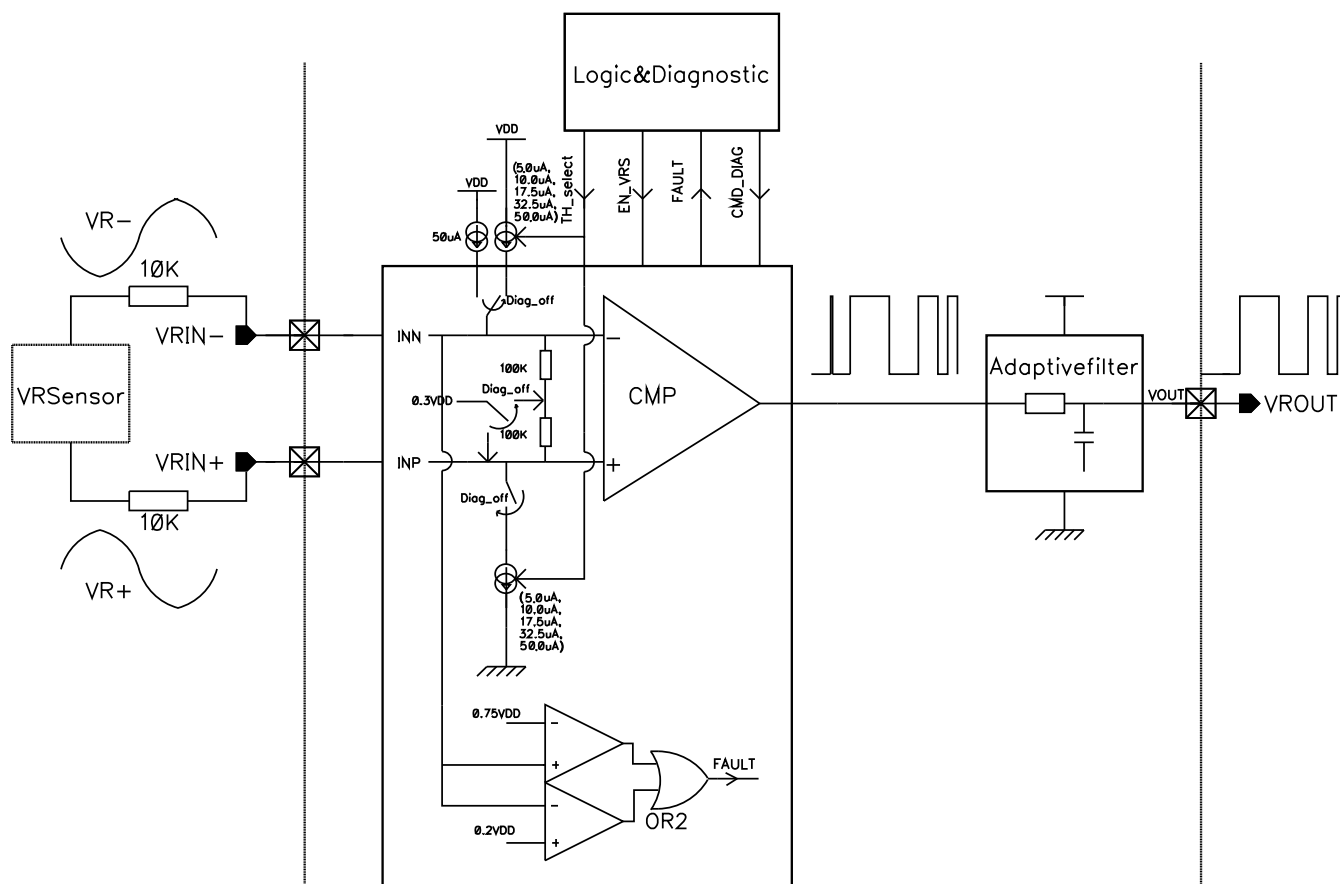
1.  $V_{diagH\_L} < V_{out} < V_{diagH\_H} \rightarrow \text{Open Load}; V_{out} < V_{diagH\_L} \rightarrow \text{Short to GND}$

## 2.5.16 Variable reluctance sensor interface

**Table 21. Variable reluctance sensor interface electrical characteristics**

| Symbol                 | Parameter                                                                 | Condition                                                    | Min                 | Typ                 | Max                 | Unit       |
|------------------------|---------------------------------------------------------------------------|--------------------------------------------------------------|---------------------|---------------------|---------------------|------------|
| $V_{HTH}$              | Input high to low differential threshold voltage at VRIN+ and VRIN- nodes | -                                                            | -50                 | -                   | 50                  | mV         |
| $V_{CM}$               | Common mode operating range at VRIN+ and VRIN-                            | -                                                            | 0                   | 1.5                 | 3                   | V          |
| $V_{cm\_internal}$     | Internal common mode voltage                                              | Switch off hysteresis current                                | $0.27 \cdot V_{DD}$ | $0.3 \cdot V_{DD}$  | $0.33 \cdot V_{DD}$ | V          |
| $V_{diagth\_H}^{(1)}$  | Diagnostic high threshold                                                 | Diagnostic voltage referred to VRIN- (see Figure 14)         | $0.67 \cdot V_{DD}$ | $0.75 \cdot V_{DD}$ | $0.82 \cdot V_{DD}$ | V          |
| $V_{diagth\_L}^{(1)}$  | Diagnostic low threshold                                                  |                                                              | $0.18 \cdot V_{DD}$ | $0.2 \cdot V_{DD}$  | $0.22 \cdot V_{DD}$ | V          |
| $I_{diag}$             | Diagnostic current                                                        | Current from VRIN- when diagnostic on                        | 35                  | 50                  | 65                  | $\mu A$    |
| $R_{internal\_common}$ | Internal common mode resistor                                             | Switch off hysteresis current                                | 50                  | 200                 | 350                 | k $\Omega$ |
| $I_{IB}$               | Input bias current                                                        | $VRIN+ = VRIN- = 1.5 V$                                      | -                   | -                   | 2                   | $\mu A$    |
| $I_{leak}$             | Output leakage                                                            | $V_{ROUT} = 5 V$                                             | -                   | -                   | 1                   | $\mu A$    |
| $V_{CLPH}$             | Input high clamping voltage                                               | $VRIN+ =  VRIN-  = 20 mA$                                    | -                   | 5                   | -                   | V          |
| $V_{CLPL}$             | Input low clamping voltage                                                | $VRIN+ =  VRIN-  =  20 mA $                                  | -1.5                | -                   | -0.3                | V          |
| $t_{of}$               | Output fall time                                                          | $C_{LOAD} = 20 pF$ , $R_{LOAD} = 5 k\Omega$                  | -                   | -                   | 300                 | ns         |
| $t_{of\_1nf}$          | Output fall time                                                          | $C_{LOAD} = 1 nF$                                            | -                   | -                   | 1.5                 | $\mu s$    |
| $V_{OUTL}$             | Output buffer low voltage                                                 | $I_{sink} = 2 mA$                                            | -                   | -                   | 0.6                 | V          |
| $I_{OUTL}$             | Output current capability                                                 | $V_{out} = 0.6 V$                                            | 2                   | -                   | -                   | mA         |
| $t_{prop}$             | Propagation delay                                                         | VRS INM = 0.5 V, INP applied to 1 V to make VRS OUT commuted | 0.1                 | 0.45                | 0.8                 | $\mu s$    |
| Tdgc_VRS               | OFF Diagnostic Deglitch filter time                                       | Guaranteed by scan                                           | 24                  | 30                  | 36                  | $\mu s$    |

1. if  $(VRIN- > V_{diagth\_H})$  or  $(VRIN- < V_{diagth\_L})$  then Fault is detected.

**Figure 14. VRS block diagram**


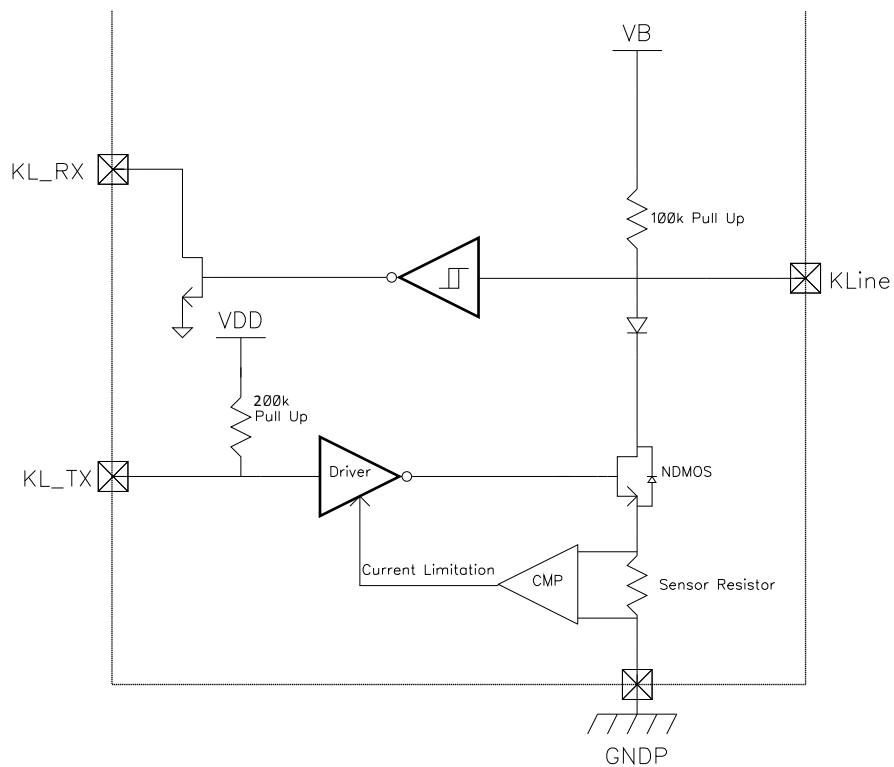
GAPGPS00598

### 2.5.17 K-line

**Table 22. K-Line interface electrical characteristics**

| Pin    | Symbol    | Parameter                           | Test conditions                                         | Min.    | Typ. | Max.    | Unit       |
|--------|-----------|-------------------------------------|---------------------------------------------------------|---------|------|---------|------------|
| KL_TX  | ITXsource | Transmitter input source current    | -                                                       | 10      | -    | 100     | $\mu$ A    |
|        | ITXsink   | Transmitter input sink current      | KL_TX = VDD                                             | -       | -    | 2.1     | $\mu$ A    |
|        | IKL_TX    | KL_TX Internal Pull-up              | -                                                       | -       | 200  | -       | k $\Omega$ |
| K_LINE | VKoutL    | Transmitter output low voltage      | IsinkK_LINE = 35 mA,<br>KL_TX = Low                     | -1      | -    | 1.5     | V          |
|        | VKinH     | Receiver input high voltage         | -                                                       | 0.7xVB  | -    | VB      | V          |
|        | VKinL     | Receiver input low voltage          | -                                                       | -1      | -    | 0.35xVB | V          |
|        | VKH       | Receiver input hysteresis           | -                                                       | 0.05xVB | -    | 0.3xVB  | V          |
|        | IKleak    | Receiver leakage current            | KL_LINE = VB, KL_TX = High                              | -       | -    | 1       | $\mu$ A    |
| K_LINE | IKshort   | Transmitter short circuit current   | KL_LINE = VB, KL_TX = Low                               | 60      | -    | -       | mA         |
|        | IKrev     | Reverse battery or GND loss current | ENABLE = KEY = VB = 0 V,<br>KL_LINE = -13.5             | -       | -    | 10      | mA         |
|        | IKpull-up | KLINE internal pull-up              | KL_TX = High                                            | 60      | -    | 140     | k $\Omega$ |
|        | IKuv      | Under voltage current               | KEY = High, KL_TX = Low, VB = 13.5 V,<br>KL_LINE = -1 V | -       | -    | 1       | mA         |

| Pin              | Symbol  | Parameter                            | Test conditions                                               | Min. | Typ. | Max. | Unit          |
|------------------|---------|--------------------------------------|---------------------------------------------------------------|------|------|------|---------------|
| KL_RX            | VRXoutL | KL_RX output low voltage             | $I_{\text{sink}} = 0.4 \text{ mA}$                            | -    | -    | 0.4  | V             |
| KL_TX to K_LINE  | Tp_HLT  | Transmitter turn-on delay time       | CKline = 10 nF,<br>RKline = 510 $\Omega$                      | -    | -    | 5    | $\mu\text{s}$ |
| K_LINE           | T_fT    | Transmitter fall time                | CKline = 10 nF,<br>RKline = 510 $\Omega$                      | -    | -    | 10   | $\mu\text{s}$ |
| KL_LINE to KL_RX | TpR     | Receiver turn-on delay time          | $C_{\text{load}} = 20 \text{ pF}$ ,<br>RPKL_Rx = 2 k $\Omega$ | -    | -    | 4    | $\mu\text{s}$ |
| KL_RX            | T_fR    | Receiver fall time                   | $C_{\text{load}} = 20 \text{ pF}$ ,<br>RPKL_Rx = 2 k $\Omega$ | -    | -    | 2    | $\mu\text{s}$ |
|                  | T_rR    | Receiver rise time                   | $C_{\text{load}} = 20 \text{ pF}$ ,<br>RPKL_Rx = 2 k $\Omega$ | -    | -    | 2    | $\mu\text{s}$ |
| K_LINE           | fMax    | Max transmission Operating frequency | Application info                                              | -    | -    | 60   | kHz           |

**Figure 15. K-line block diagram**


GAPGPS00599

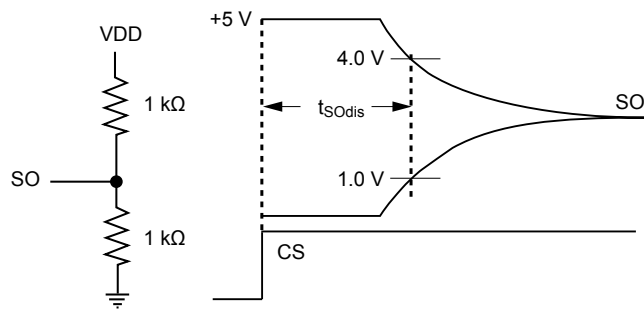
## 2.5.18 SPI interface

**Table 23. SPI characteristics and timings**

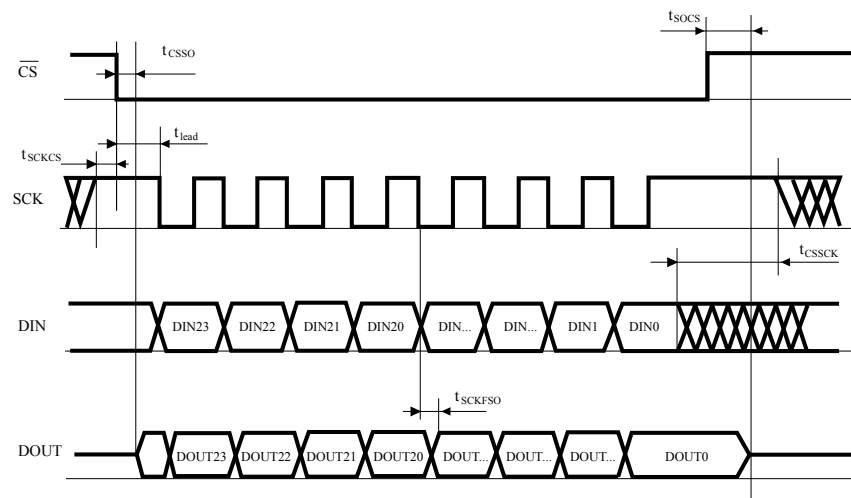
| Symbol             | Parameter                        | Test conditions | Min | Typ | Max | Unit |
|--------------------|----------------------------------|-----------------|-----|-----|-----|------|
| SiCin              | Input capacitance                | -               | -   | -   | 20  | pF   |
| SCKCin             |                                  | -               | -   | -   | 20  | pF   |
| t <sub>sckcs</sub> | Clock inactive time before frame | -               | 100 | -   | -   | ns   |

| Symbol        | Parameter                       | Test conditions                            | Min | Typ | Max | Unit |
|---------------|---------------------------------|--------------------------------------------|-----|-----|-----|------|
| $t_{CSSO}$    | Access time                     | See <sup>(1)</sup>                         | -   | -   | 500 | ns   |
| $t_{SOdis}$   | Output data (SO) disable time   | No Capacitor on SO,<br>See <sup>(2)</sup>  | -   | -   | 500 | ns   |
| $t_{lead}$    | Channels select (CS) lead time  | See <sup>(1)</sup>                         | 500 | -   | -   | ns   |
| $t_{SCKFSO}$  | Output valid time               | See <sup>(1)</sup> , @ $f_{CLK} = 5.4$ MHz | 60  | -   | -   | ns   |
| $t_{SOCS}$    | Output data (SO) disable time   | No capacitor on SO, see <sup>(1)</sup>     |     | -   | 500 | ns   |
| $t_{SIsetup}$ | Input data (SI) set-up time     | @ $f_{CLK} = 5.4$ MHz                      | 20  | -   | -   | ns   |
| $t_{SIhold}$  | Input data (SI) hold time       | @ $f_{CLK} = 5.4$ MHz                      | 20  | -   | -   | ns   |
| $t_{SCK}$     | CLK period                      | -                                          | 185 | -   | -   | ns   |
| $t_{CSSCK}$   | Clock inactive time after frame | -                                          | 600 | -   | -   | ns   |
| $t_{CSN}$     | CS de asserted time             | -                                          | 600 | -   | -   | ns   |

1. see Figure 17. SPI timing diagram
2. see Figure 16. SO loading for disable time measurement

**Figure 16. SO loading for disable time measurement**


GADG0412170958PS

**Figure 17. SPI timing diagram**


GADG0412171035PS

## 3 Functional description

### 3.1 Chip working conditions

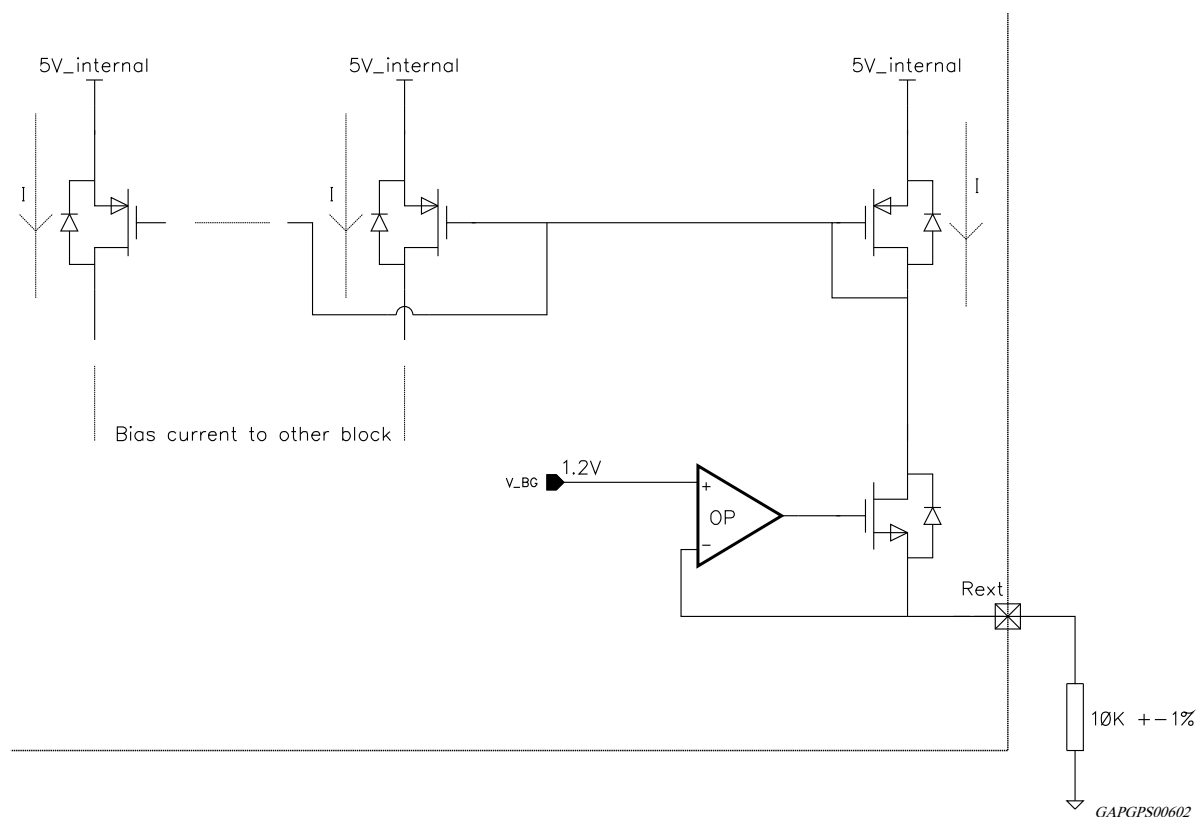
**Table 24. A outputs working conditions**

| -                             | Standby | Run mode | VB_OV   | VB_UV   | Reset             | Over current            | Thermal warning                               |
|-------------------------------|---------|----------|---------|---------|-------------------|-------------------------|-----------------------------------------------|
| VDD_SB regulator              | ON      | ON       | ON      | ON      | ON                | Current limitation      | ON                                            |
| VDD regulator                 | OFF     | ON       | OFF     | OFF     | ON                | Current limitation      | OFF if linked with VDD current limitation     |
| VDD_TRK regulator             | OFF     | ON       | OFF     | OFF     | ON                | Current limitation      | OFF if linked with VDD_TRK current limitation |
| All LS drivers                | OFF     | ON       | OFF     | OFF     | OFF               | Over current switch off | ON                                            |
| Diagnostics of all LS drivers | OFF     | ON       | OFF     | OFF     | ON <sup>(1)</sup> | -                       | ON                                            |
| HS Driver                     | OFF     | ON       | OFF     | OFF     | OFF               | Current limitation      | ON                                            |
| Stepper Motor Driver          | OFF     | ON       | OFF     | OFF     | OFF               | Over current switch off | ON                                            |
| K-line Transceiver            | OFF     | ON       | OFF     | OFF     | OFF               | Current limitation      | ON                                            |
| VRS                           | OFF     | ON       | OFF     | OFF     | OFF               | -                       | ON                                            |
| SPI                           | Default | Default  | Default | Default | Default           | ON                      | ON                                            |

1. The diagnostic currents and comparator are switched on in reset condition.

### 3.2 Chip bias current generation

The Internal current generator circuit is buffering internal band-gap voltage (1.2 V typ.) on a high precision external resistor (10 kΩ ±1 %) and generates an accurate current reference used to create all the chip bias currents.

**Figure 18. Current generator block diagram**


### 3.3 Power up/down sequences

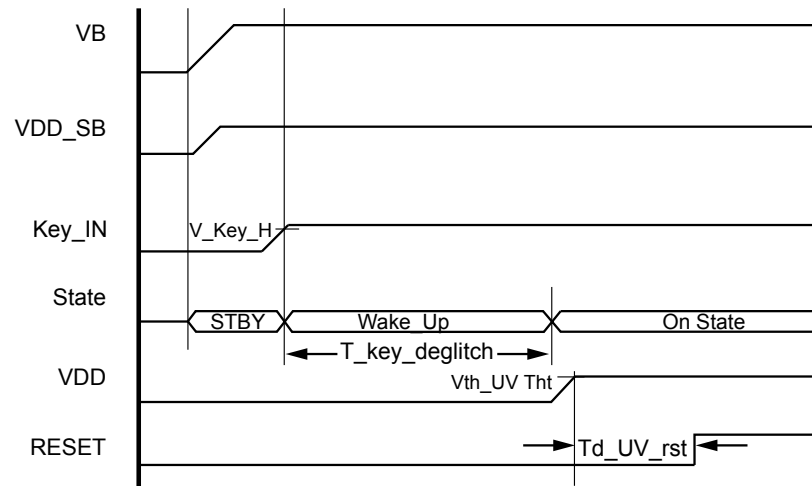
The figures below show the power-on, power-off and time diagram behaviour of the device.

VDD\_SB (standby voltage) rises together with battery input, and in standby it is always present if battery is present, no matter the KEY\_IN status.

When the KEY\_IN signal rises up and remains stable for at least  $T_{key\_deglitch}$  (see [Table 7](#)), the device goes in ON state, meaning that all voltage regulators and functions are active.

Wake-up is an intermediate status between standby and on mode, with current consumption higher than the standby one.

When Key\_IN goes low, device goes in OFF mode but standby regulator remains ON.

**Figure 19. Power-up sequence**


GAPGPS00603

**Figure 20. Power-down sequence**


GAPGPS00604

Reset signal detects a VDD undervoltage longer than TfUV\_reset by going to low level. When VDD recovers to normal level Reset signal returns to high level after Power\_On\_UV\_Reset\_Delay time (Td\_UV\_RST). The Reset signal resets all the internal SPI registers to default value.

## 3.4 SPI

SPI is a standard four wires interface, that communicates with a data word of 24 bits. By means of SPI all the channels can be driven in serial way and diagnosis is sent out. Timing of SPI's operations are reported in [Figure 17](#). The input data (DIN) is read on the rising edge of the SPI's clock (SCLK), in the same way the output data (DOUT) must be read by the Microcontroller on the SCLK's rising edge.

### 3.4.1 Data in (DIN)

DIN command is used to turn On/Off internal channels which do not have Parallel Input command, and to clear diagnostic latches.

DIN is decoded at the end of the frame if the integrity checks are passed.

Table 25. Data in (DIN) words content

| DIN23  | DIN22  | DIN21  | DIN20    | DIN19    | DIN18    | DIN17      | DIN16  |
|--------|--------|--------|----------|----------|----------|------------|--------|
| Mask   | L_0    | L_1    | VRS Diag | VRS Hys0 | VRS Hys1 | VRS Hys2   | 0      |
| DIN15  | DIN14  | DIN13  | DIN12    | DIN11    | DIN10    | DIN9       | DIN8   |
| INJ1_0 | INJ1_1 | INJ2_0 | INJ2_1   | O2H_0    | O2H_1    | RLY1_0     | RLY1_1 |
| DIN7   | DIN6   | DIN5   | DIN4     | DIN3     | DIN2     | DIN1       | DIN0   |
| RLY2_0 | RLY2_1 | RLY3_0 | RLY3_1   | TACH_0   | TACH_1   | Clear diag | Parity |

**Data in structure (MSB first)**

- **Mask** bit is used to mask serial command for diagnosis only readings on DOUT:
- 0 - Read Diag. All DIN bits are ignored.
- 1 - Write. All DIN are transferred into the internal registers.
- **Command** bits are used to control the output drivers: (INJ1-2, O2H, RLY1-2-3, L and TACH) as described in the following table:

Table 26. Data in command bits structure

| xxx_0 | xxx_1 | Description                                                 |
|-------|-------|-------------------------------------------------------------|
| 0     | 1     | Turn-off driver / parallel polarity 0                       |
| 1     | 1     | Turn-on driver / parallel polarity 1                        |
| X     | 0     | No change (the driver will maintain the previous condition) |

- **VRS Diag** bit is used active high to enable diagnostic phase of VRS block, the diagnosis can be done only when the phonic wheel is stopped.
- Programmable VRS Hysteresis: VRS hysteresis is programmable in 5 steps according to [Table 27](#).
- **Clear Diag**, when set to 1 generates a request to clear those diagnostic flags which are latched.
- In addition **odd parity bit** (that is the last bit of the frame and includes in its calculation the "Don't care" bits) is used for DIN word check together with falling clock edges count.

Table 27. Data in VRS hysteresis

| Hys 0 | Hys 1 | Hys 2 | Description                    |
|-------|-------|-------|--------------------------------|
| 0     | 0     | 0     | Auto adaptive hysteresis       |
| 1     | 0     | 0     | Hys VRS = 100 mV               |
| 0     | 1     | 0     | Hys VRS = 200 mV               |
| 1     | 1     | 0     | Hys VRS = 350 mV               |
| 0     | 0     | 1     | Hys VRS = 650 mV               |
| 1     | 0     | 1     | Hys VRS = 1000 mV              |
| 1     | 1     | 1     | Not Valid (Hys doesn't change) |

**3.4.2****Data out (DOUT)**

Status flags are sampled and sent out through DOUT pin at each R/W SPI operation. The structure of the 24 bit word is described in [Table 28](#). A three bits diagnosis is provided for stepper motor driver, a two bit diagnosis for

other drivers. VRS diagnosis is coded as '0' means No Fault, while '1' means Fault. Over temperature warning is coded as '0' means No Fault, while '1' means Fault.  
The SPI default value is: all bits set to zero.

**Table 28. Data out (DOUT) words content**

| DOUT23     | DOUT22          | DOUT21      | DOUT20      | DOUT19      | DOUT18      | DOUT17      | DOUT16      |
|------------|-----------------|-------------|-------------|-------------|-------------|-------------|-------------|
| INJ1 Diag0 | INJ1 Diag1      | INJ2 Diag0  | INJ2 Diag1  | O2H Diag0   | O2H Diag1   | RLY1 Diag0  | RLY1 Diag1  |
| DOUT15     | DOUT14          | DOUT13      | DOUT12      | DOUT11      | DOUT10      | DOUT9       | DOUT8       |
| RLY2 Diag0 | RLY2 Diag1      | RLY3 Diag0  | RLY3 Diag1  | L Diag0     | L Diag1     | TACH Diag0  | TACH Diag1  |
| DOUT7      | DOUT6           | DOUT5       | DOUT4       | DOUT3       | DOUT2       | DOUT1       | DOUT0       |
| VRS Diag   | Thermal Warning | Brdg1 Diag0 | Brdg1 Diag1 | Brdg1 Diag2 | Brdg2 Diag0 | Brdg2 Diag1 | Brdg2 Diag2 |

#### Data out structure

**Table 29. Two bits diagnosis (normal drivers)**

| Bit 0 | Bit 1 | Fault                 |
|-------|-------|-----------------------|
| 0     | 0     | No Fault              |
| 1     | 0     | Short to Ground (OFF) |
| 0     | 1     | Open Load (OFF)       |
| 1     | 1     | Overcurrent (ON)      |

**Table 30. Three bits diagnosis (bridge stage)**

| Bit 0 | Bit 1 | Bit 2 | Fault                 |
|-------|-------|-------|-----------------------|
| 0     | 0     | 0     | No Fault              |
| 1     | 0     | 0     | Short to Ground (OFF) |
| 1     | 0     | 1     | Short to VBAT (OFF)   |
| 0     | 1     | 0     | Open Load (OFF)       |
| 1     | 1     | 0     | Overcurrent (ON)      |

## 3.5 Diagnosis

The device provides a full set of diagnosis; deglitch timings listed below are digital, generated from internal clock and their accuracy is guaranteed by scan patterns and clock measurement.

### 3.5.1 Voltage regulators thermal warning and shutdown

The 5V linear voltage regulator/tracking regulator is shut down when the thermal shutdown temperature is reached and also the regulator is in current limitation. The shutdown is filtered with Tdcg filter of 30  $\mu$ s  $\pm$ 25 %. As soon as the over temperature disappears the regulator is switched on again. Over temperature flag without any latch is present via SPI.

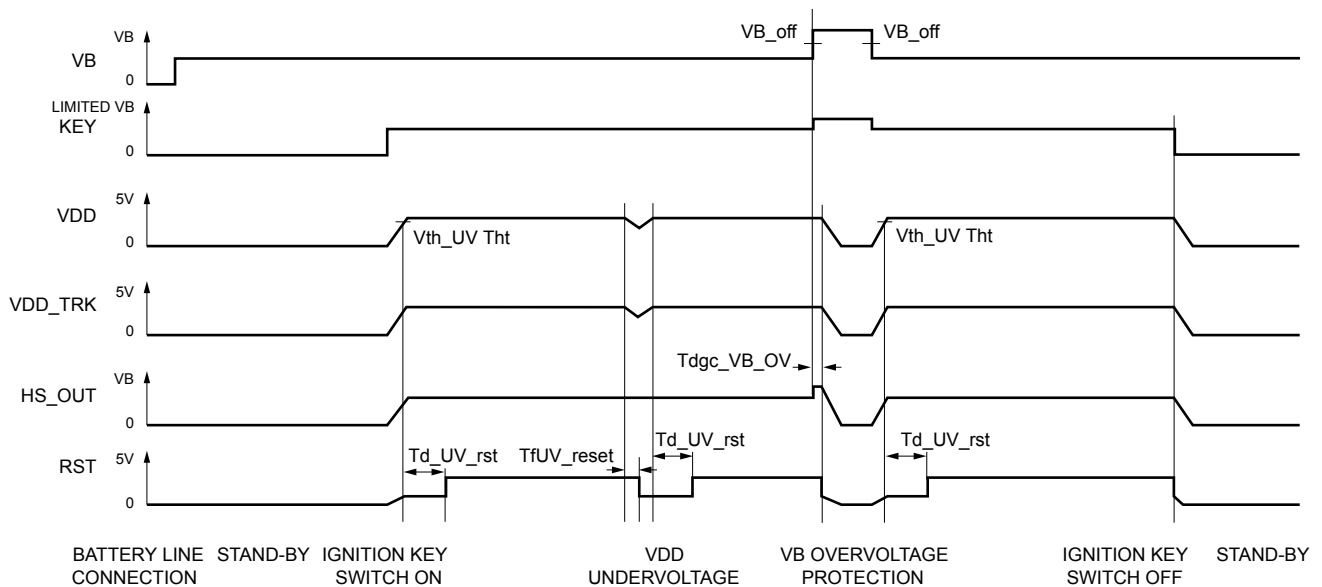
### 3.5.2 Overvoltage shut down

If the VB\_off voltage is reached after Tdgc filtering time of 30  $\mu$ s  $\pm$ 25 % the device enters a safety state where the main outputs are switched-off. Voltage regulators, all low side channels, stepper motor driver and KLINE are switched off and reset is asserted. As soon as the battery goes below VB\_off minus VB\_off\_h the device recovers standard operation.

### 3.5.3 Undervoltage shut down

If the VB\_UV voltage is reached after analog Tdgc 1  $\mu$ s  $\pm$ 20 % filtering time the device enters a safety state where main outputs are switched-off. Voltage regulators, all low side channels, stepper motor driver and KLINE are switched off. As soon as the battery rises above VB\_UV plus the hysteresis the device recovers normal operation.

**Figure 21. An example of under and over voltage time diagram**



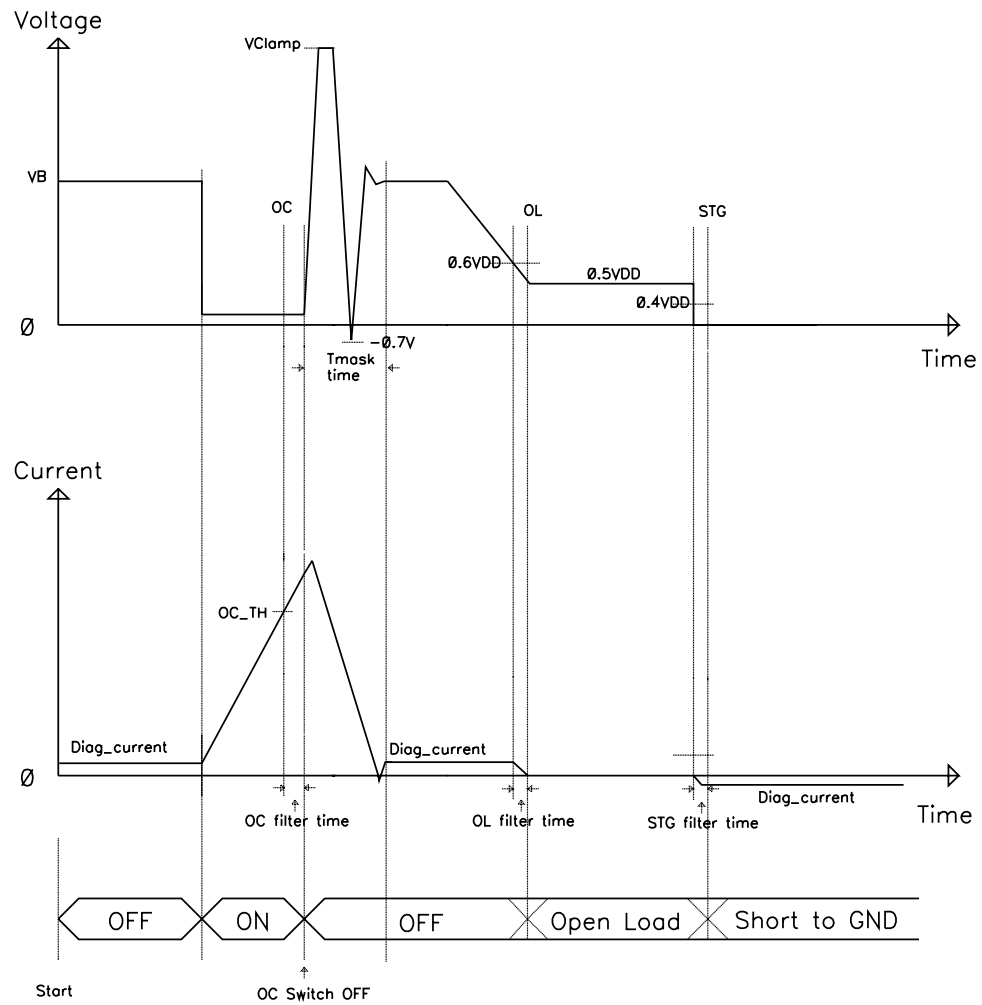
GADG0412171117PS

### 3.5.4 Low side on/off diagnosis (INJ, RLY's, TACH, O2H)

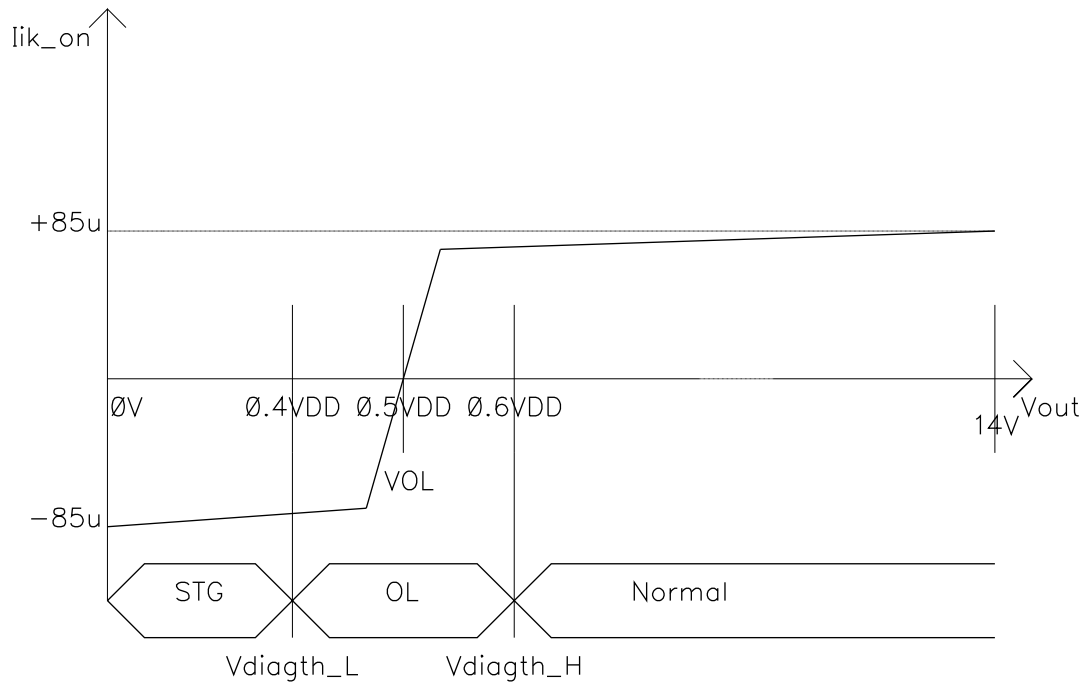
About low side channels OFF diagnosis, the device issues a masking filter Tmask after channel turning off (falling edge of driving command) to avoid false fault detecting due to output transition from low to high. Tmask is of 1 ms  $\pm$ 25 % for all channels except for the relays, for which Tmask is 3.5 ms  $\pm$ 25 %. Once masking time has expired a deglitch filter Tdgc\_noise of 3.6  $\mu$ s  $\pm$ 40 % for noise immunity is activated. A fault longer than deglitch time is latched. OFF state diagnostic fault can be overwritten by ON state fault. OFF state fault does not prevent the driver from switching on. The latched fault is cleared on request.

During on-phase if an over current fault occurs the drivers enter in current limitation condition for a digital filtering time Tdgc of 20  $\mu$ s  $\pm$ 25 %, then it is switched OFF and the fault is latched. The channel is turned ON again by input command transition. The latched fault is cleared on request via SPI.

Over current fault has higher priority respect to OFF condition faults.

**Figure 22. Low side driver diagnosis time diagram**


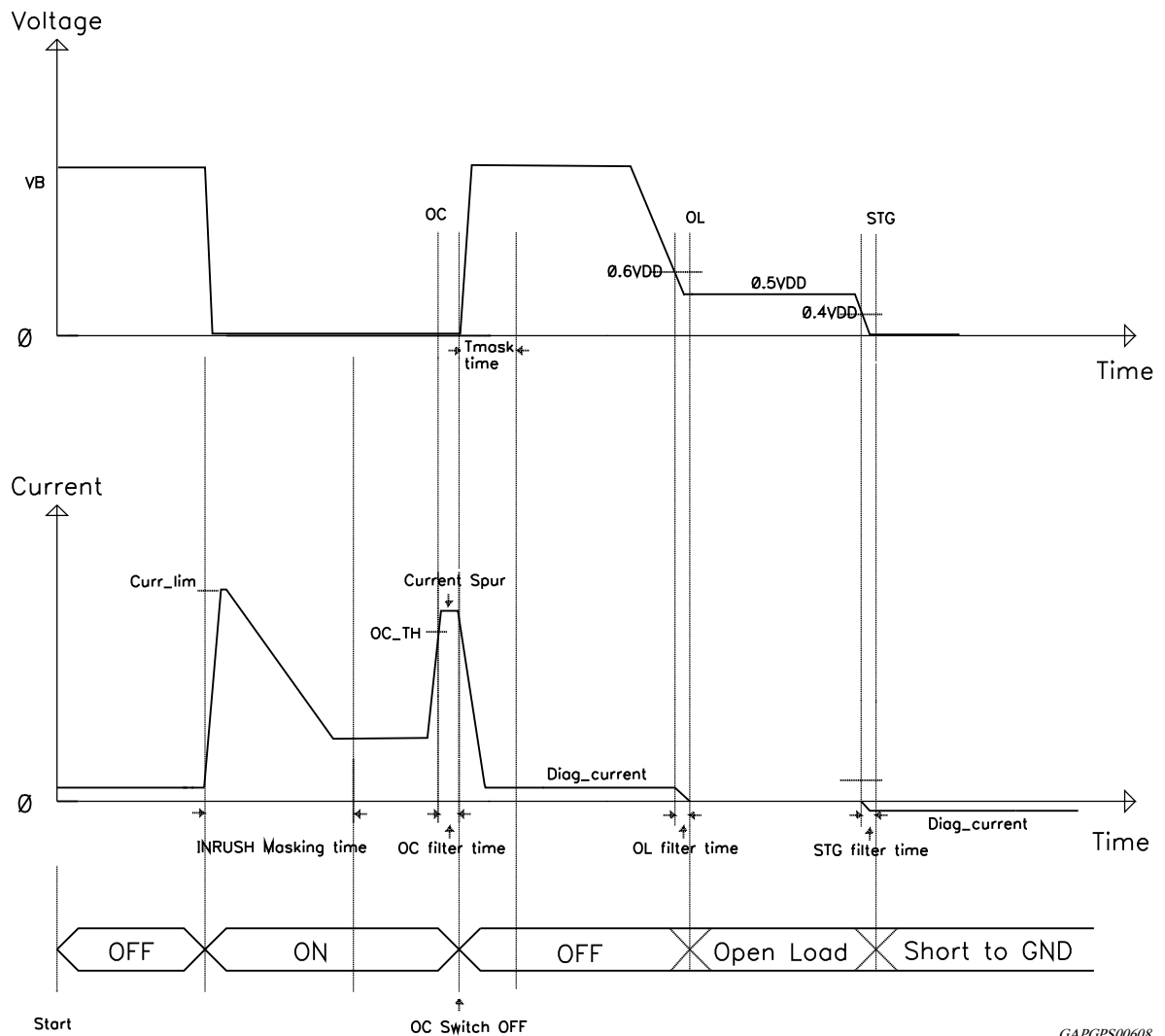
GAPGPS00606

**Figure 23. Low side driver diagnosis I-V relationship**


GAPGPS00607

### 3.5.5 Current limited low side driver on/off diagnosis

In OFF condition diagnosis is the same as Low side, with Tmask 3.5 ms  $\pm$  25 % and Tdgc\_noise 3.6  $\mu$ s  $\pm$  40 %, while in ON condition initial Inrush current is masked for Tmask\_rush of 336  $\mu$ s  $\pm$  25 % then, if an over current fault occurs the drivers enter in current limitation condition for a digital filtering time Tdgc of 20  $\mu$ s  $\pm$  25 %, then it is switched OFF and the fault is latched. The channel is turned ON again by input command transition. The latched fault is cleared on request via SPI. Over current fault has higher priority with respect to OFF condition faults.

**Figure 24. Current limited low side driver diagnosis time diagram**


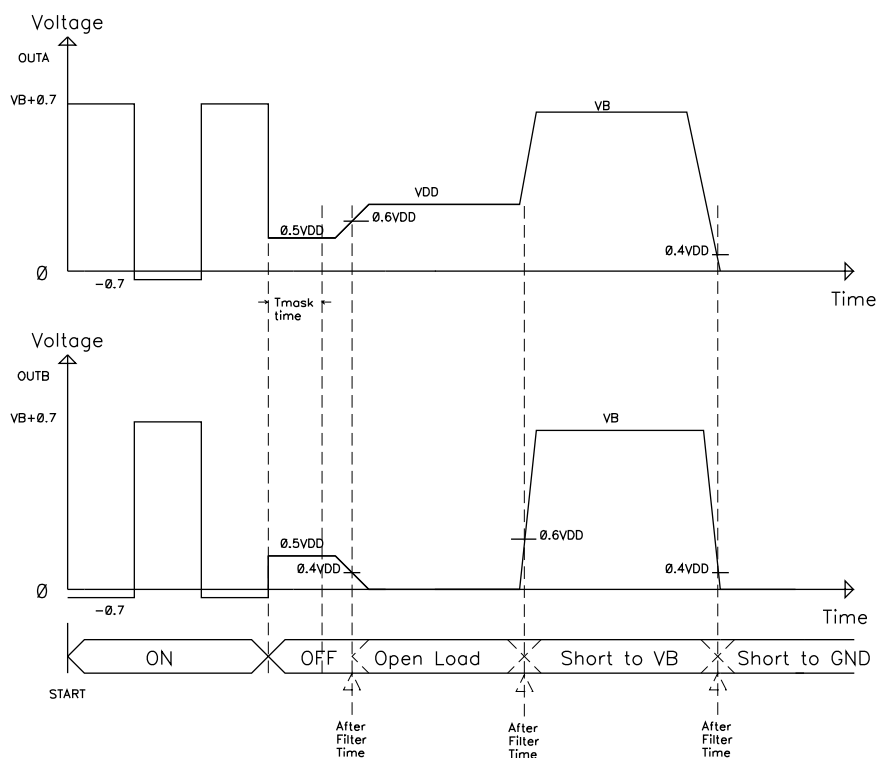
GAPGPS00608

### 3.5.6 Stepper motor driver OFF diagnosis (EN signal low and output in high impedance state)

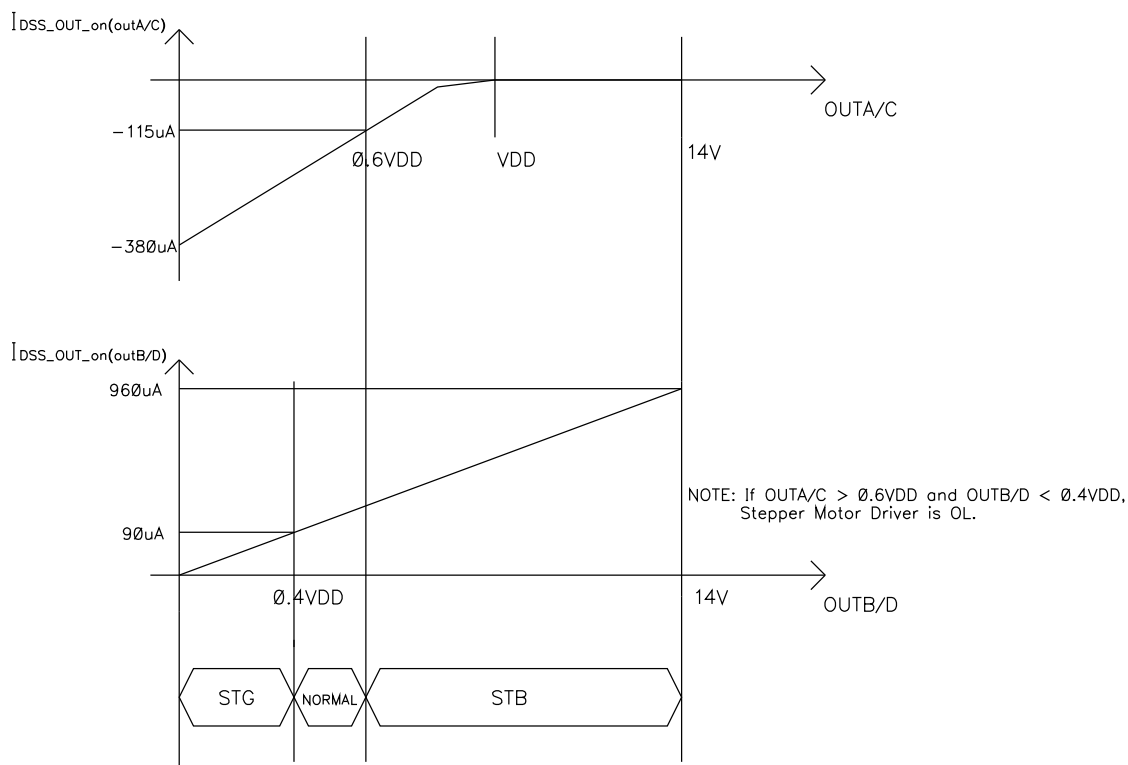
In OFF condition Short to GND/Short to VB or Open Load condition is continuously detected through a deglitch filter of  $125 \mu\text{s} \pm 25\%$ , after  $T_{\text{mask}}$  masking time of  $1 \text{ ms} \pm 25\%$  to filter ON/ OFF transition. To avoid false diagnostic due to motor residual movement, the stepper has to be disabled at least 40 ms after the PWL signal has been disabled. A fault longer than deglitch time is latched. OFF state diagnostic fault can be overwritten by ON state fault. OFF state fault does not prevent the stepper from switching on. The latched fault is cleared on request.

### 3.5.7 Stepper motor driver ON diagnosis (EN signal high and output driven by input commands)

In ON condition when over current fault is detected and validated after digital filtering time  $T_{\text{dgc}}$  of  $20 \mu\text{s} \pm 25\%$ , the bridge is turned OFF and the fault is latched. The bridge is turned ON again by input command EN transition. The latched fault is cleared on request. Over current fault has higher priority with respect to OFF condition faults. Each Bridge has dedicated fault diagnosis detection coded by three bits.

**Figure 25. Stepper motor driver diagnosis time diagram**


GAPGPS00609

**Figure 26. Stepper motor driver diagnosis I-V relationship**


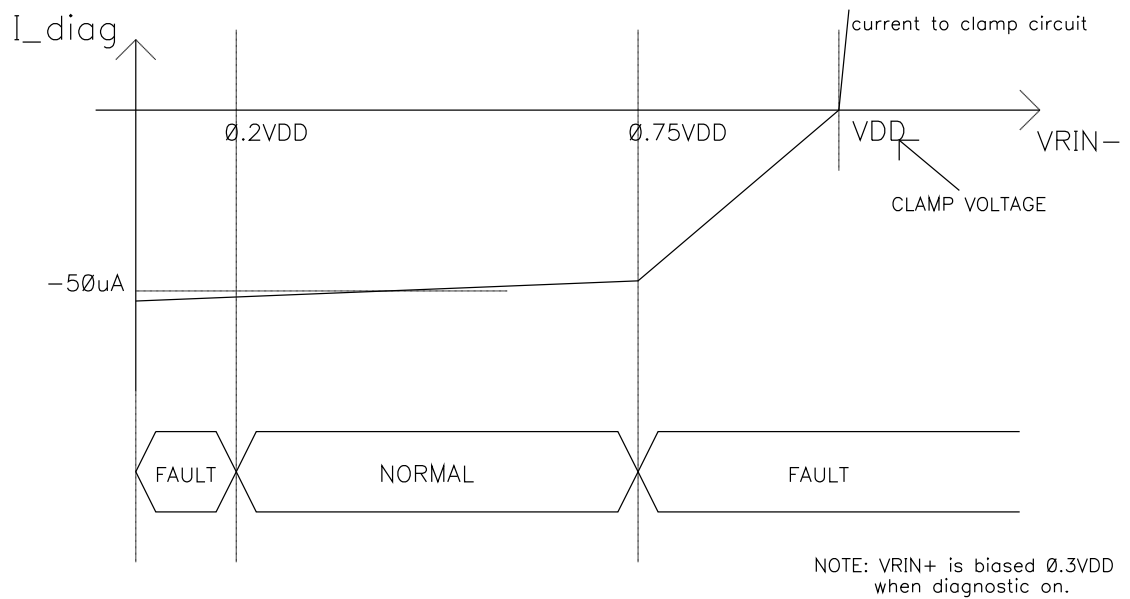
H-Bridge diagnostic I\_V plot(TYP)

GAPGPS00610

### 3.5.8 VRS diagnosis

VRS block enters diagnosis phase on request via SPI and then generates a Fault bit. If the fault exceeds the  $T_{dgc}$  filter time of  $30\ \mu s \pm 20\%$ , it is latched. The latched fault is cleared on request via SPI. The VRS diagnostic can only be activated when the phonic wheel is in stop condition.

**Figure 27. VRS diagnosis I-V relationship**



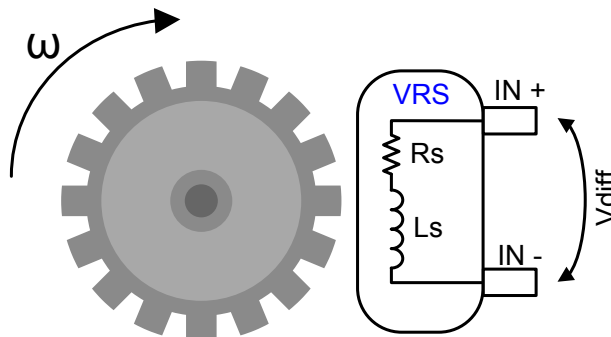
GAPGPS00611

## 3.6 VRS interface

### 3.6.1 Function characteristic

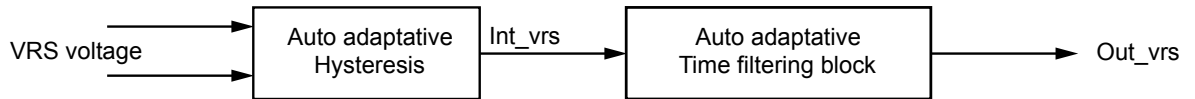
The flying wheel interface is an interface between the  $\mu P$  and the flying wheel sensor: it conditions signal coming from magnetic pick-up sensor or hall effect sensor and feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

**Figure 28. VRS typical characteristics**



GAPGPS00571

**Figure 29. VRS interface structure**

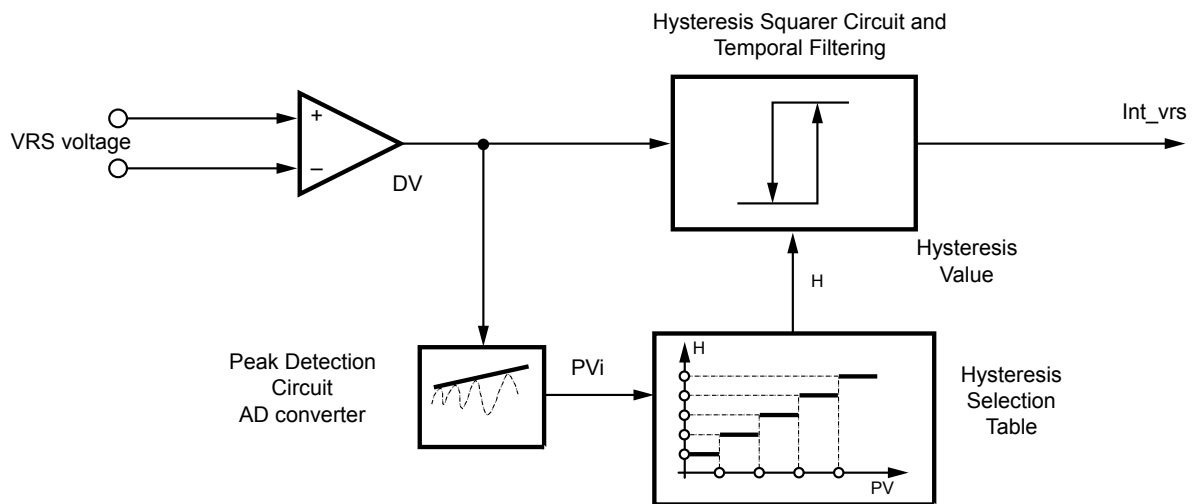


GAPGPS00612

### 3.6.2 Auto-adaptative hysteresis

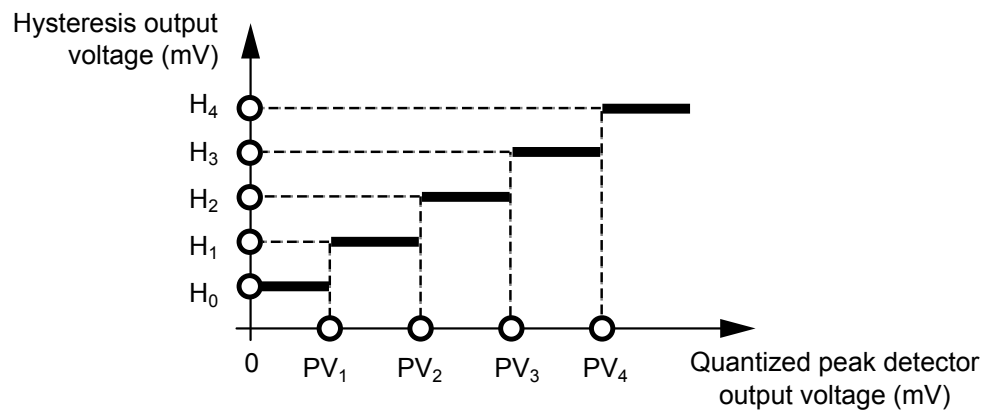
Input signals difference is obtained through a full differential amplifier; its output, DV signal, is fed to peak detection circuit and then to A/D converter implemented with 4 voltage comparator (5 levels Pvi). Output of A/D is sent to Logic block (hysteresis selection Table 32) that implements correlation function between Peak voltage and hysteresis value; hysteresis value is used by square filtering circuit which conditions DV signal.

**Figure 30. Auto-adaptive hysteresis block diagram**



GAPGPS00613

**Figure 31. Hysteresis output voltage level**



GAPGPS00614

To the previous 5 levels  $PV = [0 \text{ PV1 } PV2 \text{ PV3 } PV4]$  correspond to a set of 5 thresholds:

- $H = [H0 \text{ H1 } H2 \text{ H3 } H4]$

The advised values for the previous defined vectors are:

- $PV = [0 \text{ PV1 } PV2 \text{ PV3 } PV4] = [0, 900, 1560, 2230, 2900] \text{ mV}$
- $H = [H0 \text{ H1 } H2 \text{ H3 } H4] = [100, 200, 350, 650, 1000] \text{ mV}$

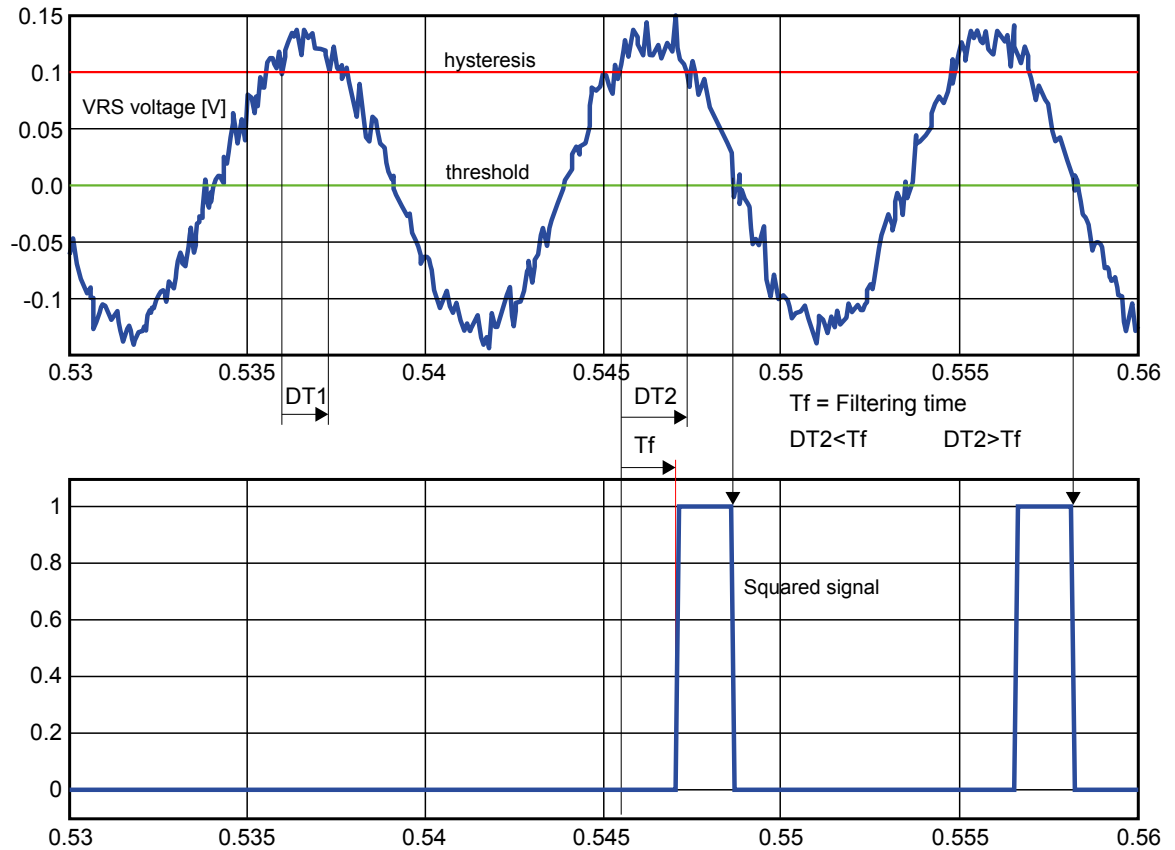
**Table 31. Peak voltage detector precision**

| Pick voltage [PV] | Value |      |      | Unit |
|-------------------|-------|------|------|------|
|                   | Min.  | Typ. | Max. |      |
| PV1               | 850   | 900  | 950  | mV   |
| PV2               | 1452  | 1560 | 1638 | mV   |
| PV3               | 2118  | 2230 | 2341 | mV   |
| PV4               | 2755  | 2900 | 3045 | mV   |

**Table 32. Hysteresis threshold precision**

| Pick voltage [PV] | Value |      |      | Unit |
|-------------------|-------|------|------|------|
|                   | Min.  | Typ. | Max. |      |
| H0                | 70    | 100  | 130  | mV   |
| HV1               | 140   | 200  | 220  | mV   |
| HV2               | 250   | 347  | 390  | mV   |
| HV3               | 490   | 644  | 720  | mV   |
| HV4               | 730   | 1000 | 1120 | mV   |

**Note:** Hysteresis voltages are achieved by injecting an hysteresis bias current on  $V_{RIN\pm}$  external resistors (typ. 10 k $\Omega$  each, see [Figure 38](#)). The resulting HV voltage is  $HV = I_{hys} * R_{typ}$ . Changing the value of R the hysteresis value would change in a linear mode.

**Figure 32. Input-output behaviour of VRS interface**


GAPGPS00615

### 3.6.3 Auto-adaptative time filter

This characteristic is useful to set the best internal filter time as function of the input signal frequency.

The Tfilter time depends on the previous period duration Tn according to the following formula:

$$T_{\text{filter}}(n+1) = 1/32 * T_n \text{ if } T_n > T_{\text{filter}}(n)$$

The filtering time purpose is to filter very short spikes.

The digital filtering time is applied to internal squared signal (int\_vrs), obtained by voltage comparators.

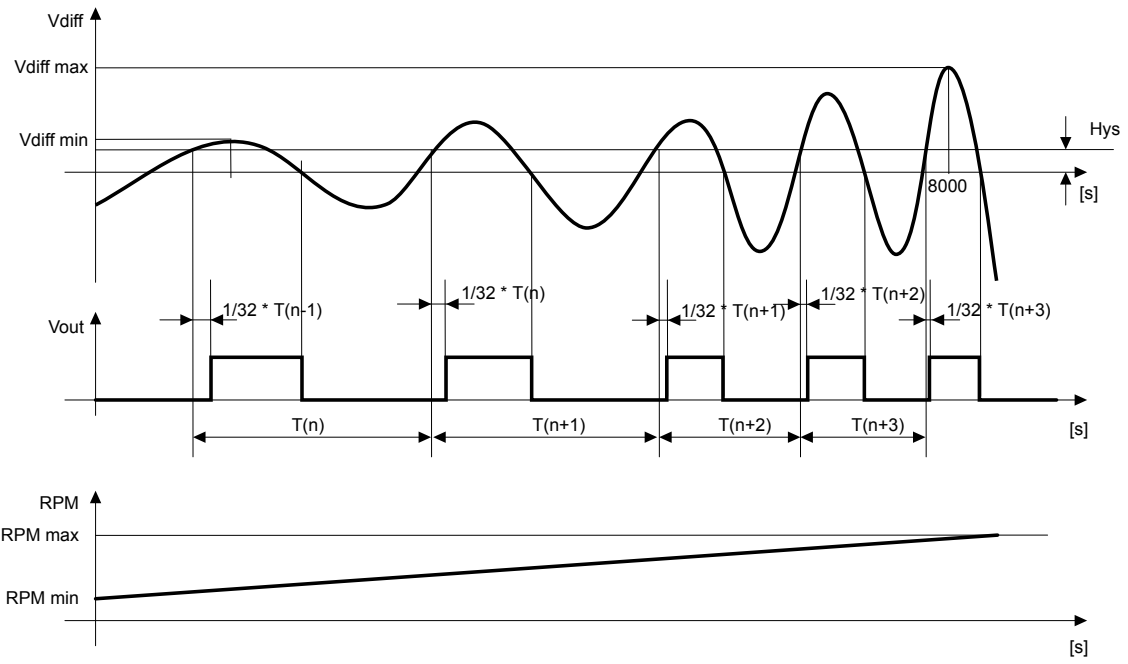
The output of time filtering block is out\_vrs signal.

The filtering time Tfilter is applied to int\_vrs signal in two different ways:

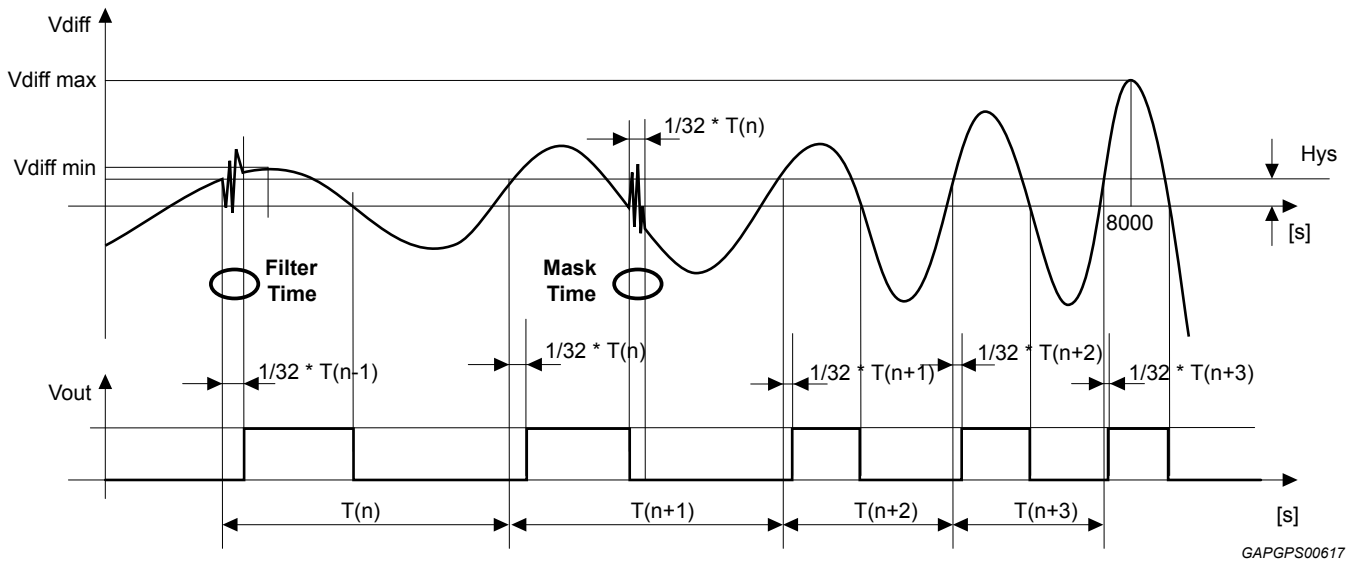
- Rising edge: if int\_vrs high level lasts less than Tfilter, out\_vrs is not set to high level.
- In absence of any spikes during input signal rising edge out\_vrs signal is expected with a delay of Tfilter time.
- Falling edge: the falling edge of int\_vrs is not delayed through time filtering block: after falling edge for a time Tfilter any other transition on int\_vrs signal is ignored

The initial value (Default) and maximum for Tfilter must be considered at RPM\_min = 20 e.g. Tmax filter = 180 µs. The minimum available value is Tmin filter = 2.8 µs.

**Figure 33. Auto-adaptative time filter behaviour 1**



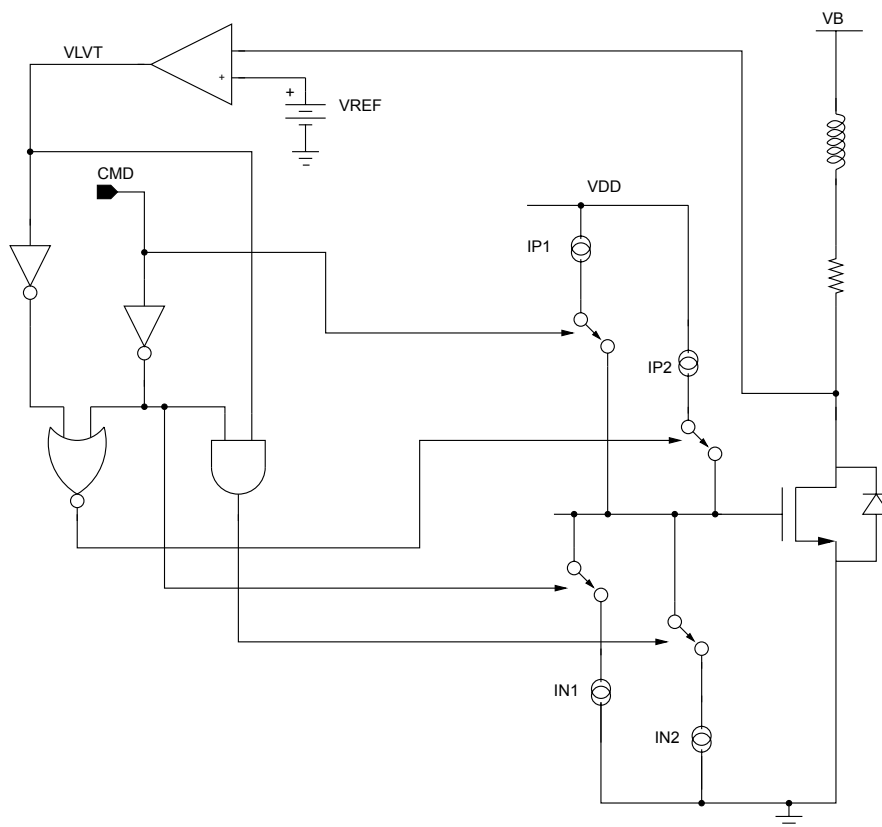
**Figure 34. Auto-adaptative time filter behaviour 2**



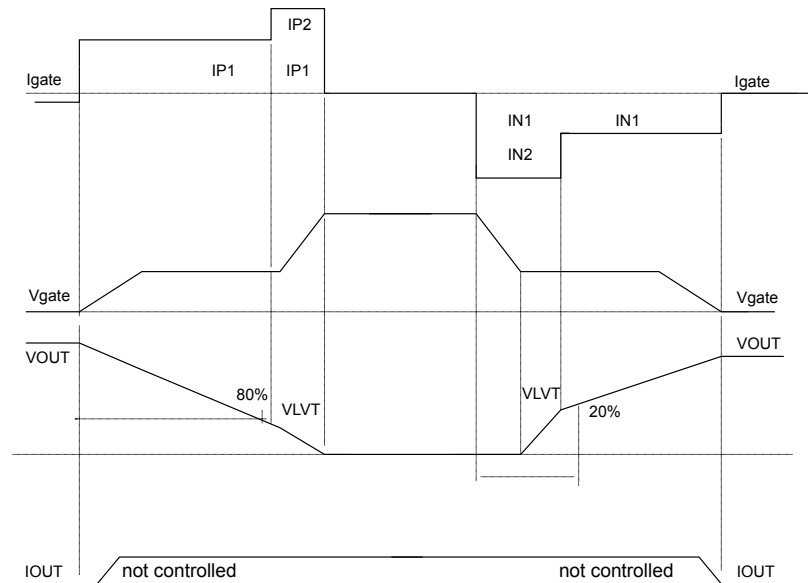
## 4 Low side drivers

Low side drivers have a voltage slew rate control during switch-on/off phase to reduce emissions. The slew-rate control is achieved controlling the gate charging current and the behavior is described in [Figure 35](#) and [Figure 36](#).

**Figure 35. Low side drivers slew rate implementation**



GAPGPS00618

**Figure 36. Low side drivers slew rate**


GAPGPS00619

At switch-on command the charging current is provided by current generator  $IP1$  and is kept constant until the output voltage is decreased of roughly 80% of typical battery level. At this point the low side transistor is on and  $VLVT$  signal is set to logic 1 to connect  $IP2$  current generator in parallel with  $IP1$ , completing the gate charge curve and providing maximum gate drive.

When the power transistor is switched-off the gate is discharged quickly using both  $IN1$  and  $IN2$  currents; as soon as the output voltage reaches roughly 20 % of the nominal battery voltage only  $IN1$  is kept connected to complete the gate discharging.

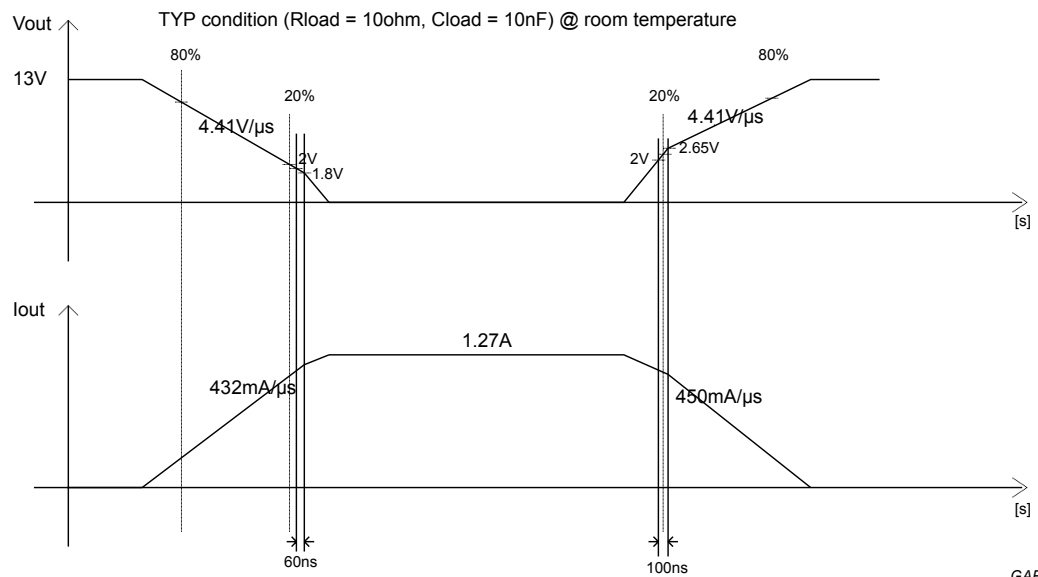
In [Table 33](#) the values for  $IPx$  and  $INx$  current generators are reported for each low side.

As an example [Figure 37](#) shows the resulting slew rate, in typical conditions, of O2H low side driver.

**Table 33. Values for  $IPx$  and  $INx$  current generators for each low side**

| Low side | $IP1$ | $IP2$ | $IN1$ | $IN2$ | Unit    |
|----------|-------|-------|-------|-------|---------|
| O2H      | 243   | 81    | 253   | 337   | $\mu A$ |
| INJ      | 174   | 23    | 180   | 124   | $\mu A$ |
| RLY's    | 78    | 0     | 80    | 120   | $\mu A$ |
| L        | 78    | 0     | 62    | 119   | $\mu A$ |
| TACH     | 22    | 0     | 21    | 25    | $\mu A$ |

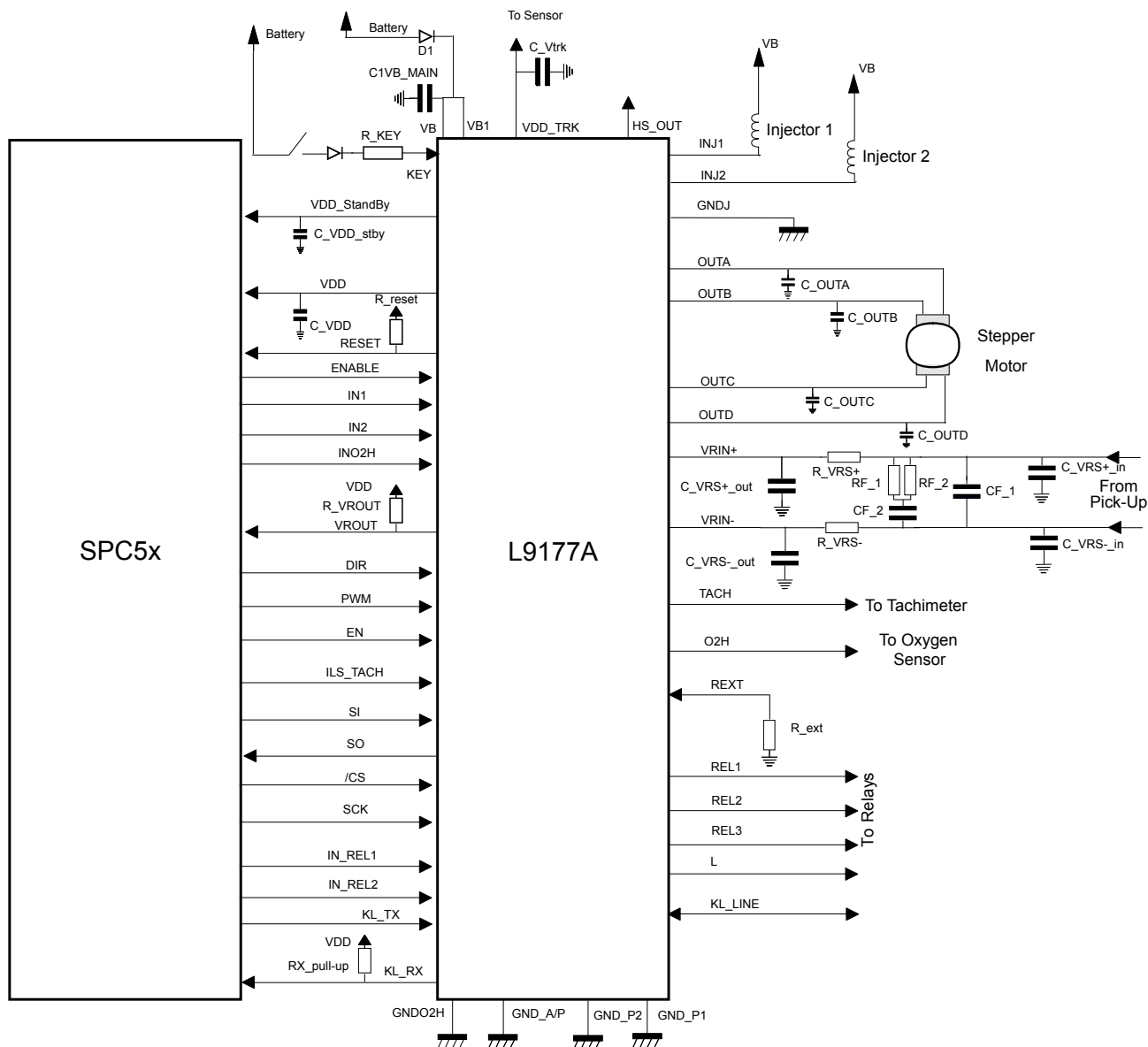
**Figure 37. O2H low side driver slew rate**



GAPGPS00620

## 5 Application circuit

**Figure 38. Application circuit**



GAPG1303150713PS

### 5.1 Bill of material

**Table 34. Bill of material**

| Block  | Component | Name      | Usage                                 | Min | Typ | Max | Unit |
|--------|-----------|-----------|---------------------------------------|-----|-----|-----|------|
| Supply | Capacitor | C1VB_MAIN | Bulk capacitor                        |     | 220 |     | μF   |
|        | Diode     | D1        | Reverse polarization protection diode |     |     |     |      |
| Key    | Resistor  | R_Key     | Current limiting resistor             |     | 20  |     | kΩ   |

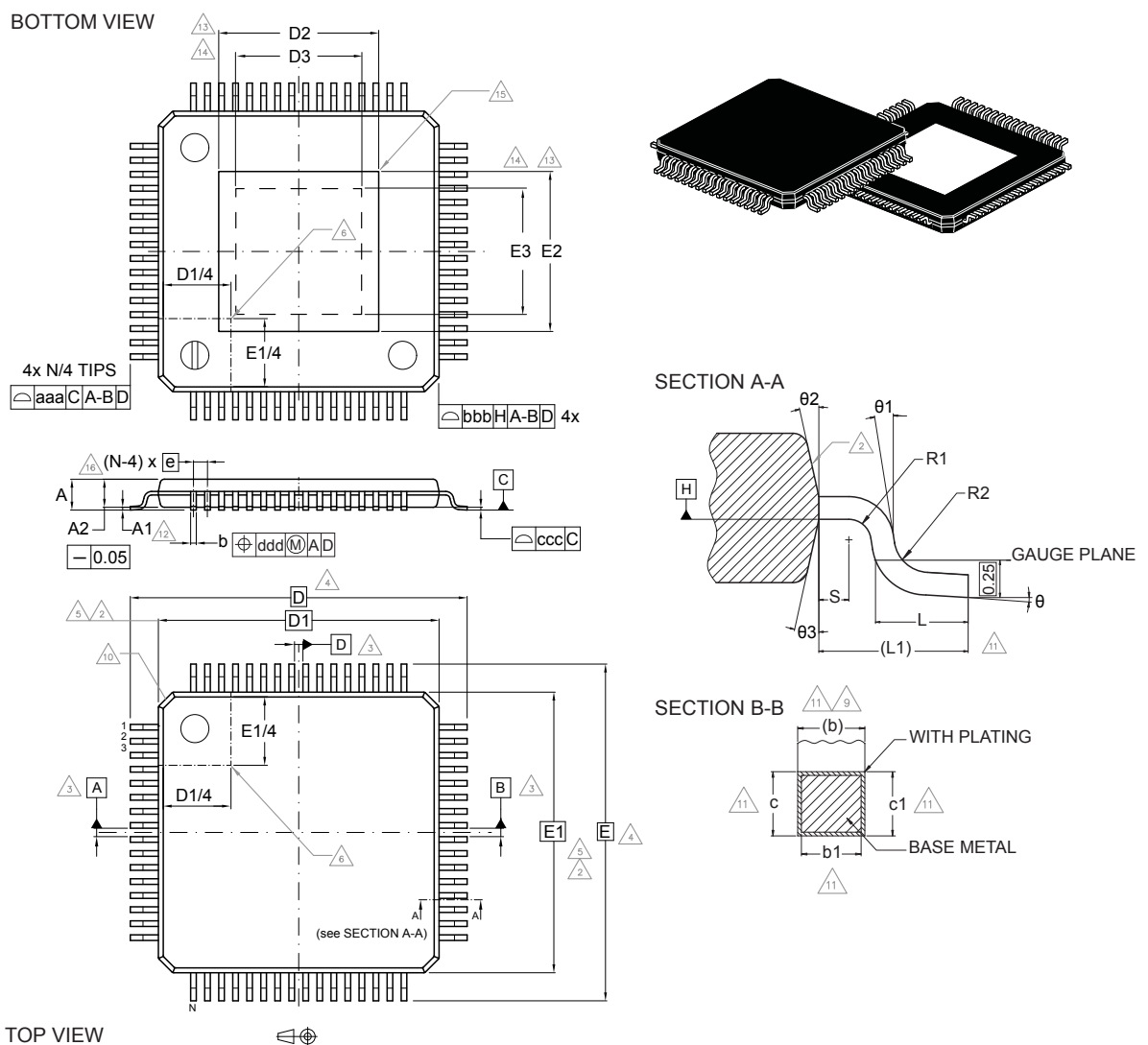
| Block   | Component | Name             | Usage                                  | Min | Typ     | Max | Unit |
|---------|-----------|------------------|----------------------------------------|-----|---------|-----|------|
| Rext    | Resistor  | R_ext            | Pull-up resistor                       |     | 10 (1%) |     | kΩ   |
| Reset   | Resistor  | R_reset          | Pull-up resistor                       |     | 1       |     | kΩ   |
| VDD     | Capacitor | C_VDD value      | Output capacitor (Ceramic or Tantalum) | 4.7 |         | 60  | μF   |
|         |           | C_VDD ESR        |                                        |     |         | 1.5 | Ω    |
| VDD_trk | Capacitor | C_Vtrk value     | Output capacitor                       | 2.2 |         | 100 | μF   |
|         |           | C_Vtrk ESR       |                                        | 10  |         | 100 | mΩ   |
| Vdd_sby | Capacitor | C_VDD_stby value | Output capacitor                       | 1   |         | 10  | μF   |
|         |           | C_VDD_stby ESR   |                                        |     |         | 200 | mΩ   |
| VRS     | Capacitor | C_VRS+_in        | Filter Capacitor                       |     |         | 100 | pF   |
| VRS     | Capacitor | C_VRS-_in        | Filter Capacitor                       |     |         | 100 | pF   |
| VRS     | Capacitor | C_VRS+_out       | Filter Capacitor                       |     |         | 470 | pF   |
| VRS     | Capacitor | C_VRS-_out       | Filter Capacitor                       |     |         | 470 | pF   |
| VRS     | Resistor  | R_VRS+           | Current limiting resistor              |     |         | 10  | kΩ   |
| VRS     | Resistor  | R_VRS-           | Current limiting resistor              |     |         | 10  | kΩ   |
| VRS     | Capacitor | CF_1             | Filter Capacitor                       |     |         | 470 | pF   |
| VRS     | Capacitor | CF_2             | Filter Capacitor                       |     |         | 100 | nF   |
| VRS     | Resistor  | RF_1             | Filter resistor                        |     |         | 33  | kΩ   |
| VRS     | Resistor  | RF_2             | Filter resistor                        |     |         | 33  | kΩ   |
| VRS     | Resistor  | R_VROUT          | Pull-up resistor                       |     | 10      |     | kΩ   |
| K-Line  | Resistor  | RX_pull-up       | Pull-up resistor                       |     |         | 2   | kΩ   |
| Stepper | Capacitor | C_OUTA           | EMI filter capacitor                   |     |         | 10  | nF   |
| Stepper | Capacitor | C_OUTB           | EMI filter capacitor                   |     |         | 10  | nF   |
| Stepper | Capacitor | C_OUTC           | EMI filter capacitor                   |     |         | 10  | nF   |
| Stepper | Capacitor | C_OUTD           | EMI filter capacitor                   |     |         | 10  | nF   |

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 6.1 TQFP64 (10x10x1 mm exp. pad down) package information

**Figure 39. TQFP64 (10x10x1 mm exp. pad down) package outline**



7278840\_Rev9.0\_PkgCode\_9I

GAPGPS03451

**Table 35. TQFP64 (10x10x1 mm exp. pad down) package mechanical data**

| Ref                            | Min.           | Typ.      | Max. | Note<br>(see # in Notes below) |
|--------------------------------|----------------|-----------|------|--------------------------------|
| Θ                              | 0°             | 3.5°      | 7°   | -                              |
| Θ1                             | 0°             | -         | -    | -                              |
| Θ2                             | 11°            | 12°       | 13°  | -                              |
| Θ3                             | 11°            | 12°       | 13°  | -                              |
| A                              | -              | -         | 1.2  | 15                             |
| A1                             | 0.05           | -         | 0.15 | 12                             |
| A2                             | 0.95           | 1         | 1.05 | 15                             |
| b                              | 0.17           | 0.22      | 0.27 | 9, 11                          |
| b1                             | 0.17           | 0.2       | 0.23 | 11                             |
| c                              | 0.09           | -         | 0.2  | 11                             |
| c1                             | 0.09           | -         | 0.16 | 11                             |
| D                              | -              | 12.00 BSC | -    | 4                              |
| D1                             | -              | 10.00 BSC | -    | 5, 2                           |
| D2                             | See VARIATIONS |           |      | 13                             |
| D3                             | See VARIATIONS |           |      | 14                             |
| e                              | -              | 0.50 BSC  | -    | -                              |
| E                              | -              | 12.00 BSC | -    | 4                              |
| E1(*)                          | -              | 10.00 BSC | -    | 5, 2                           |
| E2                             | See VARIATIONS |           |      | 13                             |
| E3                             | See VARIATIONS |           |      | 14                             |
| L                              | 0.45           | 0.6       | 0.75 | -                              |
| L1                             | -              | 1.00 REF  | -    | -                              |
| N                              | -              | 64        | -    | 16                             |
| R1                             | 0.08           | -         | -    | -                              |
| R2                             | 0.08           | -         | 0.2  | -                              |
| S                              | 0.2            | -         | -    | -                              |
| Tolerance of form and position |                |           |      |                                |
| aaa                            | -              | 0.2       | -    | 1, 7                           |
| bbb                            | -              | 0.2       | -    |                                |
| ccc                            | -              | 0.08      | -    |                                |
| ddd                            | -              | 0.08      | -    |                                |
| VARIATIONS                     |                |           |      |                                |
| Pad option 4.3 x 4.3 (T3)      |                |           |      |                                |
| D2                             | -              | -         | 4.65 | 13, 14                         |
| E2                             | -              | -         | 4.65 |                                |
| D3                             | 2.90           | -         | -    |                                |
| E3                             | 2.90           | -         | -    |                                |
| Pad option 4.5 x 4.5 (T1-T3)   |                |           |      |                                |

| Ref                       | Min. | Typ. | Max. | Note<br>(see # in Notes below) |
|---------------------------|------|------|------|--------------------------------|
| D2                        | -    | -    | 4.98 | 13, 14                         |
| E2                        | -    | -    | 4.98 |                                |
| D3                        | 3.29 | -    | -    |                                |
| E3                        | 3.29 | -    | -    |                                |
| Pad option 6.0 x 6.0 (T3) |      |      |      |                                |
| D2                        | -    | -    | 6.40 | 13, 14                         |
| E2                        | -    | -    | 6.40 |                                |
| D3                        | 4.80 | -    | -    |                                |
| E3                        | 4.80 | -    | -    |                                |
| Pad option 7.5 x 7.5 (T1) |      |      |      |                                |
| D2                        | -    | -    | 7.60 | 13, 14                         |
| E2                        | -    | -    | 7.60 |                                |
| D3                        | 7.30 | -    | -    |                                |
| E3                        | 7.30 | -    | -    |                                |

#### Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. "N" is the number of terminal positions for the specified body size.

## Revision history

**Table 36. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20-Sep-2017 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 29-Sep-2017 | 2        | <p>Updated Table 1. Pin function pin 27 column "Class" from SIGNAL to PWR;</p> <p>Updated Section 2.1.1 Supply voltage;</p> <p>Changed titles: Section 3.5.6 Stepper motor driver OFF diagnosis (EN signal low and output in high impedance state) and Section 3.5.7 Stepper motor driver ON diagnosis (EN signal high and output driven by input commands);</p> <p>Updated "Notes" in the Table 4. ESD protection;</p> <p>Updated unit of "T_key_deglitch" parameter" in Table 7. Key electrical characteristics and "R_pull" in Table 8. Digital pins characteristics.</p>                                                                                                                                                                                |
| 05-Dec-2017 | 3        | <p>Corrected typos in the titles of the sections: Section 3.5.6 Stepper motor driver OFF diagnosis (EN signal low and output in high impedance state) and Section 3.5.7 Stepper motor driver ON diagnosis (EN signal high and output driven by input commands).</p> <p>Updated Table 1. Pin function.</p> <p>Substituted in the datasheet (texts, tables and drawings) "Vdd" with "VDD".</p> <p>Updated: Figure 5. 5 V main regulator block diagram; Section 2.5.9 High side switch; Figure 10. Low-side driver block diagram; Figure 16. SO loading for disable time measurement; Figure 17. SPI timing diagram; Section 3.4.1 Data in (DIN); Section 3.4.2 Data out (DOUT); Section 3.5.3 Undervoltage shut down; Section 5.1 Bill of material.</p>       |
| 26-Nov-2018 | 4        | <p>Updated:</p> <p>Section Description; Section 2.1 Operating range; Section 2.2 Absolute maximum ratings; Table 8. Digital pins characteristics; Figure 5. 5 V main regulator block diagram; Figure 3. Input threshold; Table 17. Current limited LSD driver characteristics; Section 3.5.5 Current limited low side driver on/off diagnosis; Figure 17. SPI timing diagram; Figure 19. Power-up sequence; Figure 20. Power-down sequence; Section 3.4.1 Data in (DIN); Figure 21. An example of under and over voltage time diagram; Section 3.5.8 VRS diagnosis; Figure 38. Application circuit; Table 34. Bill of material.</p> <p>Changed in all document "LAMP" pin in "L" (Current limited LSD). Updated Section 2.5 Electrical characteristics.</p> |

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