Data Sheet
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Lucent Technologies
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L8574D Resistive Subscriber Line Interface Circuit (SLIC), Ring Relay, and Protector (SRP) for Long Loop and TR-57 Applications

Features

- Low-power scan mode for low on-hook power dissipation (55 mW max)
- Low active power dissipation; talk or on-hook transmission (240 mW max)
- Distortion-free on-hook transmission
- Eight operating states via latched paralleled data inputs with channel select feature
- Precision fixed 28 mA current limiter
- Integrated protection
- No external protection device required
- Integrated ringing access relay
- Ring trip detector
- Loop closure detector with hysteresis
- Relay driver
- Battery noise cancellation
- Thermal protection
- 44-pin, surface-mount, plastic package (PLCC)

Description

The L8574 is a resistive subscriber line interface circuit (SLIC) that is optimized for long loop applications, such as Bellcore TR-NWT-000057 requirements for digital loop carrier (DLC) applications. It interfaces the low-voltage circuits on an analog line card to the Tip/Ring subscriber loop. The L8574 does not supply dc current to the subscriber loop; external resistors are used for this purpose.

Included in the L8574 are a solid-state ringing access switch and a line break switch. Also included is a relay driver for an external (test) access mechanical relay.

State control is via four latched parallel data inputs. A chip select feature allows the user to enable, disable, or reset the data latches to a known logic state.

The L8574 offers a low-power scan state to minimize power to less than 55 mW in the on-hook state. The L8574 also supports on-hook transmission. The active power in both the talk or on-hook transmission mode is also very low (<240 mW). Current is limited to a fixed value of 25 mA by an internal precision current-limit circuit.

Because of the internal architecture of the L8574 SLIC and because of the power rating of the associated external feed resistors, the L8574 will meet most surge requirements without use of an external secondary protection device. Internal circuitry steers both positive and negative faults to fault ground. Negative faults are not dumped into battery.

The L8574 is a two-chip line interface solution packaged in a single, 44-pin PLCC package. The Tip and Ring drive amplifiers, the XMT amplifier, the receive interface, and battery noise cancellation circuits are fabricated in a 90 V complementary bipolar (CBIC) process. The ring access switch, line break switch, battery switch, current-limit, protection functions, supervision, and control functions are fabricated in a 320 V dielectrically isolated bipolar-CMOS-DMOS (BCDMOS) process. The device is available in a 44-pin PLCC package.

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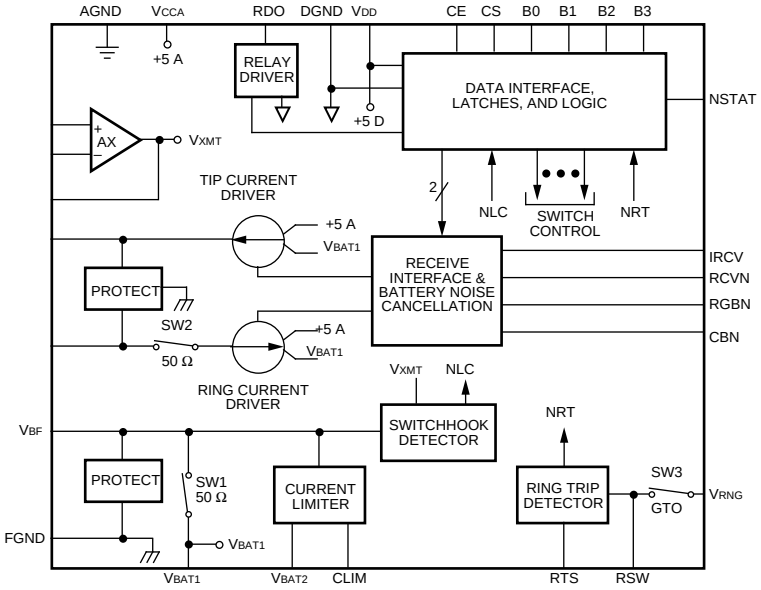

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Figure 1. Architectural Diagram

Pin Information

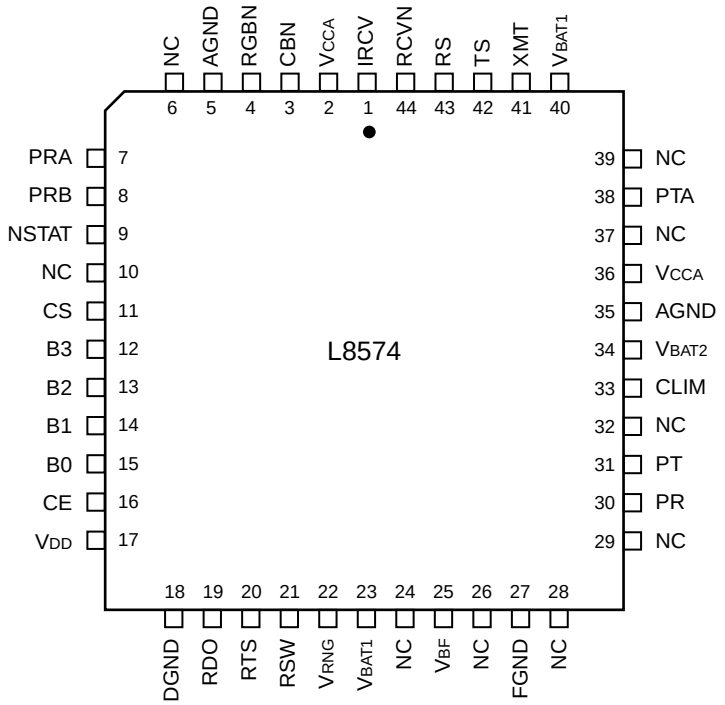

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Figure 2. Pin Layout

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	IRCV	I	**Receive Signal Input (+).** The differential current flowing from PT to PR is 200 times the current flowing into IRCV.
2	V_{CCA}	—	**+5 V Analog dc Supply.** +5 V supply for analog circuitry.
3	CBN	I	**Battery Noise Capacitor.** The current flowing out of PR is –100 times the voltage applied to CBN divided by the impedance connected between RGBN and AGND. Connect a capacitor from CBN to V_{BF} to eliminate battery noise from the Tip/Ring.
4	RGBN	I	**Battery Noise Gain Resistor.** The current flowing out of PR is 100 times the current flowing into RGBN. Connect a resistor from RGBN to AGND to set the gain of the battery noise cancellation circuit.
5	AGND	—	**Analog Ground.** Ground return for analog circuitry.
7	PRA	—	**Protected Ring A.** Connect to PRB via an external coupling network.
8	PRB	—	**Protected Ring B.** Connect to PRA via an external coupling network.
9	NSTAT	O	**Not Status.** When low, this logic output indicates either a ring trip or an off-hook condition, depending on the input state of the SLIC.
11	CS	I	**Channel Select.** A low-to-high transition on this logic input stores the data on pins B0—B3 into the input latches on the SLIC.
12	B3	I	**Bit 3.** B0—B3 determine the state of the SLIC. See the Operating States section.
13	B2	I	**Bit 2.** B0—B3 determine the state of the SLIC. See the Operating States section.
14	B1	I	**Bit 1.** B0—B3 determine the state of the SLIC. See the Operating States section.
15	B0	I	**Bit 0.** B0—B3 determine the state of the SLIC. See the Operating States section.
16	CE	I	**Channel Enable.** A low on this logic input resets latches B0—B3 to the 1111 state and disables the channel select input CS. A high on this logic input enables the channel select input CS.
17	V_{DD}	—	**+5 V Digital dc Supply.** +5 V supply for logic and switch circuitry.
18	DGND	—	**Digital Ground.** Ground return for V_{DD} and the relay driver.
19	RDO	O	**Relay Driver.** This output drives an external relay.
20	RTS	I	**Ring Trip Sense.** Sense input for the ring trip detector.
21	RSW	O	**Ringing Access Switch.** Ringing relay connects this pin to pin V_{RNG} (ringing supply). Connect this pin to pin V_{BF} through a 600 Ω current-limiting resistor.
22	V_{RNG}	—	**Ringing Supply Voltage.** Connect this pin to the ringing supply.
23	V_{BAT1}	—	**Office Battery Supply.** Negative high-voltage power supply.
25	V_{BF}	—	**Feed Resistor Battery Supply.** Negative battery and ringing supply for the loop. Connect this pin to the Ring of the loop through a 200 Ω battery feed resistor.
27	FGND	—	**Fault Ground.**
30	PR	I/O	**Protected Ring.** The input to the Ring fault protection and output of Ring current drive amplifier (via the Ring access switch). Connect this pin to the Ring of the loop through a 1 kΩ overvoltage protection resistor.
31	PT	I/O	**Protected Tip.** The input to the Tip fault protection and output of Tip current drive amplifier. Connect this pin to the Tip of the loop through a 1 kΩ overvoltage protection resistor. Connect to PTA via an external coupling network.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
33	CLIM	I	**Current Limiter Capacitor.** Connect a 0.1 µF capacitor from this pin to pin V_{BF}.
34	V_{BAT2}	—	**Office Battery Supply.** Negative high-voltage power supply.
35	AGND	—	**Analog Ground.** Ground return for analog circuitry.
36	V_{CCA}	—	**+5 V Analog dc Supply.** +5 V supply for analog circuitry.
38	PTA	—	**Protected Tip A.** Connect to PT via an external coupling network.
40	V_{BAT1}	—	**Office Battery Supply.** Negative high-voltage power supply.
41	XMT	O	**Transmit Signal Output.** Transmit amplifier output to codec.
42	TS	I	**Tip Sense.** Negative (–) input of transmit op amp. Connect one high-value resistor between TS and the Tip of the loop and another high-value resistor between TS and XMT.
43	RS	I	**Ring Sense.** Positive (+) input of the transmit op amp. Connect one high-value resistor between RS and the Ring of the loop and another high-value resistor between RS and AGND (see the application diagram, Figure 5).
44	RCVN	I	**Receive Signal Input (–).** The differential current flowing from PT to PR is –200 times the voltage applied to RCVN divided by the impedance connected between IRCV and AGND.

On the printed-wiring board (PWB), make the leads to FGND and V_{BF} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PWB copper on all leads connected to this device for the lowest operating temperature.

Absolute Maximum Ratings

(@ T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
+5 V dc Supplies (V_{CCA} & V_{DD})	—	–0.5	—	7.0	V
Office Battery Supply	V_{BAT1} V_{BAT2}	–63 –63	— —	0.5 0.5	V V
Logic Input Voltage	—	–0.5	—	V_{DD} + 0.5	V
Logic Input Clamp Diode Current, per Pin	—	—	±20	—	mA
Logic Output Voltage	—	–0.5	—	V_{DD} + 0.5	V
Logic Output Current, per Pin (excluding relay driver)	—	—	±35	—	mA
Operating Temperature Range	—	–40	—	125	°C
Storage Temperature Range	T_{stg}	–40	—	125	°C
Relative Humidity Range	—	5	—	95	%
Ground Potential Difference (DGND to AGND)	—	—	±3	—	V

Notes:
Analog voltages (V_{CCA}, V_{BAT1}, and V_{BAT2}) are referenced to AGND, and digital (logic) voltages (V_{DD}) are referenced to DGND.

The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Electrical Characteristics

In general, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and entire battery range (–35 V to –60 V). Unless otherwise specified, typical is defined as 25 °C, V_{CCA} and V_{DD} = +5.0 V, V_{BAT1} and V_{BAT2} = –48 V. Positive currents flow into the device.

Table 2. Operating Conditions and Powering

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range	5	—	95[1]	%RH
Supply Voltages:				
V_{CCA}	4.6	5.0	5.5	V
V_{DD}	4.6	5.0	5.5	V
V_{BAT1}	–42.5	–48	–60	V
V_{BAT2}	–20	–48	V_{BAT1}	V
$V_{CCA} – V_{DD}$	—	—	±0.5	V
Supply Currents (scan state; no loop current)[2]:				
$I_{VCCA} + I_{VDD}$ (+5 V)	—	—	3.0	mA
I_{VBAT1} (–48 V) + I_{VBAT2} (–48 V)	—	—	–825	µA
Supply Currents (talk or on-hook transmission state; no loop current)[2]:				
$I_{VCCA} + I_{VDD}$ (+5 V)	—	—	6.0	mA
I_{VBAT1} (–48 V) + I_{VBAT2} (–48 V)	—	—	–4.5	mA
Total Power Dissipation (no loop current)[2] (V_{CCA} and V_{DD} = +5 V; V_{BAT1} and V_{BAT2} = –48 V):				
Talk or On-hook Transmission State	—	—	240	mW
Scan State	—	—	55	mW
Power Supply Rejection (Tip/Ring)[3]:				
V_{CCA} (500 Hz—3 kHz; 50 mVrms ripple)	40	50	—	dB
V_{DD} (500 Hz—3 kHz; 50 mVrms ripple)	50	—	—	dB
V_{BAT2} and V_{BAT1} (500 Hz—2 kHz; 50 mVrms ripple)[4]	40	—	—	dB
V_{BAT2} and V_{BAT1} (2 kHz—3 kHz; 50 mVrms ripple)[4]	35	40	—	dB
Thermal[3]:				
Thermal Resistance (still air)	—	—	60	°C/W
Operating T_{jc}	—	—	135	°C
Thermal Shutdown Temperature	—	145	—	°C

1. Not to exceed 26 grams of water per kilogram of dry air.
2. Includes current in all external resistors per Figure 15.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. V_{BAT1} and V_{BAT2} power supply rejection depends on the battery noise cancellation circuit. The performance stated here applies to V_{BAT2} only during the talk state and V_{BAT1} only during the on-hook transmission state and assumes proper battery noise cancellation (see Figure 5).

Electrical Characteristics (continued)

Ring Trip Detector

Table 3. Ring Trip Detector

Parameter	Min	Typ	Max	Unit
Ringing Source[1]:				
Frequency (f)	17	20	28	Hz
dc Voltage	–36	—	–57	V
ac Voltage	60	—	105	Vrms
Ring Trip[2] (NSTAT = 0):				
Loop Resistance	1840	—	—	Ω
Trip Time (f = 20 Hz)	—	—	200	ms
NSTAT Valid	—	—	80	ms

1. The ringing source consists of the ac and dc voltages added together (battery-backed ringing); the ringing return is battery ground.
2. Pretrip: ringing must not be tripped by a 10 kΩ resistor in parallel with an 8 µF capacitor applied across Tip and Ring.

Battery Feed

Table 4. Battery Feed

Parameter	Min	Typ	Max	Unit
Loop Resistance Range[1] (3.17 dBm overload into 600 Ω):				
I_{LOOP} = 18 mA at V_{BAT2} = –42 V	1840	—	—	Ω
Longitudinal Current Capability per Wire[2]	8.5	—	—	mArms
dc Loop Current Limit (R_{LOOP} = 200 Ω)	26.5	28	29.5	mA
Current-limiter ac Output Impedance[3]:				
200 Hz to 4 kHz	—	—	25	Ω
Current-limiter Transient Current (in response to a step voltage change on V_{BF})	8	—	150	mA
Switchhook Detector Loop Resistance[4]:	—	3300	—	Ω
Off-hook (NSTAT = 0)	—	—	2700	Ω
On-hook (NSTAT = 1)	4400	—	—	Ω
Longitudinal to Metallic Balance—*IEEE*[5] Std. 455[6]:				
200 Hz to 1 kHz	58	—	—	dB
1 kHz to 3 kHz	53	—	—	dB
Metallic to Longitudinal (Harm) Balance[7]:				
200 Hz to 4 kHz	30	—	—	dB

1. Assumes 2 x 200 Ω external dc feed resistors.
2. When the current-limit circuit is active and the battery switch is off, the longitudinal current must be less than the dc loop current to ensure proper ac transmission.
3. Assumes C_{LIM} = 33 nF; C_{LIM} determines the ac output impedance of the current-limit circuit when it is active.
4. Detector values are independent of office battery and are valid over the entire range of V_{BAT1} and V_{BAT2}. However, NSTAT must indicate an on-hook (NSTAT = 1) if either V_{BAT1} or V_{BAT2} is disconnected (open circuit) from its dc source and an off-hook (NSTAT = 0) if the L8574 is in thermal shutdown. The status of the thermal shutdown circuit is output on B3 when CS is high (thermal shutdown is a logic 0). V_{BAT1} and V_{BAT2} are defined as disconnected depending on the voltage at the power supply pins as follows (the pins of supplies that have more than one pin are shorted together):
   — If $V_{BAT1} \leq$ –20 V (i.e., more negative than –20 V) and $V_{BAT2} \leq$ –20 V, then NSTAT must operate normally.
   — If $V_{BAT1} \geq$ –10 V (i.e., more positive than –10 V) or $V_{BAT2} \geq$ –10 V, then NSTAT must be on-hook (NSTAT = 1).
5. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
6. Assumes the external dc feed resistors are matched to 0.2% and proper battery noise cancellation; i.e., a 0.22 µF capacitor from V_{BF} to CBN (see Figure 5).
7. Assumes proper battery noise cancellation; i.e., a 0.22 µF capacitor from V_{BF} to CBN (see Figure 5).

Electrical Characteristics (continued)

Fault Protection

Pins PT, PR, and V_{BF}

Pins PT, PR, and V_{BF} are protected by SCRs which clamp surge currents (both positive and negative) to FGND. If the SCR on PR or V_{BF} triggers due to a negative surge, the L8574 automatically switches to the disconnect state while the SCR is conducting current above its hold current. After the SCR releases, the L8574 automatically switches back to the operating state prior to the SCR trigger.

Table 5. Electrical Characteristics of Pins PT, PR, and V_{BF}

Parameter	Min	Typ	Max	Unit
PT and PR:				
Surge Current[1]:				
Lightning—10 µs x 1000 µs	—	—	±1	A
Lightning—2 µs x 10 µs	—	—	±2.5	A
Power Cross—60 Hz, 50 ms	—	—	600	mArms
Power Cross—60 Hz, 1 s	—	—	200	mArms
Power Cross—60 Hz, 15 min.	—	—	50	mArms
SCR Trigger Voltage Pin PT:				
Positive	V_{CCA} – 2	—	V_{CCA} + 4	V
Negative	–25	—	–35	V
dc Transient Response	–25	—	–55	V
SCR Trigger Voltage Pin PR:				
Positive	150	—	280	V
Negative	–220	—	320	V
SCR Hold Current (positive and negative)	10	—	—	mA
V_{BF}:				
Surge Current[1]:				
Lightning—10 µs x 1000 µs	—	—	±5.5	A
Lightning—2 µs x 10 µs	—	—	±13	A
Power Cross—60 Hz, 50 ms	—	—	3	Arms
Power Cross—60 Hz, 1 s	—	—	800	mArms
Power Cross—60 Hz, 15 min.	—	—	150	mArms
SCR Trigger Voltage:				
Positive	150	—	280	V
Negative	–220	—	–320	V
SCR Hold Current (positive and negative)	10	—	—	mA
Trigger Current (if from a power supply—PT, PR, and V_{BF})	—	—	±250	µA
dV/dt Sensitivity[1, 2] (PT, PR, and V_{BF})	—	500	—	V/µs

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Applied voltage is 50 Vpp square wave at 100 Hz to measure dV/dt sensitivity.

Electrical Characteristics (continued)

Fault Protection (continued)

Loss of Power Supplies

The L8574 must protect itself from lightning and power cross voltages on Tip and Ring if any (or any combination) of the power supplies (V_{CCA}, V_{DD}, V_{BAT1}, and V_{BAT2}) are disconnected (open circuit) from their dc source. Additionally, if any power supply is disconnected, no overvoltage on Tip or Ring can cause a supply voltage to exceed its maximum rating. Under these conditions, V_{CCA} and V_{DD} are considered as one supply (V_{CCA} shorted to V_{DD}), the pins of supplies which have more than one pin are shorted together, and bypass capacitors are connected. To satisfy these requirements (and also to disconnect ringing from the loop when ring trip cannot be detected), the L8574 is placed into the disconnect state depending on the voltage at the power supply pins as shown in Table 6.

Table 6. Loss of Power Supplies

Parameter	Min	Typ	Max	Unit
V_{CCA} and V_{DD}:				
Normal Operating State (as defined by control logic)	1	—	—	V
Disconnect State	—	—	4.5	V
V_{BAT1}:				
Normal Operating State (as defined by control logic)	–10	—	–75	V
Disconnect State	—	—	–20	V
Disconnect State	–65	—	—	V

Electrical Characteristics (continued)

Fault Protection (continued)

Loss of Power Supplies (continued)

Table 7. Analog Signal Pins

Parameter	Min	Typ	Max	Unit
PT and PR:				
Surge Current (See the Protection section.)				
Output Drive (PT):				
Drive Current	±15	—	—	mA
Negative Voltage Swing (I_{OUT} + 10 mA)	V_{BAT1} + 4.5	—	V_{BAT1}	V
Positive Voltage Swing (I_{OUT} – 10 mA)	V_{CCA} – 3.5	—	V_{CCA}	V
dc Bias Current	600	—	900	µA
Output Drive (PR):				
Positive (sink) Drive Current	±15	—	—	mA
Negative Voltage Swing (I_{OUT} + 10 mA)	V_{BAT1} + 4.5	—	V_{BAT1}	V
Positive Voltage Swing (I_{OUT} – 10 mA)	V_{CCA} – 3.5	—	V_{CCA}	V
dc Bias Current (V_{BAT2} = V_{BAT1} – 48 V)[1]	–0.8	—	–1.4	mA
Output Short-circuit Transient Current[2]	—	—	±125	mA
Output Impedance (60 Hz—3.4 kHz)[3]	250	—	—	kΩ
Output Load Resistance (dc or ac)[3]	100	—	—	Ω
Output Load Capacitance[3]	—	—	1	nF
XMT:				
Output Drive Current	±1	—	—	mA
Output Voltage Swing (1 mA load):				
Maximum	V_{BAT1}	—	V_{CCA}	V
Minimum	V_{BAT1} + 5	—	2.5	V
Output Short-circuit dc Current	—	—	±20	mA
Output Impedance (60 Hz—3.4 kHz)[3]	—	—	10	Ω
Output Load dc Resistance[3]	50	—	—	kΩ
Output Load ac Resistance	2	—	—	kΩ
Output Load Capacitance[3]	—	—	50	pF

1. Connected per Figure 5.
2. A battery or ground short on PT, PR, or XMT shall not cause a device failure.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Fault Protection (continued)

Loss of Power Supplies (continued)

Table 7. Analog Signal Pins (continued)

Parameter	Min	Typ	Max	Unit
RCVN:				
Input Voltage Range	–1.75	—	V_{CCA} – 1.0	V
Input Bias Current	—	—	±1	µA
Input Impedance[3]	20	—	—	MΩ
IRCV:				
Input Offset Voltage (to RCVN)	—	—	±20	mV
Input Impedance[3]	—	—	5	Ω
CBN:				
Surge Current (lightning 10 µs x 1000 µs)	—	—	±100	mA
Input Voltage Range	–1.75	—	1.25	V
Input Bias Current	—	—	±250	nA
Input Impedance[3]	50	—	—	MΩ
Input Positive Clamp Voltage (I_{CBN} = +100 µA)	1.50	—	1.90	V
Input Negative Clamp Voltage (I_{CBN} = –100 µA)	–2.00	—	–3.20	V
RGBN:				
Input Offset Voltage (to CBN)	—	—	±10	mV
Input Impedance[3]	—	—	5	Ω
TS and RS:				
Surge Current from External Source	—	—	±25	mAdc
Input Voltage Range[3]	V_{BAT1} + 3	—	AGND	V
Input Bias Current	—	—	±1	µA
Differential Input Impedance[3]	50	—	—	kΩ
Common-mode Input Impedance[3]	50	—	—	MΩ
External Capacitance (67 kΩ source impedance)[3]	—	—	10	pF

1. Connected per Figure 5.
2. A battery or ground short on PT, PR, or XMT shall not cause a device failure.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Transmission Characteristics

Transmit direction is Tip/Ring to XMT. Receive direction is IRCV/RCVN to Tip/Ring.

Table 8. ac Transmission Characteristics

Parameter[1]	Min	Typ	Max	Unit
ac Termination Impedance[2]	—	600	—	Ω
Return Loss[3]:				
200 Hz—500 Hz	21	—	—	dB
500 Hz—2500 Hz	26	—	—	dB
2500 Hz—3400 Hz	21	—	—	dB
Tip/Ring Signal Level (600 Ω reference)	—	—	3.14	dBm
Total Harmonic Distortion (200 Hz—4 kHz)[3]	—	—	0.3	%
Transmit Gain (f = 1 kHz):				
(Tip/Ring) to XMT	–0.486	–0.500	–0.514	—
Receive Gain (f = 1 kHz):				
IRCV to Differential Current Flowing from IPT to IPR	195	200	205	—
RCVN to IRCV	0.995	1	1.005	—
Gain vs. Frequency (transmit and receive; 1 kHz reference)[3]:				
200 Hz—300 Hz	–1.00	0	0.05	dB
300 Hz—3.4 kHz	–0.30	0	0.05	dB
3.4 kHz—20 kHz	–3.0	0	1.0	dB
20 kHz—266 kHz	—	—	1.0	dB
Gain vs. Level (transmit and receive; 0 dBV reference)[3]:				
–50 dB to +3 dB	–0.05	0	0.05	dB
Transhybrid Loss[3]:				
200 Hz—500 Hz	21	—	—	dB
500 Hz—2500 Hz	26	—	—	dB
2500 Hz—3400 Hz	21	—	—	dB
Idle-channel Noise (Tip/Ring):				
Psophometric[3]	—	—	–77	dBmp
C-message	—	—	12	dBrnC
3 kHz Flat[3]	—	—	20	dBrn
Idle-channel Noise (XMT):				
Psophometric[3]	—	—	–77	dBmp0
C-message	—	—	12	dBrnC0
3 kHz Flat[3]	—	—	20	dBrn0

1. Requires external components connected as shown in Figure 5. Transmission characteristics are specified assuming a 900 Ω resistive termination and ±1% external resistors.
2. Transmission characteristics are specified assuming a 900 Ω resistive termination; however, feedback using external components allows the user to adjust the termination impedance from 900 Ω to most ITU-T recommended complex termination impedances.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Data Interface and Logic

Table 9. Logic Inputs (CE, CS, and B0—B3) and Output NSTAT

Parameter[1]	Symbol	Min	Max	Unit
High-level Input Voltage	V_{IH}	2	V_{DD}	V
Low-level Input Voltage	V_{IL}	0	0.8	V
Input Bias Current (high and low)	I_{IN}	—	±10	µA
High-level Output Voltage (I_{OUT} = –100 µA)	V_{OH}	V_{DD} – 1.5	V_{DD}	V
Low-level Output Voltage (I_{OUT} = 180 µA)	V_{OL}	0	0.4	V
Output Short-circuit Current (V_{OUT} = V_{DD})	I_{OSS}	1	35	mA
Output Load Capacitance[2]	C_{OL}	0	50	pF

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 10. Timing Requirements (B0—B3 and CS)

A low-to-high transition on pin CS latches the data on pins B0—B3 into the device. When CS is either high or low, the device is unaffected by data on pins B0—B3. The status of the thermal shutdown circuit is output on B3 when CS is high (thermal shutdown is a logic 0). A low on channel enable lead CE asynchronously resets the data latch to 1111 (scan state with the relay driver off) and disables CS so that CS cannot latch any data into the device. A high on CE enables CS.

Parameter[1, 2]	Symbol	Min	Max	Unit
CS Rise and Fall Time (10% to 90%)	t_R, t_F	0	50	ns
Maximum Input Capacitance	C_{IN}	—	5	pF
Minimum Setup Time from B0—B3 Valid to CS	t_{SDS}	150	—	ns
Minimum Hold Time from CS to B0—B3 Not Valid	t_{HDS}	50	—	ns
Minimum Pulse Width of CS	t_{WCS}	225	—	ns

1. Unless otherwise specified, all times are measured from the 50% point of logic transitions.
2. These parameters are not tested in production. They are guaranteed by design and device characterization.

Table 11. Relay Driver (RDO)

The relay driver output RDO is low (relay operated) when a low input on B3 is latched into the device.

Parameter[1]	Symbol	Min	Max	Unit
Off-state Output Current (V_{RDO} = V_{DD})	I_{OFF}	—	±10	µA
On-state Output Voltage (I_{RDO} = 70 mA)	V_{ON}	0	1.0	V
On-state Output Voltage (I_{RDO} = 20 mA)	V_{ON}	0	0.40	V
Clamp Diode Reverse Current (V_{RDO} = 0)	I_R	—	±10	µA
Clamp Diode On Voltage (I_{RDO} = 150 mA)	V_{OC}	V_{DD}	V_{DD} + 2.0	V
Turn-on Time[2]	t_{ON}	—	10	µs
Turn-off Time[2]	t_{OFF}	—	10	µs

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Switch Characteristics

Table 12. Battery Switch (SW1) and Ring Break Switch (SW2)

Parameter	Min	Typ	Max	Unit
Off-state[1]:				
Maximum Differential Voltage	—	—	±320[2]	V
dc Leakage Current (V_{SW} ± 320 V)	—	—	±50	µA
Feedthrough Capacitance[3]	—	—	50	pF
On-state (See Figures 3 and 4.):				
Resistance (R_{ON})	—	50	100	Ω
Maximum Differential Voltage (V_{max})	—	—	320[2]	V
Current Limit (I_{LIMIT})	20	35	60	mA
dV/dt Sensitivity[3, 4]	—	200	—	V/µs

1. SW2 must be off if the voltage on pin PR is more positive than V_{CCA}.
2. At 25 °C. Maximum voltage rating has a temperature coefficient of +0.167 V/°C.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. Applied voltage is 100 Vpp square wave at 100 Hz to measure dV/dt sensitivity.

Table 13. Ringing Access Switch (SW3)

Parameter	Min	Typ	Max	Unit
Off-state:				
Maximum Differential Voltage	—	—	±500	V
dc Leakage Current (V_{SW} = ±500 V)	—	—	±20	µA
dc Leakage Current (V_{SW} = ±250 V)	—	—	±1	µA
Feedthrough Capacitance[1]	—	—	10	pF
On-state (See Figures 3 and 4.):				
Crossover Offset Voltage (V_{OS}; I_{SW} = ± 1 mA)	—	—	3	V
Resistance (R_{ON})	—	—	10	Ω
Surge Current (10 µs x 1000 µs pulse)[1]	—	—	2.0	A
Release Current[1]	0.1	—	3	mA
dV/dt Sensitivity[1, 2]	—	500	—	V/µs

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Applied voltage is 100 Vpp square wave at 100 Hz to measure dV/dt sensitivity.

Electrical Characteristics (continued)

Switch Characteristics (continued)

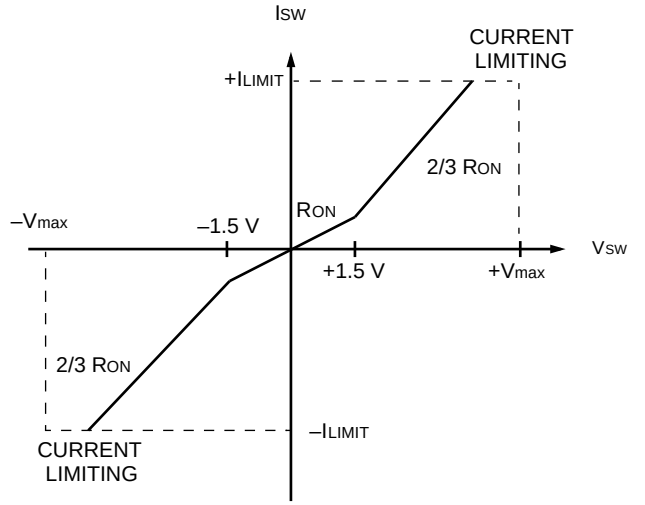


Figure 3. Switch On-State V-I Characteristics SW1 and SW2

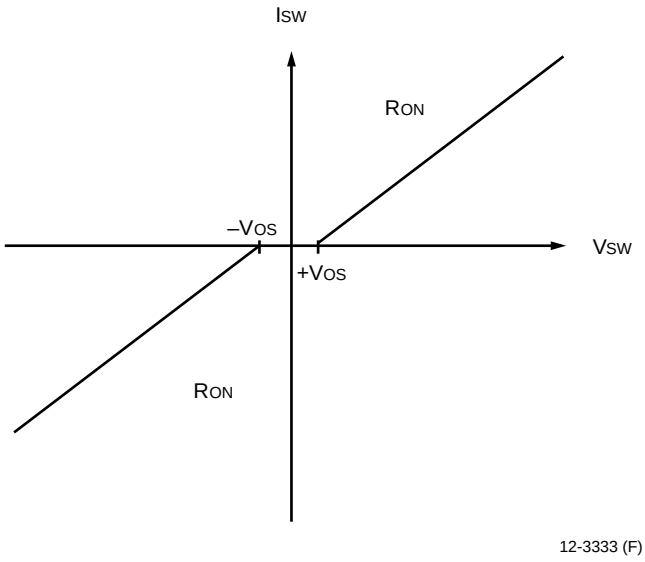


Figure 4. Switch On-State V-I Characteristics SW3

Operating States

The L8574 has eight operating states. These states are selected using three logic input bits, B0—B2, according to the truth table shown in Table 14. Logic input B3 operates a relay driver independent of the state of bits B0—B2. Data on the parallel data bus, B0—B3, is loaded into a 4-bit latch on the L8574 on the low-to-high transition of the channel select lead CS. Changes in the data at inputs B0—B3 do not affect the L8574 while CS is either low or high. A low on channel enable lead CE asynchronously resets the 4-bit latch to 1111 (scan state with the relay driver off) and disables the channel select lead CS (i.e., CS is prevented from loading any data into the 4-bit latch). A high on CE enables CS. State transitions and delays between transitions are left to the discretion of the user since, except for fault conditions described later, the state of the L8574 depends only on the external control provided through the logic interface.

Table 14. Input State Coding

CE	B3	B2	B1	B0	State
0	X	X	X	X	Scan state with relay driver off
1	X	1	1	1	Scan
1	X	1	1	0	Disconnect
1	X	1	0	1	Alternative talk—SW1 closed
1	X	1	0	0	Talk—SW1 open
1	X	0	1	1	Scan current limit
1	X	0	1	0	Ringing
1	X	0	0	1	On-hook transmission
1	X	0	0	0	Intermediate talk
1	0	X	X	X	Relay driver output (RDO) is low (relay active)
1	1	X	X	X	Relay driver output (RDO) is high (relay not active)

Scan State

- Normal on-hook supervision state.
- The receive transmission path is powered down; the transmit path is powered up.
- The battery feed is connected to the high battery supply (V_{BAT1}).
- The current limiter is powered down and disabled.
- SW1 is closed; SW2 and SW3 are open.
- NSTAT reflects the status of the switchhook detector.

Operating States (continued)

Disconnect State

- Forward disconnect state.
- The receive transmission path is powered down; the transmit path is powered up.
- The current limiter is powered down and disabled.
- SW1, SW2, and SW3 are open.
- Pins PT, PR, and V_{BF} are high impedance (>100 kΩ).
- NSTAT is forced high (on-hook).

Alternate Talk State

- Alternate talk state.
- The battery feed is connected to the high battery supply (V_{BAT1}).
- The receive and transmit transmission paths are both powered up.
- The current limiter is powered up and active.
- SW1 and SW2 are closed; SW3 is open.
- NSTAT reflects the status of the switchhook detector.

Talk State

- Normal talk state.
- The battery feed is connected to the high battery supply (V_{BAT2}).
- The receive and transmit transmission paths are both powered up.
- The current limiter is powered up and active.
- SW2 is closed; SW1 and SW3 are open.
- NSTAT reflects the status of the switchhook detector.

Scan Current-Limit State

- Alternate on-hook supervision state.
- Same as scan state but with the current limiter powered up and active.
- The receive transmission path is powered down; the transmit path is powered up.
- SW1 is closed; SW2 and SW3 are open.
- NSTAT reflects the status of the switchhook detector.

Ringing State

- Normal ringing state.
- The receive and transmit transmission paths are both powered down.
- SW3 is closed; SW1 and SW2 are open.
- The current limiter is powered down and disabled.
- NSTAT reflects the status of the ring trip detector.

On-Hook Transmission State

- Normal on-hook transmission state.
- The battery feed is connected to the high battery supply (V_{BAT1}).
- The receive and transmit transmission paths are both powered up.
- The current limiter is powered down and disabled.
- A 10 mA dc bias current flows out of the Ring current driver into PR, and a 5 mA dc bias current flows into the Tip current driver from PT (the switchhook detector is adjusted to compensate for this dc bias current).
- SW1 and SW2 are closed; SW3 is open.
- NSTAT reflects the status of the switchhook detector.

Operating States (continued)

Intermediate Talk State

- Talk state with an increased and current-limited output impedance.
- Same as talk state.
- The current limiter is powered up and active, but the output capacitance at V_{BF} is reduced to approximately 350 times I_{LIM}. This allows rapid settling of the V_{BF} voltage during transitions from on-hook transmission to the talk state.
- A 10 mA dc bias current flows out of the Ring current driver into PR, and a 5 mA dc bias current flows into the Tip current driver from PT (the switchhook detector and current limiter are adjusted to compensate for this dc bias current).
- SW2 is closed; SW1 and SW3 are open.
- NSTAT reflects the status of the switchhook detector.

Applications

General

The L8574 supplies a precise differential current to the Tip/Ring pair (via PT and PR) as a function of analog signals on IRCV and RCVN. However, the current drivers connected to PT and PR are not designed to supply dc feed current to the loop. The dc loop current is fed by two external 200 Ω resistors. When a loop is idle (on-hook), the battery switch (SW1) is turned on to connect the Ring lead to V_{BAT1} which is typically –48 V, thus providing sufficient Tip/Ring open circuit voltage to operate various types of customer premises equipment (CPE). Transmission may or may not be enabled in the idle dc feed condition. If transmission is enabled (on-hook transmission), the current drivers are biased so that they can both source and sink sufficient signal current when no dc loop current is flowing (even in the presence of longitudinal currents on Tip and Ring). When the loop is off-hook, the battery switch (SW1) is turned off and the current limiter becomes active. This connects the Ring lead to V_{BAT2} (typically –48 V) through an accurate current limiter circuit which saves off-hook power dissipation. To ensure proper ac performance, the ac output impedance of the current limiter must be small. The effective output capacitance at V_{BF} is approximately 7500 times C_{LIM} when the current limiter is active.

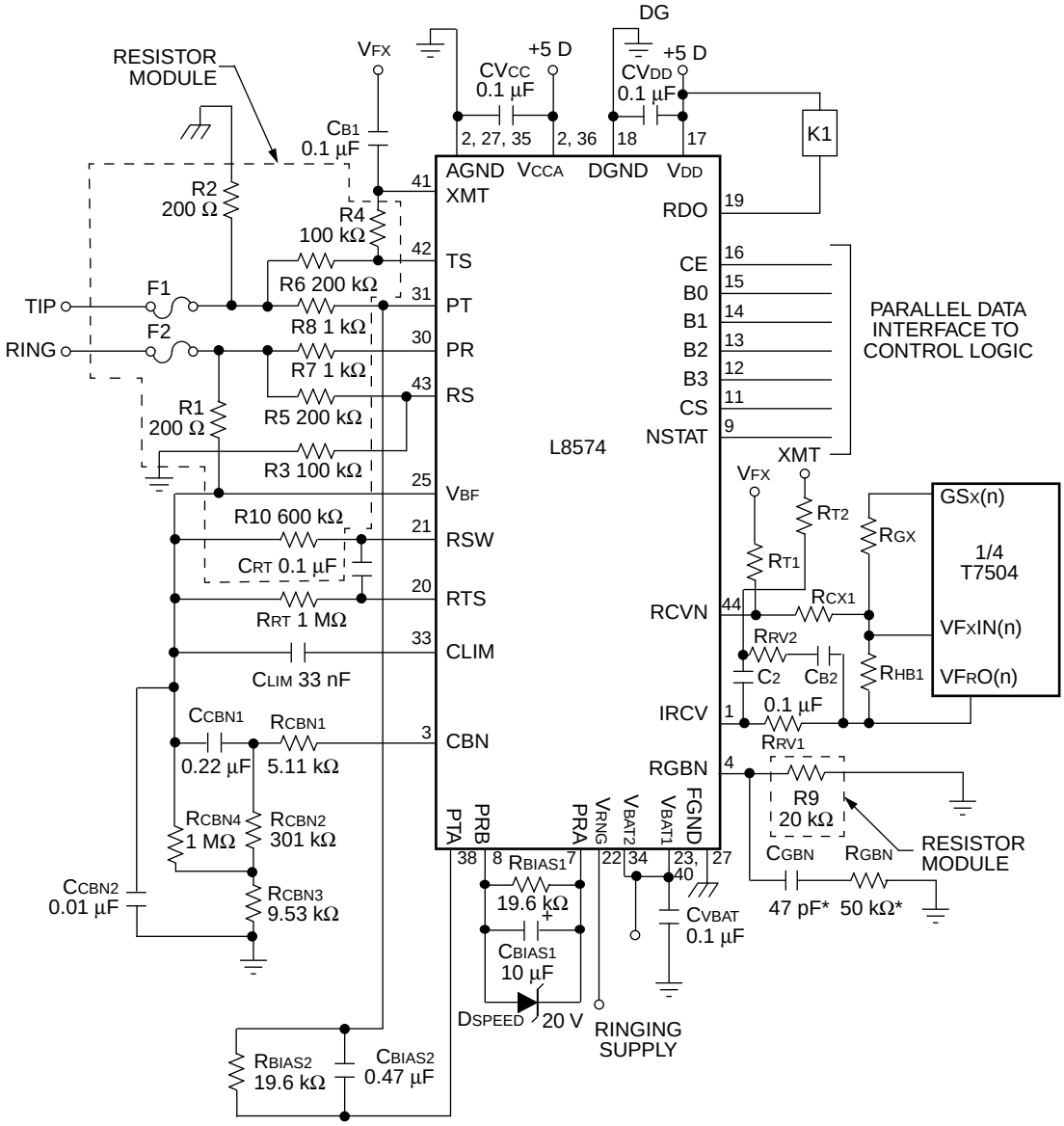
The external 200 Ω dc feed resistors will, for the most part, determine the longitudinal balance of the SLIC; thus, they must be matched appropriately to meet the longitudinal balance requirements (0.2% for 58 dB balance, 0.35% for 52 dB balance). The impedance of the battery switch and current limiter in series with the ring-side dc feed resistor is reduced by the battery noise cancellation circuit so that it has minimal effect on the longitudinal balance. The dc feed resistors also have a significant impact on the termination impedance of the SLIC. Feedback, using external components, allows the user to adjust the termination impedance from the 400 Ω dc feed resistance to satisfy most resistive and complex termination impedances. Because the L8574 does not supply dc feed current to the loop outputs, PT and PR can be coupled to the Tip and Ring through a sufficiently high resistance to allow for simple lightning protection of the drivers. However, the resistance must be low enough to achieve the coupling of sufficient ac signal to the Tip and Ring from the available power supply. Since the Tip and Ring drivers are current sources, the value of this resistance does not affect the performance of the SLIC and is somewhat arbitrary. The value chosen is typically 1000 Ω.

The L8574 also senses the differential Tip/Ring voltage via sense inputs TS and RS. The differential dc voltage is used internally for switchhook detection. The detector threshold is preset internally. The differential Tip/Ring ac signal appears on analog output XMT. Also included on the L8574 are SCR protectors, a relay driver, one logic output (indicates switchhook and ring trip status), a 4-bit parallel logic interface, a ringing access switch, a ring trip detector, and a circuit which eliminates the battery noise that is coupled to the Tip and Ring through the dc feed resistors.

The following diagram and table show the basic components required with the L8574 SLIC. Specific component values are given in cases where the value is fixed. In cases where the value may change (i.e., components that determine the ac interface), the value is not listed but equations to determine these values are given later in this document.

Applications (continued)

General (continued)



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* Optional components to improve PSRR by 6 dB.

Figure 5. External Components Required

Applications (continued)

General (continued)

Table 15. External Components Required

Comp.	Function	Implementation	Value	Attribute[1]
F1	Fuse Protector	Resistor Module	—	—
F2	Fuse Protector	Resistor Module	—	—
R_1	dc Feed Protection	Resistor Module	200 Ω	1.0%, 2 W[2]
R_2	dc Feed Protection	Resistor Module	200 Ω	1.0%, 2 W[2]
R_3	Transmit Gain	Resistor Module	100 kΩ	1.0%, 25 mW[3]
R_4	Transmit Gain	Resistor Module	100 kΩ	1.0%, 25 mW[3]
R_5	Transmit Gain	Resistor Module	200 kΩ	1.0%, 25 mW[3]
R_6	Transmit Gain	Resistor Module	200 kΩ	1.0%, 25 mW[3]
R_7	Protection	Resistor Module	1 kΩ	2.0%, 0.1 W
R_8	Protection	Resistor Module	1 kΩ	2.0%, 0.1 W
R_9	Battery Noise Cancellation	Resistor Module	20 kΩ	10 mW[4]
R_{10}	Ringing	Resistor Module	600 Ω	1.0%, 1.6 W (14 W for 250 ms)
C_{VCC}	V_{CC} Filter	External	0.1 µF	20%, 10 V
C_{VDD}	V_{DD} Filter	External	0.1 µF	20%, 10 V
C_{BAT}	V_{BAT} Filter	External	0.1 µF	20%, 100 V
C_{LIM}	Current Limit	External	33 nF	20% 100 V
R_{CBN1}	Battery Noise Cancellation	External	5.11 kΩ	1%, 1/16 W
R_{CBN2}	Battery Noise Cancellation	External	301 kΩ	1%, 1/16 W
R_{CBN3}	Battery Noise Cancellation	External	9.53 kΩ	1%, 1/16 W
R_{CBN4}	Battery Noise Cancellation	External	1 MΩ	1%, 1/16 W
C_{CBN1}	Battery Noise Cancellation	External	0.22 µF	20%, 100 V

1. Power is continuous rms power.
2. $R_1/R_2 = 1$, with a tolerance of 0.35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance. Fuses F1 and F2 provide fail-safe operation if excessive overvoltage conditions exist on Tip and Ring. They will not operate if the total power dissipation of the entire resistor network is ≤5 W at 85 °C.
3. $(R_3 + R_6)/(R_4 + R_5) = 1$ with a tolerance of 0. 35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance.
4. $R_9/R_1 = 100$ with a tolerance of 0.5%.

Applications (continued)

General (continued)

Table 15. External Components Required (continued)

Comp.	Function	Implementation	Value	Attribute[1]
C_{CBN2}	Battery Noise Cancellation	External	0.01 µF	20%, 100 V
C_{GBN}[5]	Battery Noise Cancellation	External	47 pF	20%, 100 V
R_{GBN}[5]	Battery Noise Cancellation	External	50 kΩ	20%, 100 V
C_{RT}	Ring Trip	External	0.1 µF	20%, 100 V
R_{RT}	Ring Trip	External	1 MΩ	1%, 1/16 W
R_{BIAS1}	dc Bias for On-hook Trans.	External	19.6 kΩ	1%, 1/16 W
R_{BIAS2}	dc Bias for On-hook Trans.	External	19.6 kΩ	1%, 1/16 W
C_{BIAS1}	ac Transmission	External	10 µF	20%, 100 V
C_{BIAS2}	ac Transmission	External	0.47 µF	20%, 100 V
D_{SPEED}	Reduce Settling Time Off-hook to On-hook	External	20 V	Zener
C_{B1}	dc Blocking	External	0.1 µF	20%, 10 V
C_{B2}	dc Blocking	External	0.1 µF	20%, 10 V
R_{T1}	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{T2}	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{GX}	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{GX1}	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{RV1}	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{RV2}	ac Interface	External	See ac Design Equations	1%, 1/32 W
C_2	ac Interface	External	See ac Design Equations	1%, 1/32 W
R_{HB1}	ac Interface	External	See ac Design Equations	1%, 1/32 W

1. Power is continuous RMS power.
2. R_1/R_2 = 1, with a tolerance of 0.35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance. Fuses F1 and F2 provide fail-safe operation if excessive overvoltage conditions exist on Tip and Ring. They will not operate if the total power dissipation of the entire resistor network is ≤5 W at 85 °C.
3. $(R_3 + R_6)/(R_4 + R_5)$ = 1 with a tolerance of 0. 35% for 50 dB longitudinal balance, 0.2% for 58 dB longitudinal balance.
4. R_9/R_1 = 100 with a tolerance of 0.5%.
5. Optional components to improve PSRR by 6 dB.

Applications (continued)

Resistor Module

The L8574 requires certain external resistors at the Tip and Ring interface. Because of matching and protection requirements, one of the most economical options recommended to implement these resistors is in a thick-film resistor module. A schematic and a brief description of the function of each of these resistors is given in Figure 6. Note that Microelectronic Modules Corporation *MMC** A31A8574AA and *MMC* A11A8574AA thick-film resistor modules are application-specific resistor modules designed for use with the L8574 SLIC. The values, tolerance, matching, and power rating of the *MMC* A31A8574AA and *MMC* A11A8574AA modules are given in Table 16.

Resistors R_1 and R_2 are the dc feed resistors. R1 is connected from battery to Ring and R_2 is connected from Tip to ground. The dc loop current is fed to the subscriber loop via these resistors. The resistors set the dc feed resistance, which is $R_1 + R_2$ (400 = 200 + 200).

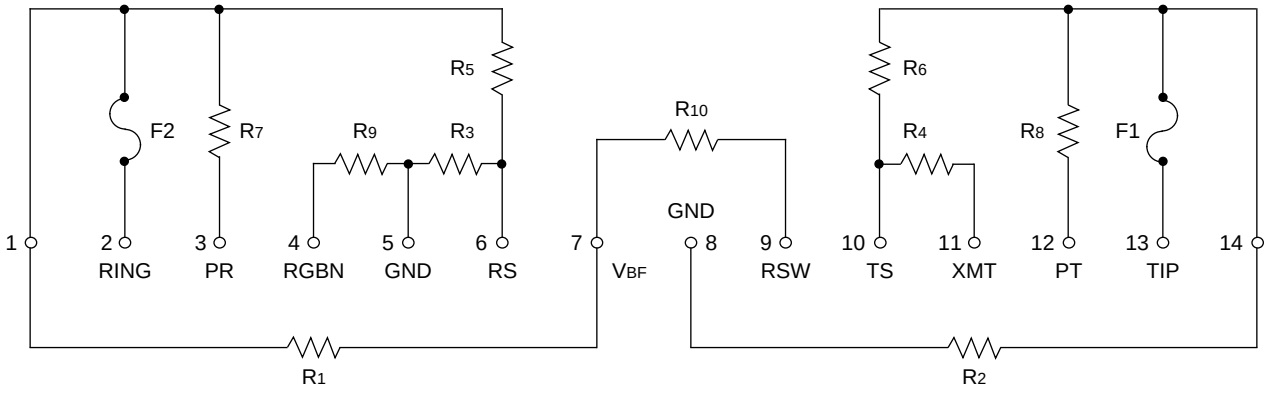
Resistors R_1 and R_2 also provide a common-mode impedance of (200 || 200) 100 Ω. These resistors will primarily determine the longitudinal balance of the line circuit; thus, they must be matched appropriately to meet longitudinal balance requirements (0.35% for 50 dB and 0.2% for 58 dB). Also, they have a significant impact on the termination impedance of the SLIC. Feedback using external components (external components when a first- or second-generation codec is used) allows the user to set the termination impedance at 600 Ω, or most ITU-T recommended termination impedances.

Under normal operating conditions, the current through resistors R_1 and R_2 is limited by the current-limit circuitry to 25 mA. Thus, the 2 W rating of resistors R_1 and R_2 in *MMC* A31A8574AA and *MMC* A11A8574AA is adequate for normal operation. The power rating of these resistors is discussed more in the Protection section of this data sheet.

* *MMC* is a registered trademark of Microelectronic Modules Corporation. For additional information, contact Microelectronic Modules Corporation (MMC), 2601 S. Moorland Rd., New Berlin, WI 53151 U.S.A.: Tel. 414-785-6506, FAX 414-785-6516, e-mail sales@mmccorp.com.

Applications (continued)

Resistor Module (continued)



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Notes:
1. Pin numbers and resistor labels are per *MMC* A31A8574AA and *MMC* A11A8574AA descriptions.
2. Node labels are per L8574 package.
3. For 600 V power cross, resistor networks should “open” in less than 40 ms.

Figure 6. Resistor Network

Table 16. *MMC* A31A8574AA and *MMC* A11A8574AA Module

Resistor	Value	Tolerance	Power[1]	Surge Rating
R_1	200 Ω	1.0%	2.0 W	Lightning: Power Cross
R_2	200 Ω	1.0%	2.0 W	Lightning: Power Cross
R_3	100 kΩ	1.0%	25 mW	None
R_4	100 kΩ	1.0%	25 mW	None
R_5	200 kΩ	1.0%	25 mW	Lightning: Power Cross
R_6	200 kΩ	1.0%	25 mW	Lightning: Power Cross
R_7	1 kΩ	2.0%	0.1 W	Lightning: Power Cross
R_8	1 kΩ	2.0%	0.1 W	Lightning: Power Cross
R_9	20 kΩ	—	10 mW	None
R_{10}	600 Ω	1.0%	1.6 W	14 W for 250 ms
R_9/R_1	100	0.5%	—	—
R_1/R_2	1	0.35%[2]	—	—
$(R_3 + R_6)/(R_4 + R_5)$	1	0.35%[2]	—	—

1. Continuous (RMS) power.
2. For 50 dB longitudinal balance; 0.2% for 58 dB balance.

Note: Fuses F1 and F2 provide fail-safe operation if excessive overvoltage conditions exist on Tip and Ring. They will not operate if the total power dissipation of the entire resistor network is ≤5.0 W @ 85 °C.

Applications (continued)

Resistor Module (continued)

Resistors R3—R6 set the gain of the SLIC in the transmit (2-wire to 4-wire) direction. This is shown in Figure 7.

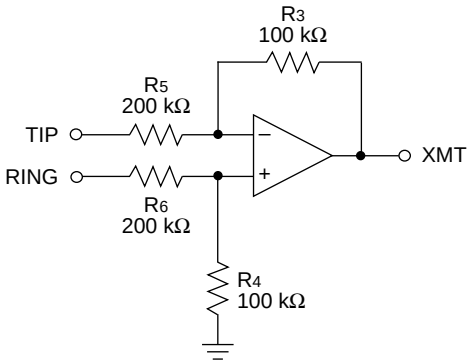

Figure 7. L8574 SLIC Matching Requirements

The matching of resistors R3—R6 will determine the gain accuracy of the SLIC; therefore, these resistors must be matched accordingly. Their matching requirements are given in Table 16.

Because of the high resistance values, the normal operating power of resistors R3—R6 will be relatively low. Given design margin and thick-film technology capabilities, a power rating of 250 mW for these resistors is not unreasonable.

Resistors R7 and R8 are used to couple the PT and PR current drive amplifiers to Tip and Ring. Since PT and PR drive amplifiers are current sources, the value of the series resistance does not affect the loop length or other performance of the SLIC, and may be arbitrarily high for protection purposes. A value of 1 kΩ is adequate for protection purposes.

Under normal operating conditions, these resistors will see the battery voltage less the Tip/Ring voltage. Assuming a Tip/Ring voltage of 6 V (representative of a short into a handset), the normal continuous operating power of R7 and R8 is given by:

(48 V – 6 V) E2/2.0 kΩ = 0.882 W per R7 and R8 resistor pair

882 mW/2 = 441 mW per resistor (R7 and R8)

Hence, the operating power rating of 500 mW for R7 and R8. This is the normal rating for R7 and R8 under normal operating conditions. The ability of these resistors to withstand fault conditions depends on the power rating.

Resistor R9 is also included on the thick-film resistor module. This resistor is used to set the gain of the battery noise cancellation circuit. See the Battery Noise Cancellation section of this data sheet for design equations to set the value of R9.

Power ringing is applied to the line circuit through resistor R10. One side of R10 is connected to L8574 node RSW. RSW is the output of the integrated solid-state ringing access switch, SW3. The other side of R10 is connected to the 200 Ω Ring feed resistor, R1. Resistor R10 also serves as a current-limiting resistor. Fault current through the solid-state ringing access switch, SW3, is limited by R10. SW3 is rated for 2 A maximum for a 10 µs x 1000 µs (lightning) pulse. Continuous current through this switch should be less than 150 mA. R10 in resistor modules *MMC* A31A8574AA and *MMC* A11A8574AA is chosen to be 600 Ω.

Protection

Because of the resistive feed architecture, a simple inexpensive protection scheme that does not require an external protection device may be used. The *MMC* A31A8574 resistor module has specifications which are qualified to ITU-T K20, *UL** 1459, *UL* 497A, FCC Part 68.302 (d) & (e), and REA Form 397G specification. The *MMC* A11A8574AA resistor module, in addition to meeting all the specifications of the *MMC* A31A8574, also meets Bellcore 1089 requirements.

Lightning and power-cross protection are provided by the two external dc feed (and current-limiting) resistors, R1 and R2, in the external resistor module. Under fault conditions, these resistors serve as fault current-limiting resistors. These resistors are designed to survive lightning surges. They are also designed to continuously dissipate 4 W each and to survive 1 Arms @ 60 Hz power crosses of ≤1 second in duration. Sustained power dissipation above these levels will cause degradation and eventual failure; however, the resistors are designed to fail gracefully under these conditions. Pins PT and PR are isolated from the loop by external 1000 Ω resistors, and pin V_{BF} is isolated from the loop by the Ring-side, 200 Ω dc feed resistor. These pins must have adequate fault protection which operates outside of their normal operating voltages. All three pins are protected by SCRs which clamp the surge currents (both positive and negative) to FGND. The

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Applications (continued)

Protection (continued)

sense inputs, TS and RS, are protected with diodes to battery (V_{BAT1}) and V_{CCA} and the series high-value external resistors which connect them to Tip and Ring. Because the battery noise cancellation input CBN is connected to pin V_{BF} through a 0.1 µF capacitor, it must also be protected. Internally, it is protected with an 8 V zener diode connected to V_{CCA}. An external resistor of at least 3 kW (5 kW is recommended) is required to limit the surge current. No external protection device is required.

Tip/Ring Drivers

The L8574 has two Tip/Ring drivers with outputs called PT and PR. Each driver operates as a current source capable of sinking or sourcing adequate ac signal current plus the dc bias current that is required during on-hook transmission.

Receive Interface

The receive interface circuitry couples the differential signal on receive inputs IRCV and RCVN to the Tip/Ring drivers. Input IRCV is a low-impedance (<5 Ω) current input while RCVN is a high-impedance voltage input. Internal feedback forces the voltage at IRCV to be equal to RCVN so that a voltage applied to RCVN causes a current flow out of IRCV which equals that voltage divided by the impedance connected from IRCV to AGND (assuming the input voltage is referenced to AGND).

The receive interface and Tip/Ring drivers provide a current gain of 200; i.e., a differential output current flows from PT to PR which is 200 times the current flowing into IRCV. The receive interface also provides a level shift since the inputs, IRCV and RCVN, are referenced to analog ground, while the outputs, PT and PR, swing between V_{CCA} and V_{BAT1}. The receive interface ensures that the input current is not converted to a common-mode current at PT and PR.

Transmit Interface

The transmit interface circuitry interfaces the differential voltage on Tip and Ring to transmit output XMT. The Tip/Ring differential voltage (both ac and dc) appears on output XMT with a gain of 0.5. The transmit interface uses an operational amplifier with four external resistors to perform a differential to single-ended conversion. The operational amplifier inputs are TS and RS. Output XMT is referenced to ground (AGND). The longitudinal balance and gain accuracy at XMT depends on the matching of the external resistors (0.35%). Because a large dc potential exists at XMT, a capacitor must be used to couple the ac signal to the low-voltage codec circuitry.

Battery Noise Cancellation

The battery noise cancellation circuit senses the ac noise on the battery via the capacitor connected from input CBN to V_{BF}. It couples this noise, 180° out of phase, to the Ring current drive amplifier. This cancels the battery noise that is coupled to the Ring through the feed resistor connected to V_{BF}.

Additionally, it ensures longitudinal balance, which depends only on the matching of the battery feed resistors by creating an ac ground at V_{BF} with respect to signals on the Ring lead.

For the cancellation to operate properly, both the phase and gain must be accurate. The battery noise cancellation gain is a transconductance which is equal to 100 divided by the resistor connected from RGBN to ground (AGND). This value must be equal to the reciprocal of the dc feed resistor (1/200). That is:

$100/R_9 = 1/200$
$R_9 = 20\ k\Omega$

It is advantageous if resistors R_9 and R_1 are matched and tracked thermally, i.e., located on the same film integrated circuit (FIC).

PSRR can be improved by adding a 47 pF capacitor in series with a 50 kΩ resistor from R_{GBN} to ground.

Also, to implement the battery noise cancellation function, connect the following circuit from CBN to V_{BF} and analog ground.

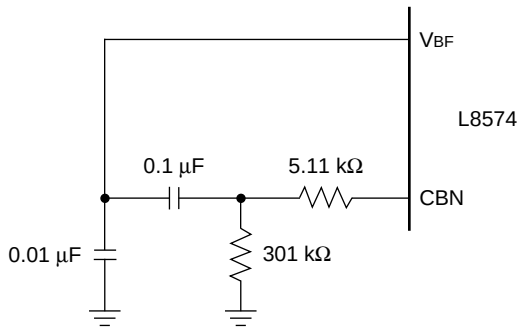


Figure 8. Implementing the Noise Cancellation Function

Applications (continued)

On-Hook Transmission

During the on-hook transmission and talk/on-hook transmission states, the L8574 provides 750 µA dc bias current out of the Tip/Ring current driver amplifiers. This creates a dc voltage drop across the external 19.6 kΩ resistors, R_{BIAS1} and R_{BIAS2}, which provides sufficient dc bias to support on-hook transmission. The switchhook detector is adjusted to compensate for this dc bias current. The L8574 is able to support on-hook transmission to drive a 3.17 dBm signal into a 600 Ω or 900 Ω ac loop. The capacitors, C_{BIAS1} and C_{BIAS2}, provide an ac path so transmission is not distorted by R_{BIAS1} and R_{BIAS2}. Zener diode, D_{SPEED}, reduces the settling time transition from on- to off-hook.

Parallel Data Interface

A 6-wire parallel interface (CE, CS, B0, B1, B2, and B3) is used to pass control information from the control logic on the line card to the L8574. The L8574 has eight operating states. These states are selected using three logic input bits, B0—B2, according to the truth table shown in Table 14. Logic input B3 operates a relay driver independent of the state of bits B0—B2. Data on the parallel data bus, B0—B3, is loaded into a 4-bit latch on the L8574 on the low-to-high transition of the channel select lead CS. Changes in the data at inputs B0—B3 do not affect the L8574 while CS is either low or high. A low on channel enable lead CE asynchronously resets the 4-bit latch to 1111 (scan state with the relay driver off) and disables the channel select lead CS (i.e., CS is prevented from loading any data into the 4-bit latch). A high on CE enables CS. State transitions and delays between transitions are left to the discretion of the user since, except for fault conditions, the state of the L8574 depends only on the external control provided through the logic interface.

Supervision

The L8574 offers the ring trip, loop closure, and thermal shutdown functions. The status of these functions are provided as device outputs. The outputs of the ring trip and off-hook supervision detectors are multiplexed into a single output called NSTAT. The device state determines which output is connected to NSTAT. The device state table, Table 14, details which supervision output (loop closure or ring trip) is seen at NSTAT during a given device state.

Detector values are independent of office battery and are valid over the entire range of V_{BAT1} and V_{BAT2}. However, NSTAT must indicate an on-hook (NSTAT = 1) if either V_{BAT1} or V_{BAT2} is disconnected (open circuit) from its dc source and an off-hook (NSTAT = 0) if the L8574 is in thermal shutdown. V_{BAT1} and V_{BAT2} are defined as disconnected depending on the voltage at the power supply pins as follows (the pins of supplies which have more than one pin are shorted together):

If $V_{BAT1} \leq -20$ V (i.e., more negative than –20 V) and $V_{BAT2} \leq -20$ V, then NSTAT must operate normally.
If $V_{BAT1} \geq -10$ V (i.e., more positive than –10 V) or $V_{BAT2} \geq -10$ V, then NSTAT must be on-hook (NSTAT = 1).

The status of the thermal shutdown circuit is output on B3 when CS is high (thermal shutdown = 0 V).

Off-Hook Detection

The off-hook or loop closure threshold on the L8574 SLIC is internally fixed. Off-hook is indicated (NSTAT = 0) if the loop resistance is a maximum 2700 Ω. On-hook is indicated (NSTAT = 1) if the loop resistance is a minimum 4400 Ω.

Ring Trip

The ring trip threshold is set by resistor R_{10} in the resistor module. With R_{10} set to 600 Ω, the circuit is guaranteed to ring trip up to 1840 Ω. With a 20 Hz ringing source, the trip time is guaranteed less than 200 ms. The ring trip circuit assumes uses of battery-backed ringing. Pretrip immunity is such that a load across Tip and Ring of 10 kΩ in parallel with an 8 µF capacitor will not cause ring trip. Three external components are required for ring trip, a 1 MΩ resistor from R_{TS} to V_{BF}, resistor R_{10}, which is a 600 Ω resistor from R_{SW} to V_{BF}, and a 0.1 µF capacitor from R_{SW} to R_{TS}. The components required for ring trip circuit are shown in Figure 9. Note that R_{10} is implemented in the resistor module. All other components are discrete.

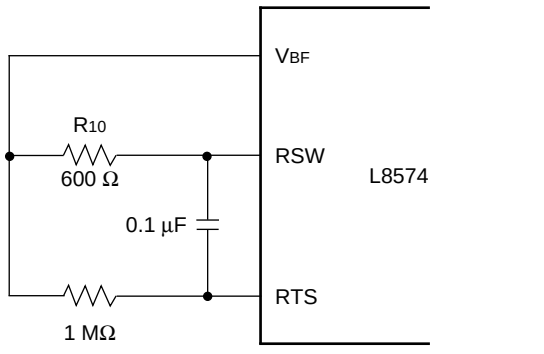


Figure 9. Ring Trip Threshold

Applications (continued)

Thermal Shutdown

If the silicon temperature rises above a nominal 145 °C, the L8574 will enter a thermal shutdown mode where all switches are off and the SLIC is in a state that is functionally equivalent to the disconnect state.

Relay Driver

The L8574 offers a single integrated relay driver. The relay driver output RDO is low (relay operated) when a low input on B3 is latched into the device. The driver has sufficient driver capability to provide 70 mA with a 1.0 V drop and 20 mA with a 0.4 V drop. Turn-off and turn-on times are a maximum of 10 μs.

Solid-State Ringing Access

The L8574 offers a solid-state ringing access switch for power ringing access and for the associated line break function. During the Ringing state, unbalanced battery-backed power ringing is applied to the Ring lead through resistors R_{10} and R_1 via ringing access switch SW3. The Ring drive amplifier of the L8574 SLIC is isolated from the subscriber loop via the integrated line break switch SW2 during the power ringing state. Since the Tip lead of the L8574 SLIC is tied to ground via resistor R_2, no line break function is associated with the Tip lead. The return ground path for the power ringing signal is via R_2.

The line break switch, SW2, is implemented using a high-voltage MOS transistor. This gives a linear V-I characteristic, as seen in Figure 3. The ON resistance of this switch is a nominal 50 Ω with a maximum 100 Ω. This switch is current limited to a nominal 35 mA and has a maximum off-state voltage rating of 320 V. The ringing access switch, SW3, is implemented using a pnpn type structure. This gives a linear V-I characteristic with an offset through the origin, as shown in Figure 4. This offset is less than 3 V. The off-state voltage rating is 500 V. Surge current (10 μs x 1000 μs) through this switch must be limited to less than 2 A. Steady state current through this switch must be limited to less than 150 mA.

Battery Supplies

There are two battery pins on the L8574, V_{BAT1} and V_{BAT2}. These two nodes may be connected to a common negative battery voltage. The magnitude of the battery should be sufficient to supply the required dc current into the specified (long) loop requirement.

Integrated into the L8574 is solid-state switch, SW1. SW1 has similar characteristics to the line break switch, SW2, including the 35 mA current limit. When SW1 is closed, the battery is applied through SW1 from the V_{BAT1} node. dc current from the battery will be limited by the current-limiting action of SW1. When SW1 is open, the battery at V_{BAT1} is isolated from the loop. The internal current-limit circuit is associated with the V_{BAT2} node; thus, when the current-limit circuit is active, the battery is applied to the subscriber loop through V_{BAT2} node and through the internal current-limiting circuitry, limiting dc current to the subscriber loop to 28 mA. When the current-limit circuit is not active, the voltage battery at V_{BAT2} is isolated from the loop.

The state of SW1 and the current-limiting circuit is controlled via logic inputs B0—B2. The L8574 state table (Table 14) details, for a given operational state, the condition of SW1 and the current-limit circuit.

dc Characteristics

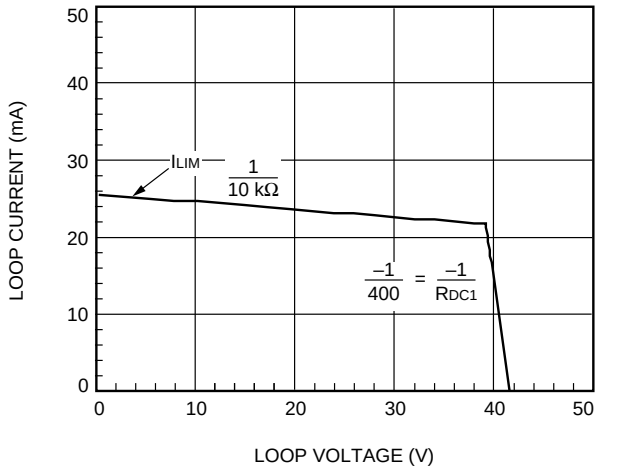
V-I Characteristics

Resistors R_1 and R_2 are the dc feed resistors. R_1 is connected from battery to Ring, and R_2 is connected from Tip to Ground. The dc loop current is fed to the subscriber loop via these resistors. When the L8574 is operating in the linear region of the V-I characteristic, the dc feed resistance or slope of this region of operation is determined by the sum of resistors R_1 plus R_2. The slope of the V-I characteristic will be –1/400 Ω. When the L8574 is operating in the current-limited region of the V-I characteristic, the current will be constant, regardless of loop length, and will be set and fixed by the internal current-limit circuit. The current limit is internally fixed to a nominal 28 mA. Connect a 33 nF capacitor from C_{LIM} to V_{BF}. Note that there is a slope of 1/10 kΩ to the V-I characteristic in the current-limited region of operation.

dc Characteristics (continued)

V-I Characteristics (continued)

In longer loops, the L8574 will operate in the linear region of operation, and in short loops, to conserve power, the L8574 will operate in the (fixed) current-limit region of operation. A typical V-I characteristic for the L8574 is shown in Figure 10 below.



Note: V_{BAT1} = –48 V, V_{BAT2} = –48 V; I_{LIM} = 28 mA; R_{DC} = 400 Ω.

Figure 10. Loop Current vs. Loop Voltage

Loop Length

The loop range is calculated as follows:

$R_L = (\{|V_{BAT}| – V_{OHLIM}\}/I_{LIMIT}) – R_1 – R_2$

Where:

R_L is the dc resistance of the subscriber loop.

V_{OHLIM} is the overhead or drop associated with the current-limit circuit, typically 2.2 V.

I_{LIMIT} is the minimum specified current that is required at the maximum loop length, typically 18 mA.

$|V_{BAT}|$ is the minimum magnitude of the battery—assume 43.2 V.

$R_1 = R_2$ = dc feed resistors = 200 Ω.

$R_L = (\{43.2\ V – 2.2\ V\}/0.018\ A) – 200\ \Omega – 200\ \Omega = 1877\ \Omega$.

ac Design

Codec Features and Selection Summary

There are four key ac design parameters:

- **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set.
- **Transmit gain** is measured from the 2-wire port to the PCM highway.
- **Receive gain** is done from the PCM highway to the transmit port.
- **Hybrid balance network** cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. Below is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and μ-law/A-law selectability. This generation of codec has the lowest cost. It is most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components. It also adds several I/O latches that are needed in the application. It does not have the transmit op amp, since the transmit gain and hybrid balance are set internally.

ac Design (continued)

Codec Features and Selection Summary (continued)

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following:

- Will the application require only one value for each gain and impedance?
- Will the board be used in different countries with different requirements?
- Will several versions of the board be built? If so, will one version of the board be most of the production volume?
- Does the application need only real termination impedance?
- Does the hybrid balance need to be adjusted in the field?

Design Equations

The following section gives the relevant design equations to choose component values for any desired gain, termination, and balance network, assuming a complex termination is desired. Complex termination will be specified in one of the two forms shown below.

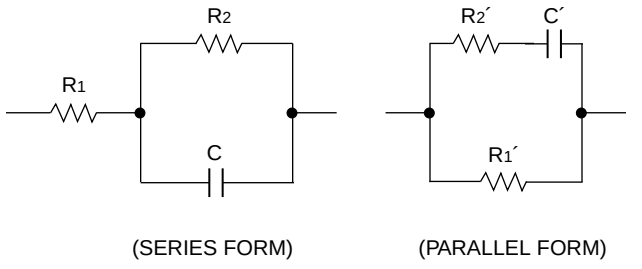


Figure 11. Equivalent Complex Terminations

Both forms are equivalent to each other, and it does not matter which form is specified. The component values in the interface circuit of Figure 11 are calculated assuming the parallel form is specified. If the termination impedance to be synthesized is specified in the series form, convert it to the parallel form using the equations below:

$$R_1' = R_1 + R_2$$

$$R_2' = \frac{R_1^2 + R_2 R_1}{R_2}$$

$$C' = \frac{C}{1 + 2\frac{R_1}{R_2} + \left(\frac{R_1}{R_2}\right)^2}$$

Note that if the termination impedance is specified as pure resistive:

$$R_2 = R_2' = 0 \text{ and } C = C' = \infty$$

Define the gain constant, K, as follows:

$$K_{RCV} = K_0 10^{Rx/20} \text{ for receive gain}$$

$$K_{TX} = \frac{1}{K_0} 10^{Tx/20} \text{ for transmit gain}$$

Where,

R_X = desired receive (or PCM to Tip/Ring) gain in dB

T_X = desired transmit (or Tip/Ring to PCM) gain in dB

$$K_0 = \sqrt{\frac{|Z_T|\ 1\ kHz}{600}} = \text{ power transfer ratio}$$

Where $|Z_T|$ (1 kHz) is the magnitude of the complex termination impedance Z_T being synthesized. This equation assumes that the TLP of the codec is 0 dBm referenced to 600 Ω.

The following equation applies when referring to Figure 11:

$$Z_T = \frac{\omega^2 C^2 R_1 R_2^2 + R_1 + R_2 - j\omega R_2^2 C}{1 + \omega^2 R_2^2 C^2}$$

Where,

$\omega = 2\pi f$

f = 1000 Hz

CR_1R_2 is defined per Figure 11 (series form), and

$$|Z_T| = \sqrt{\left(\frac{\omega^2 C^2 R_1 R_2^2 + R_1 + R_2}{1 + \omega^2 R_2^2 C^2}\right)^2 + \left(\frac{\omega R_2^2 C}{1 + \omega^2 R_2^2 C^2}\right)^2}$$

ac Design (continued)

Design Equations (continued)

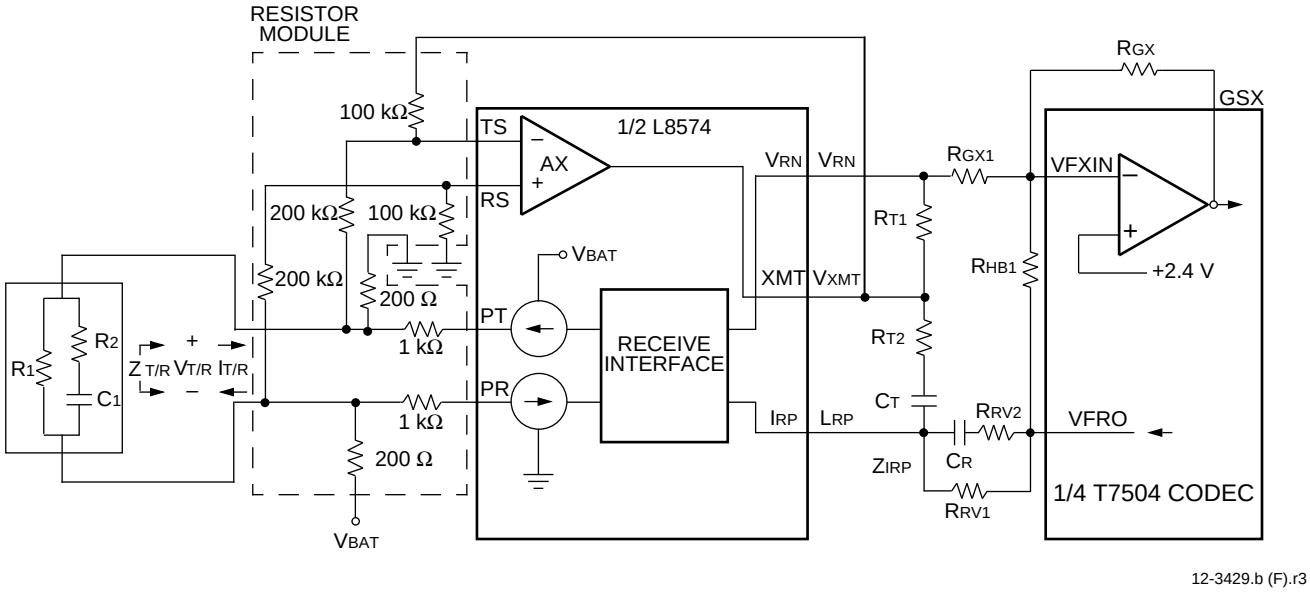


Figure 12. Initial ac Interface for Complex Termination Between L8574 SLIC and T7504 Codec
Note: dc Blocking Capacitor (C_B) Not Shown, C_T and C_R Separate

The Tip/Ring differential current is given by:

$$I_{T/R} = 200\left(I_{RP} - \frac{V_{RN}}{Z_{IRP}}\right)$$

The voltage at pin XMT is given by:

$$V_{XMT} = \frac{-V_{T/R}}{2}$$

The component values in the ac interface of Figure 12 are calculated (for the transmit and receive gains defined by the respective gain constants K_{RX} and K_{RCV}, and for the termination impedance seen in Figure 11) using the following equations:

$$R_{RV1} = \frac{100R_1'}{K_{RCV}}$$

$$R_{RV2} = \frac{100R_2'}{K_{RCV}}$$

$$C_R = \frac{K_{RCV}C'}{100}$$

$$\frac{R_{GX1}}{R_{GX1} + R_{T1}} = \frac{R_{RV1}}{100}\left(\frac{1}{600} - \frac{1}{R_1'}\right)$$

$400\ \Omega = 2 \times 200\ \Omega$ feed resistors

$$R_{GX} = 2 \times K_{TX}(R_{GX1} + R_{T1})$$

$$C_T = \frac{C'}{100}\left[1 + \frac{R_{GX1}}{R_{T1}}\left(1 + \frac{100R_1'}{R_{RV1}}\right)\right]$$

$$R_{T2} = \frac{R_2'C'}{C_T}$$

Note that the 200 Ω feed resistors contribute 400 Ω to the termination impedance. The termination impedance associated with the circuit in Figure 12 consists of this inherent 400 Ω feeding impedance in parallel with:

- A negative impedance, where,

$$\frac{2}{100} \times \frac{R_{GX1}}{R_{GX1} + R_{T1}}$$

- A positive impedance, where,

$$\left(R_{T2} + \frac{1}{j\omega C_T}\right) \bullet \left(\frac{R_{GX1} + R_{T1}}{R_{T1}}\right)$$

The negative and positive impedance terms are used to adjust the termination impedance from the inherent 400 Ω to any complex termination.

ac Design (continued)

Design Equations (continued)

Using the circuit of Figure 12, the ratio of capacitors C_T and C_R will affect the (transmit and receive) gain flatness, and to a lesser degree the return loss of the line circuit. Thus, depending on the requirements, C_T and C_R may need to be tight tolerance capacitors.

If this is the case, capacitors C_T and C_R may be combined into a single capacitor with a looser tolerance. This is illustrated in Figure 13.

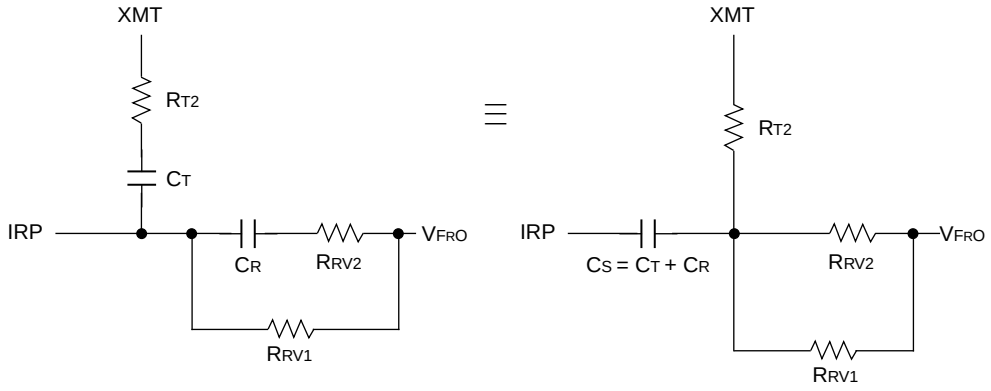


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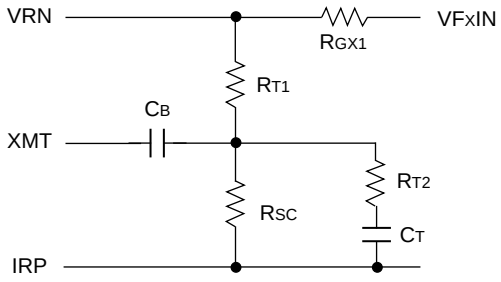
Figure 13. Revised ac Interface C_T and C_R Combined into a Single Capacitor C_S

To scale C_S (higher), increase C_T (and decrease R_{T2}) by increasing the $R_{GX1}/(R_{GX1} + R_{T1})$ ratio by rearranging the circuit in Figure 13 and by adding resistor R_{SC} from XMT to IRP as shown below.



12-3427.abF)

Figure 14. Addition of Resistor R_{SC} from XMT to IRP

Then,

$$\frac{R_{GX1}}{R_{GX1} + R_{T1}} = \frac{(R_{RV1} \parallel R_{SC})}{100}\left(\frac{1}{400} - \frac{1}{R_1'}\right) + \frac{R_{RV1}}{R_{RV1} + R_{SC}}$$

Once the gains and complex termination are set, if the hybrid balance network is identical to the termination impedance, then the hybrid balance is set by a single resistor (shown in Figure 12) and is computed as follows:

$$R_{HB} = \frac{R_{GX}}{K_{TX} \times K_{RCV}}$$

The L8574 SLIC is ground referenced. However, a +5 V only codec, such as T7504, is referenced to +2.5 V. The L8574 SLIC has sufficient dynamic range to accommodate an ac signal from the codec that is referenced to +2.5 V without clipping distortion. Furthermore, a dc current will flow between the L8574 SLIC and +5 V only codec. With the L8574 SLIC, this current will not affect ac performance, but it does waste power. To avoid wasted power consumption, blocking capacitors can be added. Capacitors should be placed to block any path from any low impedance +2.5 V biased node on the T7504 codec (or other +5 V only codec) to the SLIC. A blocking capacitor (C_B) has been added in the application drawing in Figure 14.

After the blocking capacitor C_B is added, the above component values may have to be adjusted slightly to optimize performance.

The effects of the blocking capacitor are best evaluated and optimized by circuit simulation. Contact your Lucent Technologies Microelectronics Group Account Manager for information on availability of a *PSPICE** model.

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ac Design (continued)

Design Equations (continued)

As a practical design example, design the interface for the following set of requirements:

RX = 0 dB

TX = 0 dB

ZT = 900 Ω

Hy = 900 Ω

First, calculate the gain constants:

$$Ko = \sqrt{\frac{|ZT|}{600}} = \sqrt{\frac{900}{600}} = 1.2247$$

$$KRCV = Ko10^{RX/20} = 1.2247 \times 10^{0/20} = 1.2247$$

$$KTX = \frac{1}{Ko}\ 10^{TX/20} = 0.8165$$

Second, calculate individual components:

RRV1 = 73,487 Ω

Choose a standard value component:

RRV1 = 73.2 kΩ

$$RRV2 = \frac{100\ RX'}{RRCV} = 0$$

$$CR = \frac{KRCVC'}{100} = \infty$$

$$\frac{RGX1}{RGX1 + RT1} = \frac{RRV1}{100}\left(\frac{1}{400} - \frac{1}{R1'}\right)$$

Choose RGX1 = 100 kΩ:

$$\frac{100\ k\Omega}{100\ k\Omega + RT1} = \frac{73.2\ k\Omega}{100}\left(\frac{1}{400} - \frac{1}{900}\right)$$

$$\frac{100\ k\Omega}{100\ k\Omega + RT1} = 1.01$$

RT1 = 0

$$CT = \frac{C'}{100}\left[1 + \frac{RGX1}{RT1}\left(1 + \frac{100\ R1'}{RRV1}\right)\right]$$

CT = ∞

$$RT2 = \frac{R2'C'}{CT} = 0$$

RGX = 2 x KTX (RGX1 + RT1)

RGX = 2 x 0.8165 (100 kΩ + 0)

RGX = 163.3 kΩ

Choose a standard value resistor:

RGX = 165 kΩ

$$RHB = \frac{RGX}{KTX \times KRCV}$$

$$RHB = \frac{165\ k\Omega}{0.8165 \times 1.2247} = 165\ k\Omega$$

Therefore, for this design example, use the following values in the circuit shown in Figure 12.

RT1 = 0 kΩ
RT2 = 0
RGX = 165 kΩ
RGX1 = 100 kΩ
RRV1 = 73.2 kΩ
RRV2 = 0
RHB1 = 165 kΩ
CT = ∞
CR = ∞

Figure 15 is the application circuit with the above values.

Application Diagram

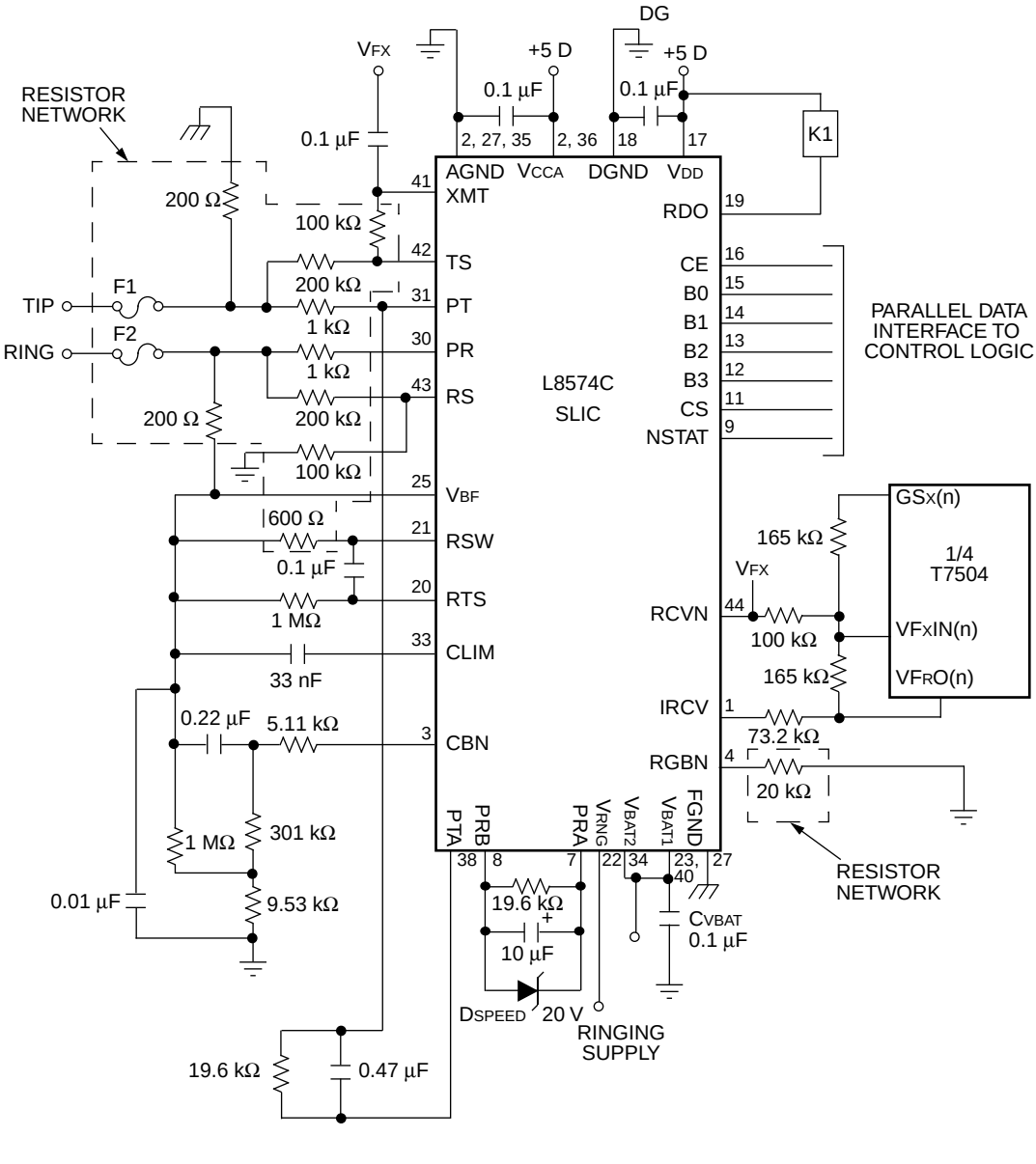

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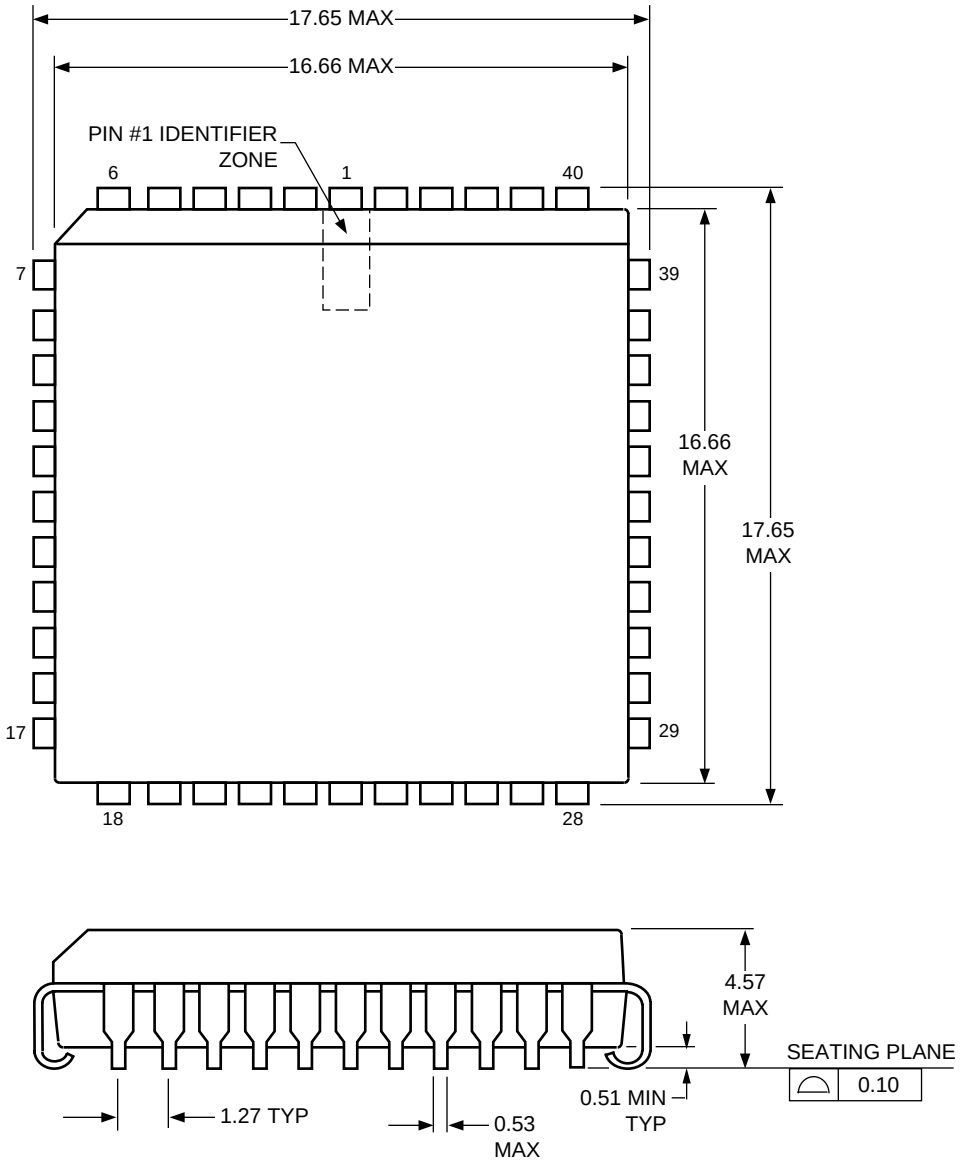
Figure 15. TR-57 Application Diagram

Outline Diagram

44-Pin PLCC

Dimensions are in millimeters.



5-2506 (C) r07

Ordering Information

Device Part No.	Description	Package	Comcode
LUCL8574DP-D	Resistive SLIC, Ring Relay, and Protector for Long Loop and TR-57 Applications	44-Pin PLCC (Dry-bagged)	107874794
LUCL8574DP-DT	Resistive SLIC, Ring Relay, and Protector for Long Loop and TR-57 Applications	44-Pin PLCC (Tape and Reel, Dry-bagged)	107840688

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