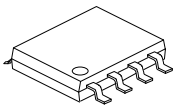
POWER FACTOR CORRECTED DIMMABLE LED DRIVER



SOP-8

■ DESCRIPTION

The UTC **L8532** is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. The device is designed to operate in critical conduction mode (CrM) and is suitable for flyback as well as buck topologies. Constant on time CrM operation is particularly suited for isolated flyback LED applications as the control scheme is straightforward and very high efficiency can be achieved even at low power levels. These are important in LED lighting to comply with regulatory requirements and meet overall system luminous efficacy requirements. In CrM, the switching frequency will vary with line and load and switching losses are low as recovery losses in the output rectifier are negligible since the current goes to zero prior to reactivating the main MOSFET switch.

The device features a programmable on time limiter, zero current detect sense block, gate driver, trans-conductance error amplifier as well as all PWM control circuitry and protection functions required to implement a CrM switch mode power supply. Moreover, for high efficiency, the device features low startup current enabling fast, low loss charging of the V_{CC} capacitor. The current sense protection threshold has been set at 500 mV to minimize power dissipation in the external sense resistor. To support the environmental operation range of Solid State Lighting, the device is specified across a wide junction temperature range of -40°C ~125°C.

■ FEATURES

* Very Low 24μA Typical Startup Current
* Constant On Time PWM Control
* Cycle-by-Cycle Current Protection
* Low Current Sense Threshold of 500mV
* Low 2mA Typical Operating Current
* Source 500mA/Sink 800mA Totem Pole Gate Driver
* Reference Design for TRIAC and Trailing Edge Line Dimmers
* Wide Operating Temperature Range
* No Input Voltage Sensing Requirement
* Enable Function and Overvoltage Protection

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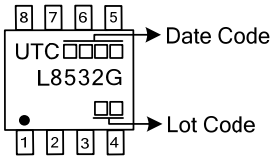
■ ORDERING INFORMATION

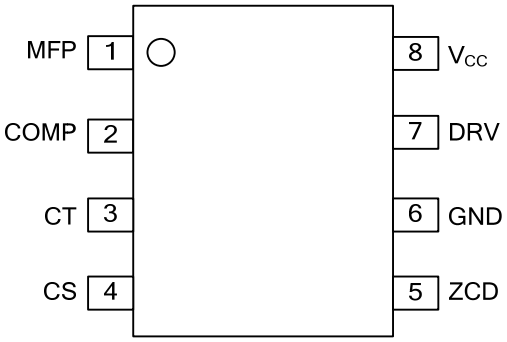
Ordering Number	Package	Packing
L8532G-S08-R	SOP-8	Tape Reel

L8532G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



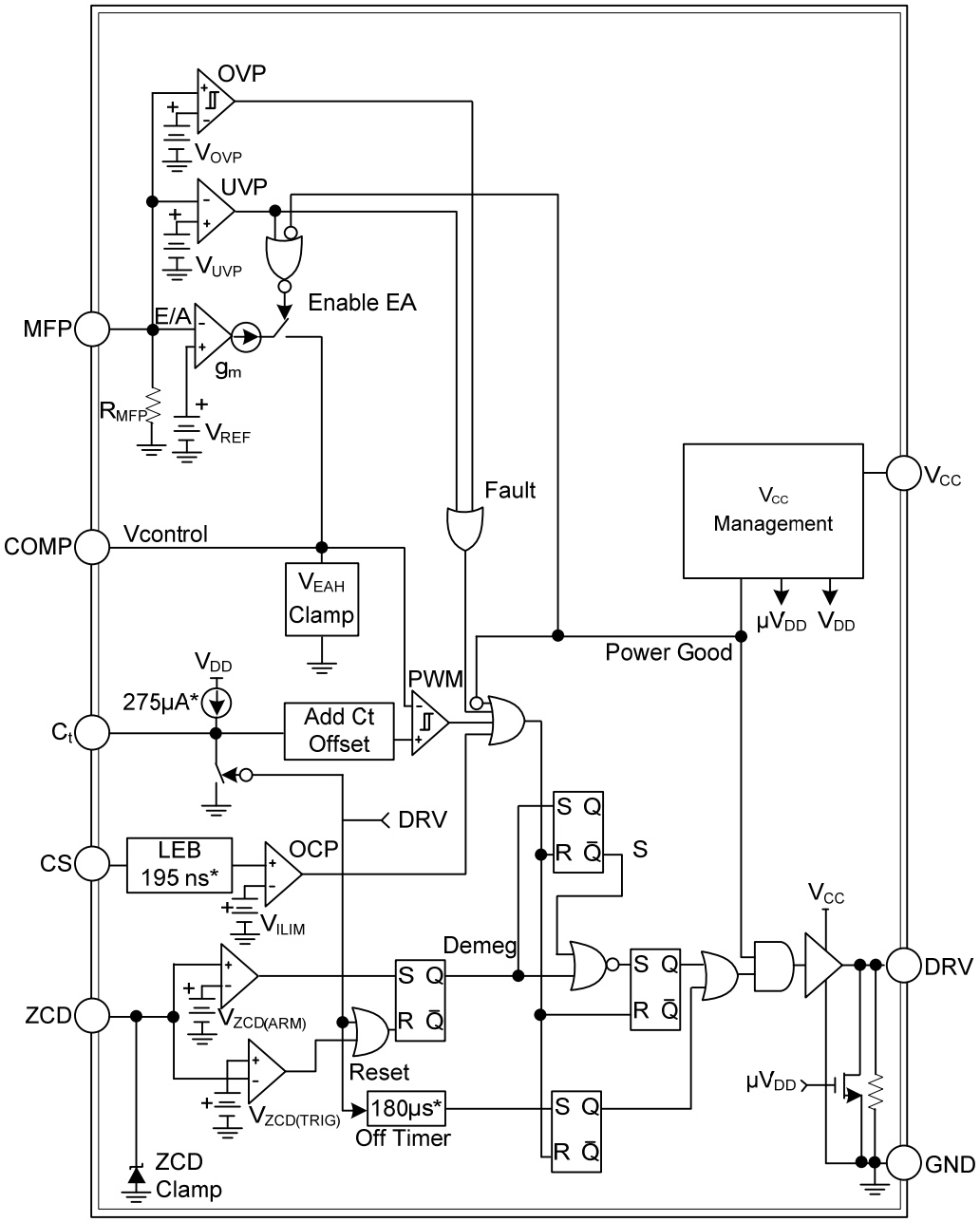
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	MFP	The multi-function pin is connected to the internal error amplifier. By pulling this pin below the V_{uvp} threshold, the controller is disabled. In addition, this pin also has an over voltage comparator which will disable the controller in the event of a fault.
2	COMP	The COMP pin is the output of the internal error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth. Normally this bandwidth is set at a low frequency (typically 10Hz~20Hz) to achieve high power factor and low total harmonic distortion (THD).
3	CT	The C_T pin sources a regulated current to charge an external timing capacitor. The PWM circuit controls the power switch on time by comparing the C_T voltage to an internal voltage derived from $V_{Control}$. The C_T pin discharges the external timing capacitor at the end of the on time cycle.
4	CS	The CS input is used to sense the instantaneous switch current in the external MOSFET. This signal is filtered by an internal leading edge blanking circuit.
5	ZCD	The voltage of an auxiliary zero current detection winding is sensed at this pin. When the ZCD control block circuit detects that the winding has been demagnetized, a control signal is sent to the gate drive block to turn on the external MOSFET.
6	GND	This is the analog ground for the device. All bypassing components should be connected to the GND pin with a short trace length.
7	DRV	The high current capability of the totem pole gate drive (+0.5/-0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs. The driver stage provides both passive and active pull down circuits that force the output to a voltage less than the turn-on threshold voltage of the power MOSFET when $V_{CC(on)}$ is not reached.
8	V_{CC}	This pin is the positive supply of the controller. The circuit starts to operate when V_{CC} exceeds $V_{CC(on)}$, nominally 12V and turns off when V_{CCgoes} below $V_{CC(off)}$, typically 9.5V. After startup, the operating range is 10.2V up to 20V.

■ BLOCK DIAGRAM



* Typical Values Shown All SR Latches are Reset Dominant

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
MFP Voltage	V_{MFP}	-0.3~10	V
MFP Current	I_{MFP}	±10	mA
COMP Voltage	$V_{Control}$	-0.3~6.5	V
COMP Current	$I_{Control}$	-2~10	mA
Ct Voltage	V_{Ct}	-0.3~6	V
Ct Current	I_{Ct}	±10	mA
CS Voltage	V_{CS}	-0.3~6	V
CS Current	I_{CS}	±10	mA
ZCD Voltage	V_{ZCD}	-0.3~10	V
ZCD Current	I_{ZCD}	±10	mA
DRV Voltage	V_{DRV}	-0.3~V_{CC}	V
DRV Sink Current	$I_{DRV(sink)}$	800	mA
DRV Source Current	$I_{DRV(source)}$	500	mA
Supply Voltage	V_{CC}	-0.3~20	V
Supply Current	I_{CC}	±20	mA
Power Dissipation (T_A =70°C, 2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)	P_D	450	mW
Operating Junction Temperature Range	T_J	-40~125	°C
Maximum Junction Temperature	$T_{J(MAX)}$)	150	°C
Storage Temperature Range	T_{STG}	-65~150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. As mounted on a 40×40×1.5mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	178	°C/W

■ ELECTRICAL CHARACTERISTICS

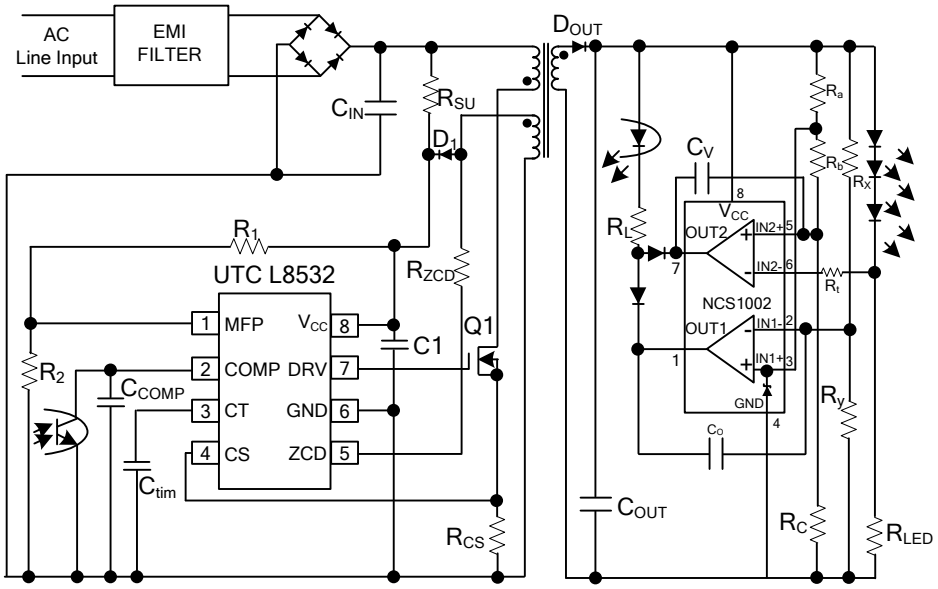
V_{MFP}=2.4V, $V_{Control}$= 4V, Ct=1nF, V_{CS}=0V, V_{ZCD}=0V, C_{DRV}=1nF, V_{CC}=12V, unless otherwise specified (For typical values, T_J=25°C. For min/max values, T_J=-40°C~125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP AND SUPPLY CIRCUITS						
Startup Voltage Threshold	$V_{CC(on)}$	V_{CC} Increasing	11	12	12.5	V
Minimum Operating Voltage	$V_{CC(off)}$	V_{CC} Decreasing	8.8	9.5	10.2	V
Supply Voltage Hysteresis	H_{UVLO}		2.2	2.5	2.8	V
Startup Current Consumption	$I_{CC(startup)}$	0V<V_{CC} <$V_{CC(on)}$ -200 mV		24	35	uA
No Load Switching Current Consumption	I_{CC1}	C_{DRV}=Open, 70kHz Switching, V_{CS} =2V		1.4	1.7	mA
Switching Current Consumption	I_{CC2}	70kHz Switching, V_{CS}=2V		2.1	2.6	mA
Fault Condition Current Consumption	$I_{CC(fault)}$	No Switching, V_{MFP}=0V		0.75	0.95	mA
Overvoltage And Undervoltage Protection						
Overvoltage Detect Threshold	V_{OVP}/V_{REF}	V_{MFP}= Increasing	105	106	108	%
Overvoltage Hysteresis	$V_{OVP(HYS)}$		20	60	100	mV
Overvoltage Detect Threshold Propagation Delay	t_{OVP}	V_{MFP}=2~3V ramp, dV/dt=1V/us, V_{MFP}=V_{OVP} to V_{DRV}=10%		500	800	ns
Undervoltage Detect Threshold	V_{UVP}	V_{MFP}=Decreasing	0.25	0.31	0.4	V
Undervoltage Detect Threshold Propagation Delay	t_{UVP}	V_{MFP}=1~0V ramp, dV/dt=10V/us, V_{MFP}=V_{UVP} to V_{DRV}= 10%	100	200	300	ns
ERROR AMPLIFIER						
Voltage Reference	V_{RER}	T_J=25°C	2.475	2.500	2.525	V
		T_J=-40°C~125°C	2.460	2.500	2.540	
Voltage Reference Line Regulation	$V_{REF(line)}$	$V_{CC(on)}$+200mV<V_{CC}<20V	-10		10	mV
Error Amplifier Current Capability	$I_{EA(sink)}$	V_{MFP}=2.6V	6	10	20	uA
	$I_{EA(sink)OVP}$	V_{MFP}=1.08×V_{REF}	20	30	40	
	$I_{EA(source)}$	V_{MFP}=0.5V	-110	-280	-350	
Transconductance	gm	V_{MFP}=2.4~2.6V, T_J= 25°C	90	110	120	us
		V_{MFP}=2.4~2.6V, T_J= -40~125°C	70	110	135	
Feedback Pin Internal Pull−Down Resistor	R_{MFP}	V_{MFP}=V_{UVP} to VREF	1		10	MΩ
Feedback Bias Current	I_{MFP}	V_{MFP}=2.5V	1	1.3	1.6	uA
Control Bias Current	$I_{Control}$	V_{MFP}=0V	-1		1	uA
Maximum Control Voltage	V_{EAH}	$I_{Control(pullup)}$=10uA, V_{MFP}=V_{REF}	5	5.5	6	V
Minimum Control Voltage to Generate Drive Pulses	$Ct_{(offset)}$	$V_{Control}$=Decreasing until V_{DRV} is low, V_{Ct}= 0V	0.37	0.65	0.88	V
Control Voltage Range	$V_{EA(DIFF)}$	V_{EAH}-$Ct_{(offset)}$	4.5	4.9	5.3	V
RAMP CONTROL						
Ct Peak Voltage	$V_{Ct(MAX)}$	V_{COMP}=open	4.775	4.93	5.025	V
On Time Capacitor Charge Current	I_{charge}	V_{COMP}=open, V_{Ct}= 0V to $V_{Ct(MAX)}$	235	275	297	uA
Ct Capacitor Discharge Duration	$t_{Ct(discharge)}$	V_{COMP}=open, V_{Ct}=$V_{Ct(MAX)}$ -100~500mV		50	150	ns
PWM Propagation Delay	t_{PWM}	dV/dt=30V/us, V_{Ct}=$V_{Control}$-$C_{t(offset)}$ to V_{DRV}=10%		550	600	ns

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZERO CURRENT DETECTION						
ZCD Arming Threshold	$V_{ZCD(ARM)}$	V_{ZCD}=Increasing	1.25	1.4	1.55	V
ZCD Triggering Threshold	$V_{ZCD(TRIG)}$	V_{ZCD}=Decreasing	0.6	0.7	0.83	V
ZCD Hysteresis	$V_{ZCD(HYS)}$		500	700	900	mV
ZCD Bias Current	I_{ZCD}	V_{ZCD}= 5V	-2		+2	uA
Positive Clamp Voltage	$V_{CL(POS)}$	I_{ZCD}=3mA	16	18	20	V
Negative Clamp Voltage	$V_{CL(NEG)}$	I_{ZCD}=-2mA	-0.9	-0.7	-0.5	V
ZCD Propagation Delay	t_{ZCD}	V_{ZCD}=2V~0V ramp, dV/dt=20V/us, V_{ZCD}=$V_{CD(TRIG)}$ o V_{DRV}= 90%		200	270	ns
Minimum ZCD Pulse Width	t_{SYNC}			70		ns
Maximum Off Time in Absence of ZCD Transition	t_{start}	Falling V_{DRV}=10% to Rising, D_{RV}=90%	75	165	300	us
DRIVE						
Drive Resistance	R_{OH}	I_{source}=100mA		12	20	Ω
	R_{OL}	I_{SINK}=100mA		6	13	
Rise Time	t_{rise}	10%~90%		35	80	ns
Fall Time	tfall	90% to 10%		25	70	ns
Drive Low Voltage	$V_{out(start)}$	V_{CC}=$V_{CC(on)}$-200mV, I_{sink}=10mA			0.2	V
CURRENT SENSE						
Current Sense Voltage Threshold	V_{ILIM}		0.45	0.5	0.55	V
Leading Edge Blanking Duration	t_{LEB}	V_{CS}=2V, V_{DRV}= 90%~10%	100	195	350	ns
Overcurrent Detection Propagation Delay	t_{CS}	dV/dt=10V/us, V_{CS}=V_{ILIM} to V_{DRV}= 10%	40	100	170	ns
Current Sense Bias Current	I_{CS}	V_{CS}= 2 V	-1		1	uA

■ TYPICAL APPLICATION CIRCUIT



Simplified Flyback Application with Secondary side Constant Current Control

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