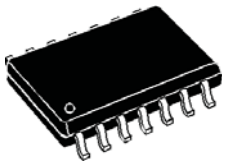
L6572

High voltage smart ballast controller

Datasheet – production data

Features

- 600 V half-bridge driver
- Integrated bootstrap diode
- Failure protection logic
- Programmable deadtime
- Programmable preheated start
- Two-step dimming with programmable dimmed current
- Thermal powerboost
- Closed loop control operation



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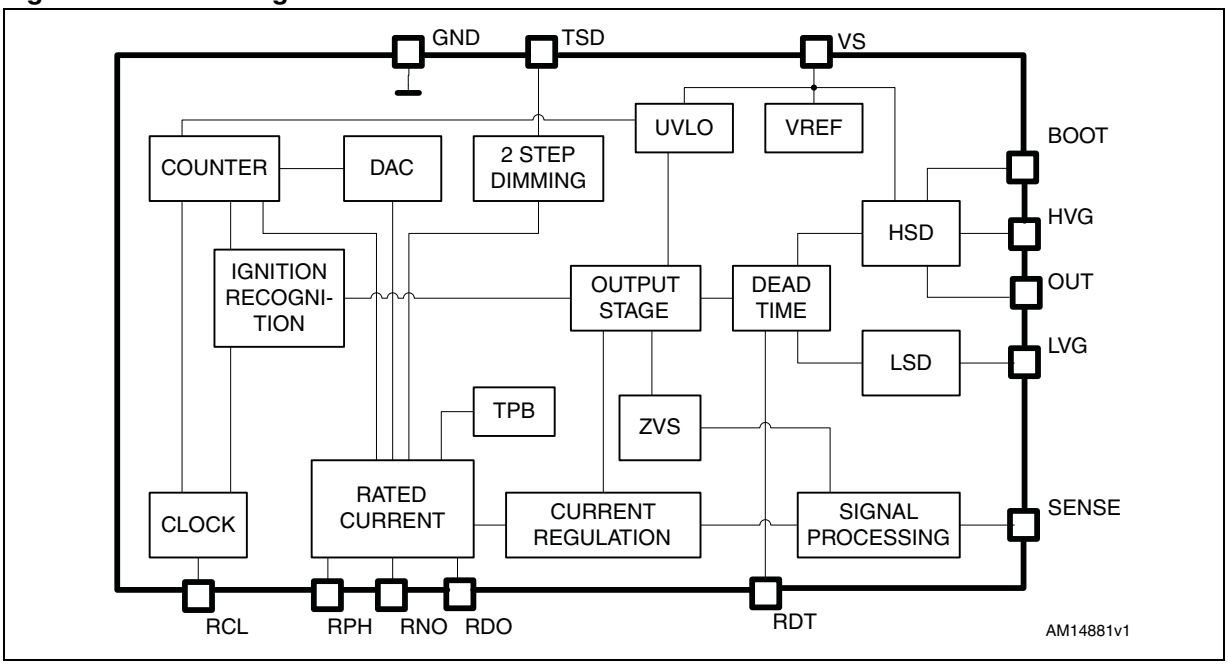
Applications

- CFLi
- Electronic ballast

Figure 1. Block diagram



Contents

1 Description

The L6572 is a high voltage half-bridge driver for current regulation, quasi-self-oscillating ballast.

It contains all functions that are needed to preheat the filaments, to ignite and to operate a fluorescent lamp.

During normal operation of the lamp, the ballast operates either with the nominal or with a reduced resonant current which results in a nominal or a reduced light output of the lamp.

A change between those two possible light outputs of the lamp is triggered by disconnecting the mains voltage for a short time (two-step dimming). The filaments are preheated before the lamp is re-ignited after every disconnection of the mains voltage.

A powerboost function is included to accelerate the startup behavior of the fluorescent lamp when the junction temperature is below a defined temperature.

An undervoltage lockout is active while loading the blocking capacitor via the startup resistor as long as the supply voltage VS is below a defined value. The bootstrap capacitor is loaded before the high-side transistor is switched on the first time to start the oscillation of the ballast.

The output drivers are designed to drive external N-channel power MOSFET and IGBT (max. input capacity $C_{input} \leq 1$ nF) without any additional gate resistor.

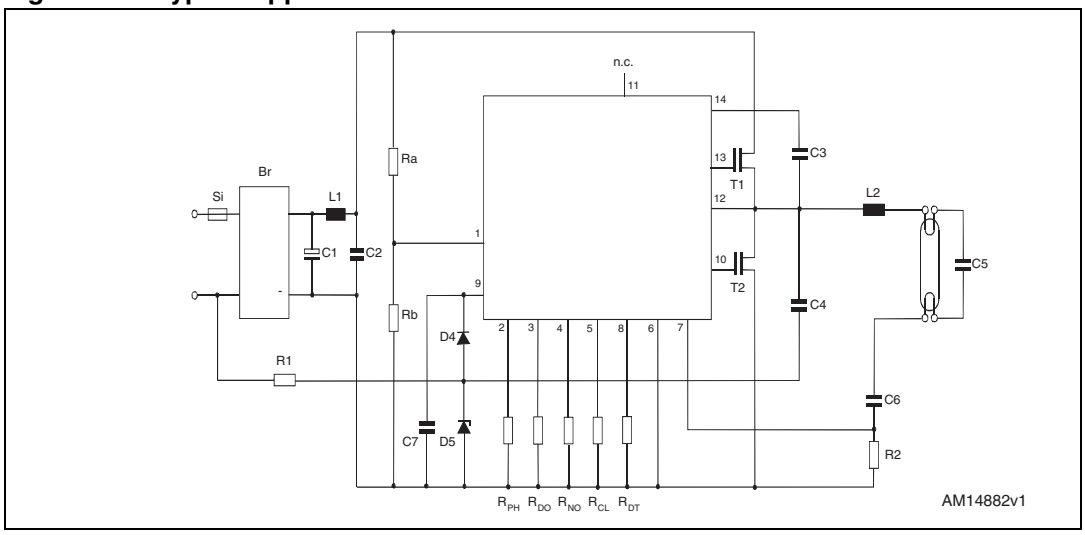
A constant deadtime for both switches can be programmed with one external resistor.

The rated resonant current for the nominal lamp operation with nominal light output, the dimmed operation with reduced light output and the preheating phase is defined by three external resistors considering the shunt resistance.

The ratio X_{PB} between the nominal rated resonant current during normal operation and the powerboost phase is fixed internally. The time lapse is given by an internally fixed number of load/unload-cycles of an internal capacitor.

An absolute time base, used to regulate periods and intervals, is given by the duration of a load/unload-cycle of the internal capacitor with a load current that is defined with an external resistor.

Figure 2. Typical application



2 Pin connection

Figure 3. Pin connection

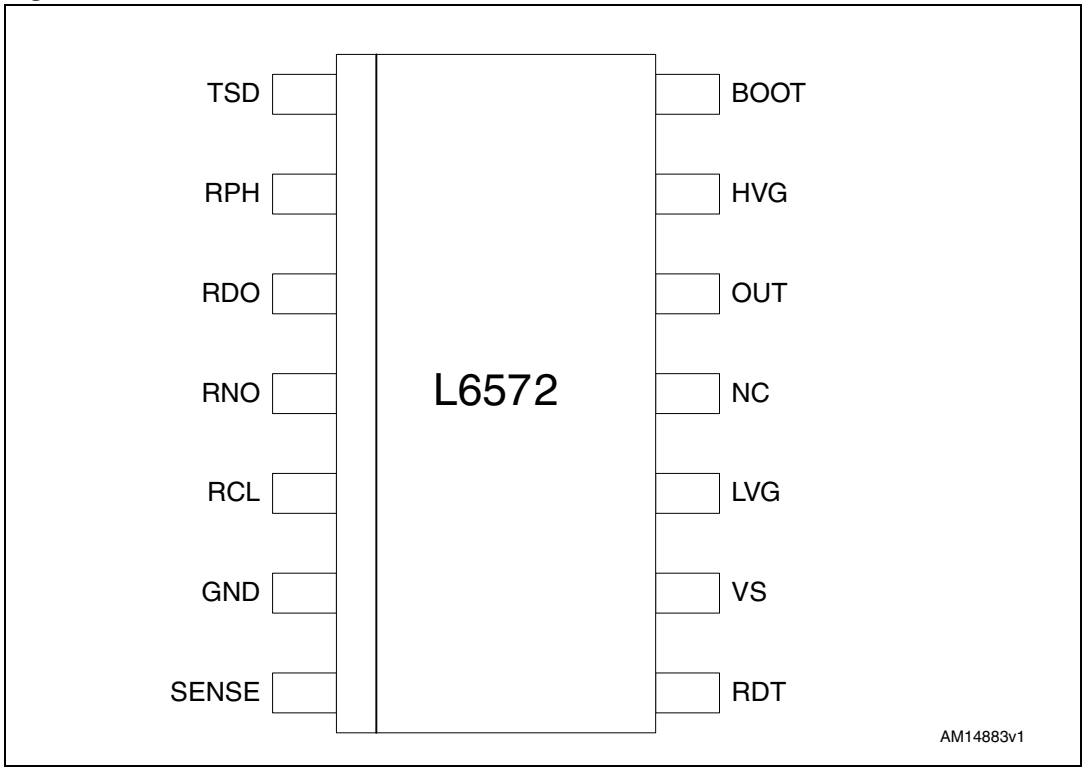


Table 1. Pin description

Symbol	Pin	Description
TSD	1	Input voltage for dimmed operation detection. Connected to ground if unused.
RPH	2	Preheating current programming. A resistor placed between this pin and ground defines the rated load current during the preheating phase.
RDO	3	Reduced light level current programming. A resistor placed between this pin and ground defines the rated load current during the dimmed operation.
RNO	4	Nominal light level current programming. A resistor placed between this pin and ground defines the rated load current during the normal operation.
RCL	5	Time base period programming.
GND	6	Reference voltage of the device.
SENSE	7	Current sense input. This pin has to be connected to a shunt resistor placed in series with the load.
RDT	8	Deadtime programming. A resistor paced between this pin and ground allows the deadtime to be programmed between LSG and HSG pulses in the range (1 µs to 5 µs).
VS	9	Supply voltage of the device. A bulk capacitor and an optional ceramic capacitor must be connected between this pin and ground.

Table 1. Pin description (continued)

Symbol	Pin	Description
LVG	10	Low-side transistor driver. The gate of an N-channel MOSFET or IGBT having an equivalent gate capacitance lower than 1 nF can be directly connected to this pin.
NC	11	Unconnected pin for creepage purpose
OUT	12	Reference voltage of the floating gate driver. To be connected to the middle point of the half-bridge.
HVG	13	High-side transistor driver. The gate of an N-channel MOSFET or IGBT having an equivalent gate capacitance lower than 1 nF can be directly connected to this pin.
BOOT	14	Supply voltage of the floating gate driver. A ceramic bootstrap capacitor must be placed between this pin and OUT pin

3 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage	15	V
VRDT	Voltage control resistor	5	V
VRPH			
VRNO			
VRPB			
VRCL			
VSENSE	Sense input voltage	±10	V
VLVG	Low-side switch gate output	VS	V
VOUT	High-side switch source output	-2,5 to VBOOT - VS	V
VHVG	High-side switch gate output	-2,5 to VBOOT - VS	V
VBOOT	Floating supply voltage	580	V
VBOOT/OUT	Floating supply vs out voltage	VS	V
dVBOOT/dt	VBOOT slew rate (repetitive)	± 50	V/ns
dVOUT/dt	VOUT slew rate (repetitive)	± 50	V/ns
ITSD(1)	Supply current tsd-function	1,5	mA

1. The device has an internal Zener clamp between TSD and GND (typical 12.8 V)

Table 3. Recommended operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply voltage	12	15	V
V_{BOOT}	Floating supply voltage	-	500	V
V_{OUT}	High-side switch source output	-1	VBOOT-VS	V
V_{NO}, V_{DO}	Voltages at pins Rno, Rdo	0.3		V
VPH(1)	Voltage on pin RPH	0.3	4.8	V

1. No external circuitry has to force any voltage on the pin RPH while the undervoltage lockout is activated.

Table 4. Thermal characteristics

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Max. thermal resistance junction-ambient	120	°C/W
T_{STG}	Storage temperature	-40 to 150	°C
T_J	Junction temperature	-40 to 150	°C
T_{AMB}	Ambient temperature (operative)	-40 to 130	°C

4 Electrical characteristics

(V_S = 14.4 V, V_{BOOT} - V_{out} = 14.4 V, T_{AMB} = 25 °C, unless otherwise specified)

Table 5. Electrical characteristics

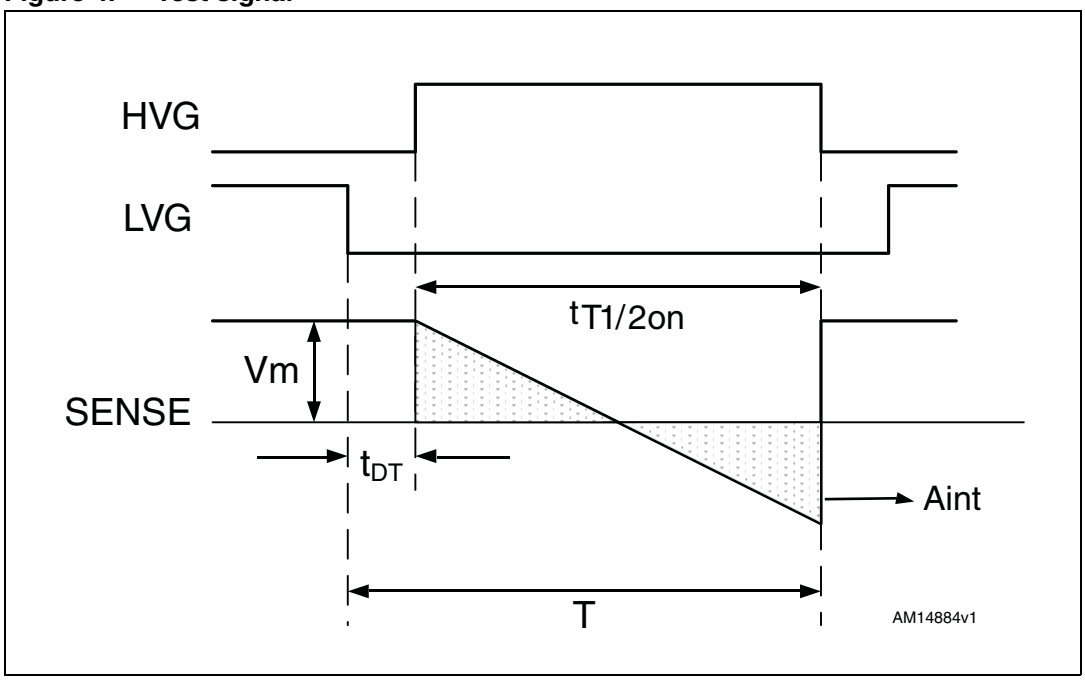
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SUVP}	V_S turn-ON threshold		10.1	11	11.9	V
V_{SUVN}	V_S turn-OFF threshold		7.3	8	8.7	V
V_{SUVH}	V_S hysteresis		2.7	3	3.3	V
I_{SU}	Startup current	$V_S < V_{SUVP}$		160	250	µA
I_q	Quiescent current	$V_S > V_{SUVP}$	1	2		mA
I_{BOOTLK}	BOOT pin leakage current	V_{BOOT} = 580 V			5	µA
I_{OUTLK}	OUT pin leakage current	V_{OUT} = 562 V			5	µA
$I_{HVG\ SO}$	High-side driver source current	V_{HVG} - V_{OUT} = 5 V	20	40		mA
$I_{HVG\ SI}$	High-side driver sink current	V_{HVG} - V_{OUT} = 5 V	40	50		mA
$I_{LVG\ SO}$	Low-side driver source current	V_{LVG} = 5 V	20	40		mA
$I_{LVG\ SI}$	Low-side driver sink current	V_{LVG} = 5 V	40	50		mA
t_{DT}	Programmable deadtime	R_{DT} = 27 kΩ	1.95	2.50	3.05	µs
t_{DT}	Minimum deadtime	R_{DT} = 14 kΩ (1)	1			µs
t_{DT}	Maximum deadtime	R_{DT} = 40 kΩ (1)			5	µs
f_{CL}	Frequency clock generator	R_{CL} = 47 kΩ	72	90	108	kHz
f_{CL}	Minimum frequency	R_{CL} = 220 kΩ (1)	12			kHz
f_{CL}	Maximum frequency	R_{CL} = 22 kΩ (1)			250	kHz
$t_{T1/2on}$	Time with T1/2 switched on during preheating phase	R_{PH} = 20 kΩ, R_{DT} = 27 kΩ testing signal: test A	3.60	4.17	4.70	µs
$t_{T1/2on}$	Time with T1/2 switched on during normal operation	RNO = 27 kΩ, R_{DT} = 27 kΩ testing signal: test B	6.40	7.50	8.40	µs
$t_{T1/2on}$	Time with T1/2 switched on during dimmed operation	RDO = 27 kΩ, R_{DT} = 27 kΩ testing signal: test B	6.40	7.50	8.40	µs
XPB	XPB = $t_{T1/2on}$(powerb) / $t_{T1/2on}$(nom)	RNO = 27 kΩ, R_{DT} = 27 kΩ NO: test. signal: test B PB: test. signal: test C	1.24	1.34	1.42	
tdisc	Time to activate UVLO when VSENSE = VZVS	V_{LVG} = V_S	10	20	30	µs
VZVS	ZVS threshold referred to SENSE pin	(1)	330	385	440	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
TPB	Temperature threshold for powerboost activation	(1)	64	80	106	°C
VTSD	VTSD low voltage threshold		5.5	6.2	6.9	V
VTSD-Z	Zener voltage on TSD pin	ITSD = 600 µA (2)	11.5	12.8	14.0	V
ITSD	Current consumption TSD-function	VTSD = 11 V	30	40	50	µA

1. Guaranteed by design.
2. For a correct operation of the TSD function, the internal clamping diode has always to be turned on with the minimum supply voltage of the device.

Figure 4. Test signal



where:

- Test A: starting voltage Vm = ± 465 mV, half period T = 6,67 µs (f = 75 kHz; t_{DT} = 2,5 µs)
- Test B: starting voltage Vm = ± 340 mV, half period T = 10,0 µs (f = 50 kHz; t_{DT} = 2,5 µs)
- Test C: starting voltage Vm = ± 340 mV, half period T = 12,5 µs (f = 40 kHz; t_{DT} = 2,5 µs)
- T measured from the falling edge of HVG (LVG) to the falling edge of LVG (HVG).

5 Functional description

5.1 Signal processing block

The resonant current is detected with a shunt resistor which delivers a voltage signal to the SENSE pin that is related to the GND pin.

Voltages at the SENSE pin amount to approx. 400 $mV_{(rms)}$ during normal operation respectively up to 10 $V_{(peak)}$ during ignition.

An overriding of the amplifier is given by sense voltages above ± 4.5 V.

5.2 Current regulation

This block provides the lamp current regulation. It consists of one integrator that loads an internal capacity (C_{int}) with a current that is directly proportional (factor: Rint1) to the signal at the sense input. The output of the integrator is (T1/2 stands for "LVG or HVG MOSFET"):

Equation 1

$$V_{int} = \frac{1}{R_{int} \cdot C_{int}} \cdot \int_0^{\tau} V_{SENSE}(t)dt$$

(t = 0: T1/2 switched on; t = τ: T1/2 switched off).

The output signal of the integrator V_{int} is compared to the rated value (rated resonant current) programmed by RNO, RPH or RDO depending on the operational phase; the relevant comparator triggers the output stage block that switches off the current conducting power transistor.

The internal capacitor C_{int} is reset during the deadtime of the half-bridge (programmed by RDT).

5.3 ZVS control

Thanks to the implemented ZVS control function, the conducting transistor is switched off at the latest when the resonant current changes its direction. Therefore, the half-bridge operates in the inductive region of the resonance characteristics of the ballast. In the worst case, working close to the pole frequency is allowed.

5.4 Two-step dimming

The ballast operates the lamps with nominal or reduced light output. A change between these two operation modes is achieved by disconnecting the line voltage for a time t < tTSD.

An internal binary information cell changes its state at the end of every preheating phase. Depending on the state of this cell, the reduced or the nominal rated resonant current is given to the current regulation unit in order to operate the lamp with nominal or reduced light output.

The internal information cell is provided with the structure embedded in TSD pin and is able to keep its state as long as the voltage on this pin is above VTSD. When the voltage on the TSD pin decreases below VTSD before the ballast is reconnected to the mains, the information cell is set to a state that leads to nominal light output of the lamp when the lamp is reconnected to the line voltage next time.

The time tTSD is defined by the voltage of the half-bridge when the oscillation stops, the current consumption (ITSD) of the TSD-pin and the resistor RA. Decreasing the time, tTSD may be achieved by connecting a resistor RB between the TSD pin and GND. (see *Figure 7*).

When the lamp is operated with reduced light output, the thermal powerboost time (see *Section 5.6*) is shortened to 1022 period times of the clock generator in any case.

If the voltage on the TSD pin is kept below 0.5 V until the lamp has ignited, a change between normal operation mode and dimmed operation mode can be achieved by every transition of the voltage on the TSD pin while the lamp is burning: a voltage VTSD < 0.5 V leads to the normal operation, a voltage VTSD > 6.2 V (typ.) leads to the dimmed operation. Steady-state voltages between 0.5 V and 6.2 V (typ.) on the TSD pin have to be avoided.

The current consumption of the TSD pin is controlled by design with an internal bias circuit that has a compensated temperature behavior.

The two-step dimming function can be deactivated by connecting the TSD pin to GND. In this case, the lamp is always operated with nominal light output.

5.5 Rated current generation

A reference current is used to feed the external resistors RPH, RNO and RDO. The voltages formed across these resistors are converted into internal rated voltage for integrator's comparator during each operation phases of the ballast (see *Figure 5*).

In order to compensate both the tolerances and the temperature variations of such a reference current, it is matched with the current used to charge the integrating capacitance C_{int}. As a result, the obtained lamp current has the same tolerance as the external programming resistors even if the relevant rated voltages have noticeable variations.

During the preheating phase, the rated resonant current is defined by the external resistor RPH.

The length of the preheating phase is defined by the duration of 40960 period times of the clock generator (a frequency fCL=100 kHz results in a duration of the preheating phase of 410 ms).

During the ignition phase, the rated resonant current increases from the preheating level to a level that ensures an operation of the half-bridge very close to the pole frequency of the resonant lamp circuit.

This increase is internally reached with a ramp composed by 31 steps given by the D/A-converter block. In the first half of the ramp, height out of the ramp steps are smaller than those in the second half of the ramp. The length of each step is defined by the duration of 512 half waves of the resonant current. The last step of the ramp is reached after 15872 half waves (512 x 31).

The end of the ignition phase is reached only when the ignition recognition unit delivers a trigger signal (*Section 5.11*). In this case, the ignition phase is ended and the rated resonant

current is set to the powerboost level. Otherwise, the ZVS control prevents the half-bridge from operating below resonance. This condition does not lead to a latched turn-off.

During the powerboost phase, the current defined by the voltage across the RNO resistor is internally increased by the fixed ratio XPB. During the first half of the powerboost phase, the rated resonant current remains constant at the defined level, while during the second half, the rated current decreases in 15 equal steps up to the value of the normal lamp operation.

The length of the powerboost phase is roughly defined by the duration of 4063232 period times of the clock generator. There are 2097152 period times for the constant powerboost level. The decrease to the normal operation level takes place in equal steps with a length of 131072 period times of the clock generator per step.

The duration of the powerboost phase is shortened to 1022 period times of the clock generator when the lamp is already warm or when operated with reduced light output.

During normal operation, two possible rated resonant currents can be achieved related to the output signal of the two-step dimming unit. During the operation of the lamp with nominal light output, the nominal rated value is defined by the external resistor RNO. When operating the lamp with reduced light output, the reduced rated value is defined by the external resistor RDO.

The ratio between both possible rated values of the resonant current leading to reduced or nominal light output is defined by the ratio RNO/RDO.

5.6 Thermal powerboost control

A cold lamp emits a lower light level even when driven by a correct rated current. To speed up the lamp heating, a higher current is applied during few seconds of nominal operation (thermal powerboost). The junction-temperature of the device is measured: if it is above TPB the powerboost phase is entered as described in *Section 5.5*, otherwise the lamp is directly operated with nominal light output.

5.7 Output stage

The output stage processes the trigger signals from the current regulation unit, the ignition recognition unit and the UVLO block and controls the high-side and low-side driver. Corresponding with the UVLO function the output stage controls the startup of the device.

5.8 Deadtime generation

The deadtime of the half-bridge is programmed by the external resistor RDT and it is equal for both high-side and low-side driver. It is adjustable between 1 µs and 5 µs. A minimum deadtime that avoids cross conduction of the power transistors is ensured by a minimum resistance of the external resistor RDT.

The deadtime generator delays the switch on both of power transistors, while the switch off signal from the output stage runs immediately to the drivers.

5.9 Undervoltage lockout

After the turn-on of the ballast, the UVLO is activated until the supply voltage exceeds the specified turn-on threshold voltage VSUVP.

While loading the blocking capacitor after power on, the low-side transistor has to be turned on to charge the bootstrap capacitor before the high-side transistor is switched on the first time.

When the supply voltage falls below the VSUVN threshold the device waits for the condition "activated LVG and deactivated HVG". The UVLO is activated with a delay time of 1.3 µs after this condition comes true.

Moreover, a logic UVLO is activated in order to restart the device with the preheating phase when no resonant current is sensed in a period of tdisc.

During the logic UVLO, all logic blocks of the device are reset, but the current references and internal regulators are still on.

5.10 Voltage reference

The voltage reference delivers a reference signal with a very small tolerance (band gap).

5.11 Ignition recognition

This unit is activated at the beginning of the ignition phase (see *Figure 6*). It provides a synchronization pulse to the clock generator every time either the current control units are triggered by the signal processing unit or ZVS control turns on the relevant transistor. Being the half of the clock frequency programmed to be lower than resonance frequency, the clock period during the ignition phase is forced to be shorter than the programmed one.

Once the lamp ignites the integral of the operating current, it takes longer time to reach the rated value and the clock period reaches the programmed value.

In this case, the ignition phase is terminated, the ignition recognition unit is deactivated and the rated resonant current is set on the powerboost level.

On the contrary, the end of ignition is not detected and both the half-bridge and the clock remain locked to resonance frequency by ZVS control unit.

5.12 Clock generator

This high frequency oscillator provides with time bases for the IC during the various operating phases.

During the preheating phase it delivers a fixed time base for the counter. At the beginning of the ignition phase when the ignition recognition unit is active, the oscillator is synchronized with the output stage. Therefore the timing element of the oscillator is reset with the frequency of the output stage. If one half cycle, of period time of the output stage given by the current regulator exceeds the fixed period time of the clock generator, a trigger signal is formed and given to the output stage and the counter. This leads to a defined termination of the ignition phase. After setting the rated resonant current to the powerboost level, the clock generator continues in a self-oscillating way until it is stopped by the counter at the end of the powerboost phase.

The frequency of the clock generator is fixed with the external resistor RCL, increasing the resistance of RCL and reducing fCL.

5.13 Counter

The counter is formed as binary counter. A digital network generates signals that activate the ignition recognition unit and control the D/A converter and the rated current generation unit. The counter is reset by the UVLO unit.

5.14 D/A converter

The D/A converter forms the ramps for the rated resonant current during the ignition phase and the powerboost phase.

Figure 5. Operating phases

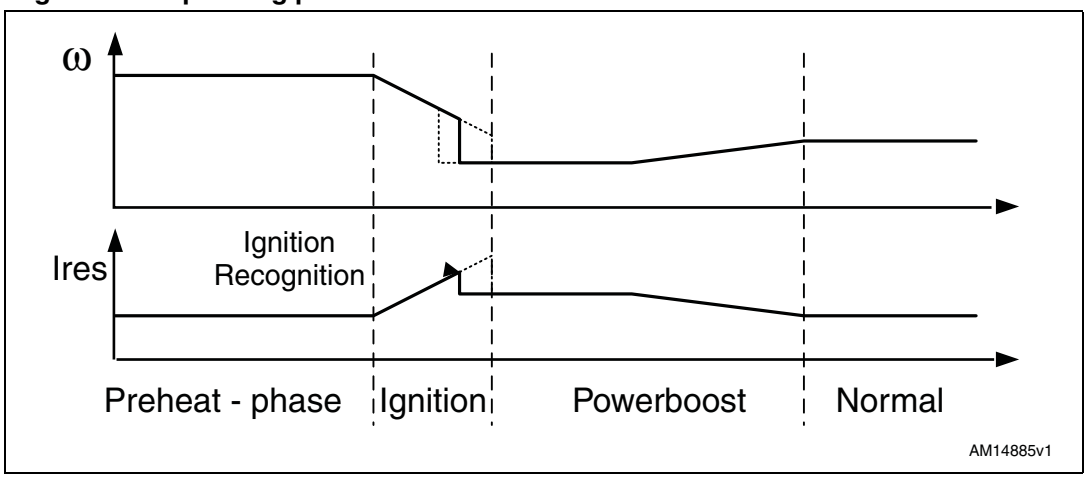


Figure 6. Ignition recognition

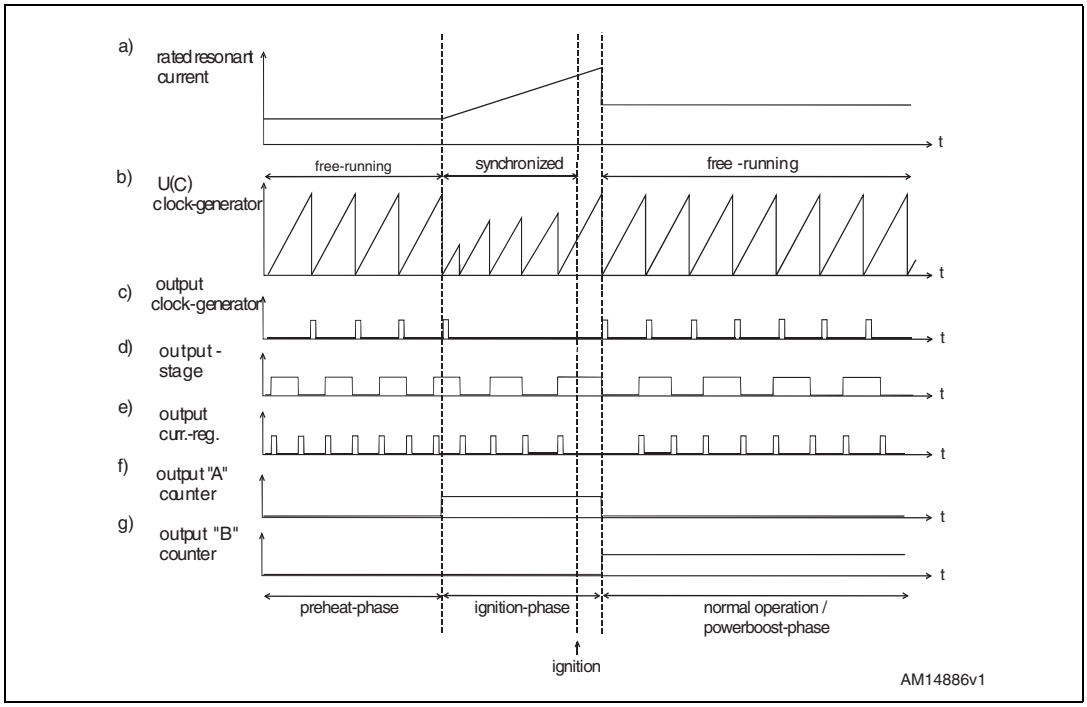
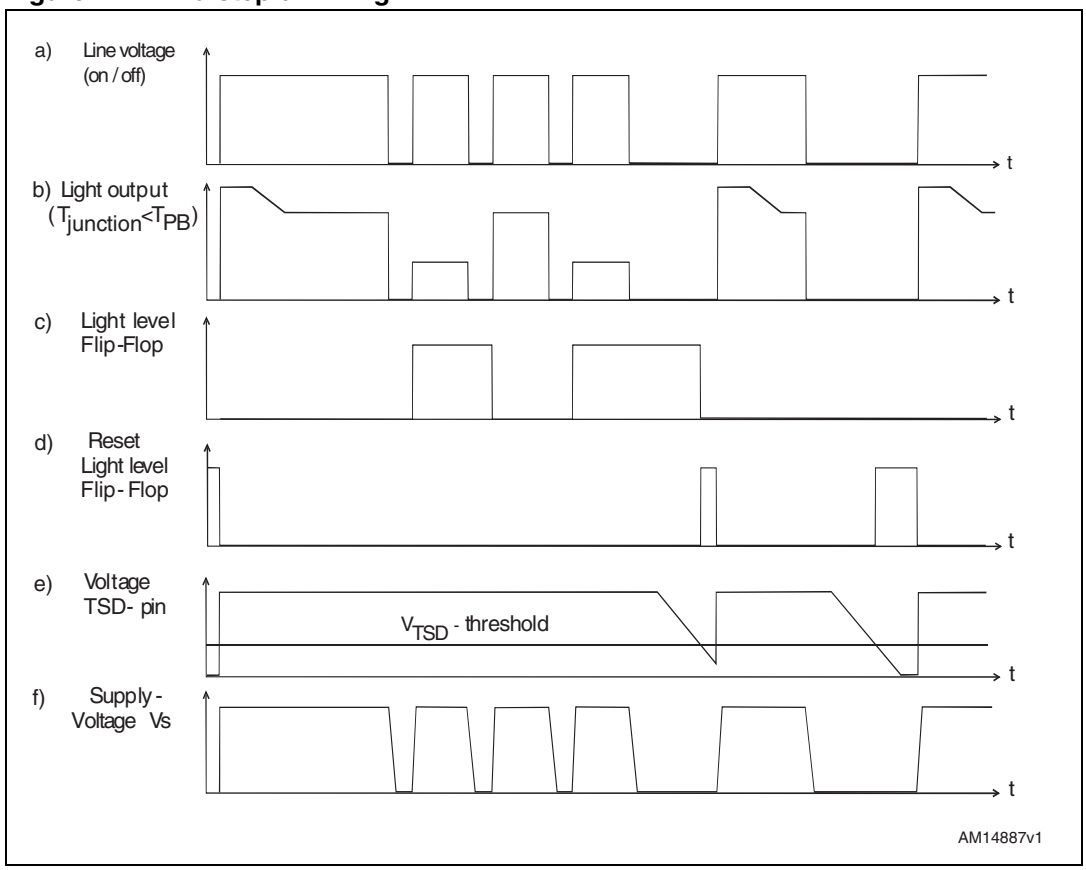


Figure 7. Two-step dimming



6 Application information

6.1 Target applications

The L6572 is primarily intended to accurately drive, with a minimum number of external components, integrated compact fluorescent lamps. Its particular current control method allows a noticeable extension of lamp lifetime and a higher light quality compared to that obtainable by self oscillating ballasts. Also, the operation of the application during normal operation is very similar to the above mentioned ballasts, but with an improved repeatability of the lamp parameters (see *Figure 2*).

The same advantages can be exploited by separately controlled fluorescent lamp applications, especially CFLs up to 26 W.

Using further external components, higher power ratings are also reachable.

Furthermore, dimming functionality, in particular two-step dimming, helps to implement variable light sources.

6.2 Designing a simple fixed power CFLi application using the L6572

The first step to follow is to define the clock frequency: it can be calculated in order to fit the preheating time requirements. The following equations give the relationships between the typical value of clock period, the preheating time and RCL value.

- $RCL_{k\Omega} \cong 0.10327 \cdot T_{PH|_{ms}}$
- $TCL_{\mu s} \cong 0.2364 \cdot RCL_{k\Omega}$
- $FCL_{KHZ} \cong \frac{1000}{TCL_{\mu s}}$

Given the clock frequency, the value of the resonance frequency of the LC cell must be selected higher than the half of the clock frequency in all possible conditions. Otherwise the ignition recognition circuitry may operate incorrectly.

- $F_{Res} \cong \frac{1}{2\pi \cdot \sqrt{L \cdot C}}$

The range of frequencies related to nominal operation and to the preheating phase can be now selected respectively below and above F_{Res}. Considering the operating frequency ranges and the lamp parameters, the value for resonant components can now be selected: different calculation approaches can be adopted.The value of the sense resistor has to be chosen in order to guarantee a sufficient signal level for the ZCD function: at minimum the peak of the resonant current in every condition must be above VZVS. As the reference current of programming resistors is matched the integrator reference current, a relation between the programming resistor value and the obtained voltage*time area (VTA) can be expressed. These relations can be used to evaluate a first tentative value for the programming resistors RPH, RNO and RDO. A subsequent iterative verification on the real project is usually required: in fact, the value of the integral is highly dependent on the real shape of the sense voltage. Deadtime duration somewhat affects the result of the integration as well.

In ideal conditions the resonant current is almost sinusoidal, having a phase term (ϴ) in respect to the voltage applied by the half-bridge. Generally, it can be written that:

Equation 2

$$I_{res}(t) = I_{res,\ rms}\sqrt{2} \cdot \sin(2\pi \cdot f_{sw} \cdot t - \theta)$$

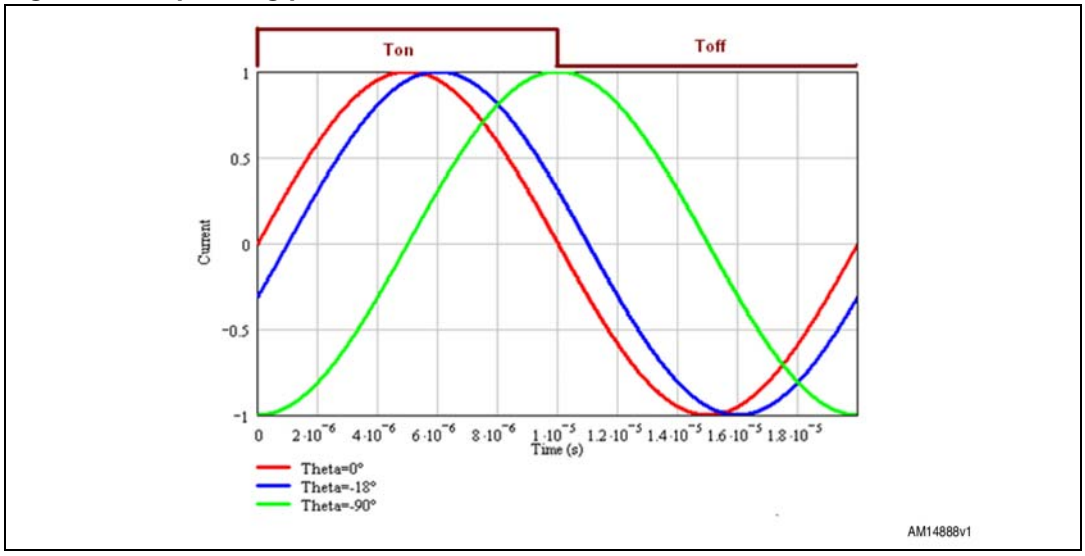
The term "ϴ" is here expressed in radiant, but it can be expressed in terms of time. Moreover, it is always positive as long as the operating point is above the resonance.

Equation 3

$$I_{res}(t) = I_{res,\ rms}\sqrt{2} \cdot \sin(2\pi \cdot f_{sw} \cdot t - 2\pi \cdot f_{sw} - \theta)$$

The following figure illustrates the case of operation at resonance (red line), with a small phase, usually seen during normal operation (blue line) and finally during preheating (green line) where a 90° phase is experienced.

Figure 8. Operating phases



The voltage at SENSE pin has the same shape as the resonant current and is rectified and then integrated by the current signal processor of the L6572. It can be easily demonstrated that the integral of the rectified waveform does not depend on the initial phase (ϴ) but only on the waveform amplitude and frequency.

Equation 4

$$A = \int_{T1/2on} |V_{SENSE}| dt \cong \frac{\sqrt{2} \cdot I_{res,\ rms} \cdot R_{SENSE}}{2\pi \cdot f_{SW}}$$

As previously discussed, the non linear behavior of the glow discharge characteristics makes this result quite approximate because the resonant current is not exactly sinusoidal. Nevertheless it is more accurate during the preheating.

Therefore, suggested starting values for the application dimension are around:

Equation 5

$$R_{ph(k\Omega)} \cong A_{ph(\mu V \times s)} \cdot 20$$
$$R_{no(k\Omega)} \cong A_{no(\mu V \times s)} \cdot 20$$

The second relation is also valid for dimmed operations.

A small capacitor placed in parallel with Rph (around 10 pF), helps to improve the preheating phase.

Deadtime can also be fixed during this step.

A useful relationship to find the right value of Rdt, expressed in kΩ, given the value of the selected deadtime, expressed in µs is:

Equation 6

$$R_{dt} = 10.8 \cdot T_{dt}$$

Being a non dimmable application, the RDO pin and TSD pin have to be connected to ground. To be noted that CFLi applications up to 25 W are equipped by MOSFETs having small gate charges: therefore no gate resistance is required and the gate pin of the MOSFETs can be directly connected to driver output.

6.3 Two-step dimmable CFLi application

Once a fixed power application is designed, the dimmability feature can be added by activating TSD pin and RDO.

The first pin is intended to sense the interval between AC turn-off and on, usually using only Ra. As soon as the AC line is turned off, resonant current decreases and consequently the half-bridge stops switching due to Tdis function. Once this occurs the supply voltage drops below turn-off threshold.

The present voltage across the half-bridge is decreasing, but it is greater than zero keeping the TSD structure well supplied thanks to Ra. The smaller the Ra, the longer the time the TSD voltage remains above the dimming enable threshold and the slower the required turn-off turn-on action to enable dimming.

If, during the turn-off interval TSD drops below the threshold, the internal memory cell is reset, otherwise it remains in its previous state.

At subsequent turn-on, after preheating, this state is checked to determine which power level is required.

The dimmed area is selected by Rdo: its value is expected to be lower or equal to Rno. Frequently, the starting voltage across the half-bridge has a wide voltage ripple, and its nominal value is variable as well. For these reasons, a precise design guidance of the selection of Ra cannot be provided. The quickest way to proceed is represented by direct measurements on the real application. Selection of Rdo can be done using the same approach used to determine Rno.

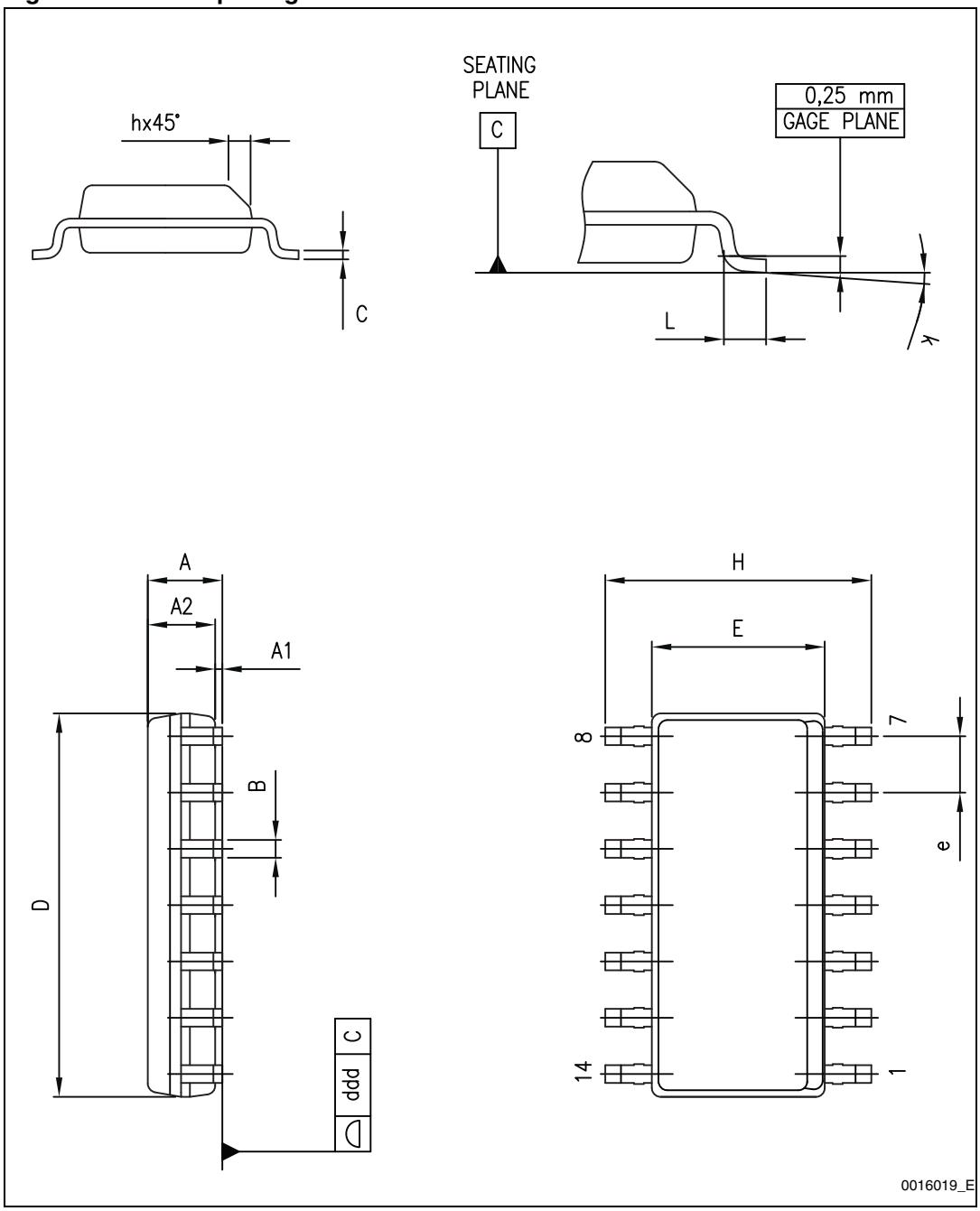
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 6. SO-14 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
K	0		8
e		0.40	
ddd			0.10

Figure 9. SO-14 package dimensions



8 Revision history

Table 7. Document revision history

Date	Revision	Changes
31-Oct-2012	1	Initial release.