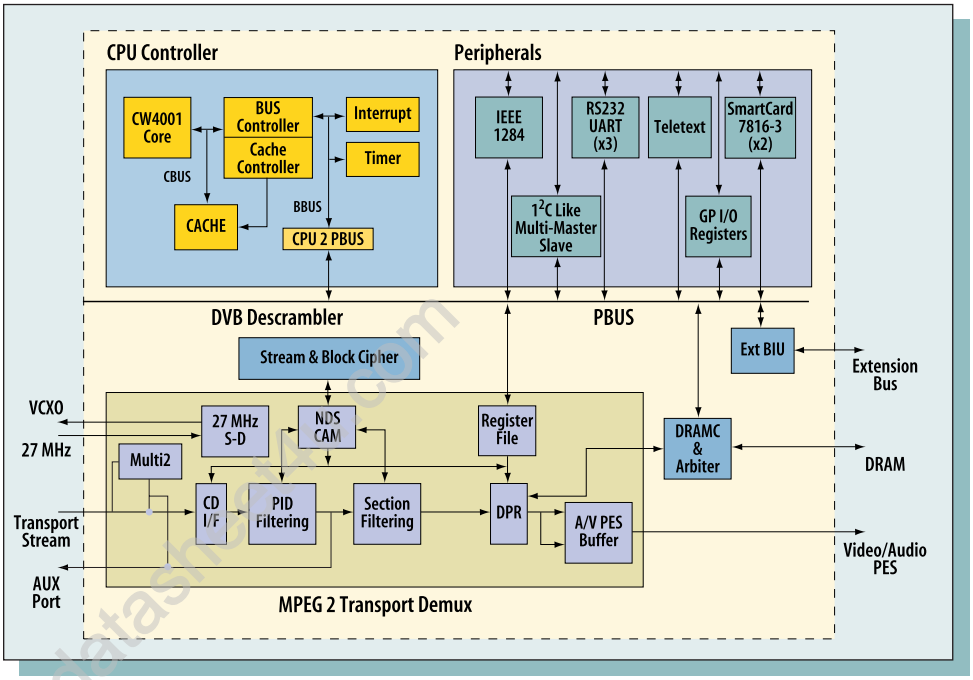
L64108 Transport with Embedded CPU and Control

Overview

The L64108 combines a 32-bit 54 MHz RISC CPU, a programmable transport demultiplexer, a DVB Descrambler, a DRAM controller and other peripherals on a single chip. This versatile device interfaces to all of the other members of the Integra™ 1100 set-top product family. This includes a serial or parallel input from the L64724 satellite modem or the L64768 cable modem and an output of multiplexed audio and video PES streams to the L64105 MPEG-2 A/V Decoder. The L64108 is suitable for worldwide use in DBS, CATV, or telco set-top boxes.

Intelligence, Flexibility, Performance

The on-chip high performance CW4001 MiniRISC® 32-bit RISC MIPS CPU subsystem provides the set-top with intelligence, flexibility and performance. The CPU subsystem includes 8 KB of instruction cache and 4 KB of data cache to substantially enhance performance as well as timers and counters that are needed by real-time operating systems. The powerful 54 MHz CPU is capable of processing all of the set-top application and control needs. These include complete set-top system initialization and testing, security handling, communication ports protocol processing, remote control handling, PCR recovery and locking, audio/video synchronization, subtitles, OSD overlay, closed caption, teletext, and electronic program guide (EPG).



L64108 Block Diagram

Features and Benefits

- ISO/IEC 13818-1 (MPEG-2) compliant transport demultiplexer
  - 32 PIDs support
  - Sustained input rate up to 60 Mbits/sec serial and 9 Mbytes/sec parallel
  - Extensive and fully programmable hardware section filtering scheme
  - Robust error handling and recovery
  - Support of a Program Clock Reference (PCR) PID
  - Automatic detecting and switching of audio and video PIDs on splice points
- Integrated high performance 54 MHz CW4001 MiniRISC MIPS CPU
  - Host CPU for set-top box; powerful enough to also handle transport, graphics, ATM SAR layer processing and other functions
  - 4 KB Data (Direct Mapped); 8 KB Instruction (2-way set associative) Cache
  - Timers, interrupt controller
  - BBCC- Basic Bus and Cache Controller Unit
  - Interfaces to external Set-top components through Motorola 68K style extension bus
  - MIPS-II instruction set compatible
- On-chip DVB, NDS, and Multi2-compliant descramblers
  - Support for transport-level and PES-level descrambling
  - Seamless support of scrambled and unscrambled data
  - Support of up to 12 pairs of 64-bit keys

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Intelligence, Flexibility, Performance (continued)

In addition, the CPU will support transport-related software processing including handling operations such as PSI and DVB SI tables maintenance and private section filtering.

Compatibility and Security

The Transport Demultiplexer with 32 PID (Packet ID) is MPEG-2, DVB- and JSAT-compliant and features a very extensive hardware-assisted PSI section filtering scheme. This functionality is not only a superset of the standard MPEG-2 section filtering scheme but also covers worldwide service providers' specific filtering requirements. The integration of the DVB descrambler block into the chip substantially increases the security of the set-top box since the interface to the descrambler is no longer observable at the board level. In addition to the common DVB descrambler, L64108 has integrated NDS (News Data Service) and Multi2 (required for Japanese Market) Conditional Access Module.

The L64108 integrates several on-chip peripherals including three RS232 serial communication ports, two SmartCard ports, an IEEE1284 parallel communication port, I²C-like serial communication port, a teletext port and general purpose I/Os.

Features and Benefits (Continued)

- DRAM controller with support for up to 16 Mbits EDO/FPM DRAM
- On-chip Peripherals
  - Three 8251-compatible serial ports (RS232)
  - IEEE 1284 parallel port
  - Two ISO7816 SmartCard interfaces
  - I²C-compatible interface port supporting multimaster or slave modes
  - Teletext serial interface to NTSC/PAL encoder
  - Auxiliary (AUX) fast output port that can output transport packets after PID filtering or after descrambling
  - 50 General Purpose I/Os
- Support of direct interface to LSI single-chip channel decoder devices, such as the L64724 for DBS and the L64768 for CATV
- A/V serial or parallel output for a direct interface to the L64005 or L64105 MPEG-2 A/V decoder devices
- Supported by industry-standard RTOS and software vendors like Nucleus+, Integrated Systems (pSOS), OpenTV and WindRiver Systems (VxWorks)
- Supported by Integra™ SDP1100 set-top box hardware and software development platform
- JTAG Support
- Uses low-power 0.35 micron, 3.3 V process
- Packaged in 240-pin Plastic Quad Flat Package

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