LinkSmart Technology Co., Ltd.
聯新科技股份有限公司

LST 无锡致合微电子科技有限公司
Link Smart Microelectronics Technology Co.,Ltd.

L24W02

Serial EEPROM

Data Sheet

Revision A

Revision history

Rev. No.	Approved date	History	Remark (purpose)
A	2004/8/20	Initial issue	Preliminary

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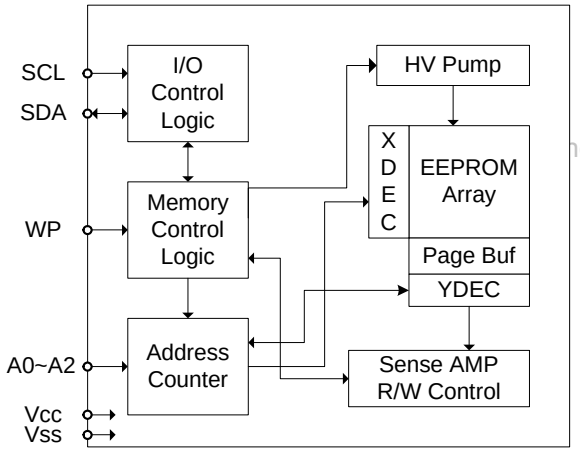
Features

- Operating voltage: 3V~5.5V
- Low power consumption
  - Operation: 5mA max.
  - Standby: 5µA max.
- Internal organization:
  - 2K: 256x8
- 2-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 8-byte Page Write Mode
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 1,000,000 (10^6)rewrite cycles per word
- Commercial temperature range (0°C to +70°C)
- 8-pin SOP/DIP/TSSOP package

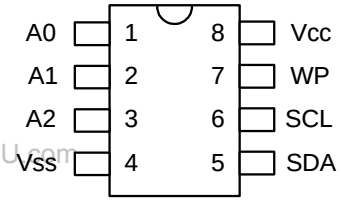
General Description

The L24W02 is a 2K-bits serial read/write non-volatile memory device using the CMOS floating gate process. Its 2,048 bits of memory are organized into 256 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to eight L24W02 devices may be connected to the same two-wire bus. The L24W02 is guaranteed for 1,000,000 (10^6) erase/write cycles and 40 years data retention.

Block Diagram



Pin Configurations



L24W02
8PIN SOP/DIP/TSSOP

Pin Description

Pin Name	I/O	Description
A0~A2	I	Address inputs
SDA	I/O	Serial data inputs/output
SCL	I	Serial clock data input
WP	I	Write protect
Vss	—	Negative power supply
Vcc	I	Positive power supply

Absolute Maximum Ratings

Operating Temperature (Commercial) ..... 0°C to 70°C
Storage Temperature ..... –50°C to 125°C
Applied V_{CC} Voltage with Respect to V_{SS} ..... –0.3V to 6.0V
Applied Voltage on any Pin with Respect to V_{SS} ..... –0.3V to V_{CC}+0.3V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics Ta=0°C to 70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		Vcc	Conditions				
V_{CC}	Operating Voltage	—	—	3	—	5.5	V
I_{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I_{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	—	–1	—	0.3Vcc	V
V_{IH}	Input High Voltage	—	—	0.7V_{CC}	—	Vcc+0.5	V
V_{OL}	Output Low Voltage	3V	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 or V_{CC}	—	—	1	µA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 or V_{CC}	—	—	1	µA
I_{STB1}	Standby Current	5V	V_{IN}=0 or V_{CC}	—	—	5	µA
I_{STB2}	Standby Current	3V	V_{IN}=0 or V_{CC}	—	—	4	µA
C_{IN}	Input Capacitance (See Note)	—	f=1MHz 25°C	—	—	6	pF
C_{OUT}	Output Capacitance (See Note)	—	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested

A.C. Characteristics Ta=0°C to 70°C

Symbol	Parameter	Remark	Standard Mode*		Vcc=5V±10%		Unit
			Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	—	—	100	—	400	kHz
t_{HIGH}	Clock High Time	—	4000	—	600	—	ns
t_{LOW}	Clock Low Time	—	4700	—	1200	—	ns
t_R	SDA and SCL Rise Time	Note	—	1000	—	300	ns
t_F	SDA and SCL Fall Time	Note	—	300	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	4000	—	600	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	4000	—	600	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	200	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	4000	—	600	—	ns
t_{AA}	Output Valid from Clock	—	—	3500	—	900	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4700	—	1200	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	—	5	ms

Notes: These parameters are periodically sampled but not 100% tested
* The standard mode means V_{CC}=3V to 5.5V
For relative timing, refer to timing diagrams

Functional Description

- Serial clock (SCL)

The SCL input is used for positive edge clock data into each EEPROM device and negative edge clock data out of each device.

- Serial data (SDA)

The SDA pin is bidirectional for serial data transfer. The pin is open-drain driven and may be wired-OR with any number of other open- drain or open collector devices.

- A0, A1, A2

The A2,A1 and A0 pins are device address inputs that are hard wired for the L24W02.As many as eight 2K devices may be addressed on a single bus system (The device addressing is discussed in detail under the Device Ad- dressing section).

- Write protect (WP)

The L24W02 has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to the Vss. When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Protect Array
At Vcc	Full Array (2K)
At Vss	Normal Read/Write Operations

Memory organization

- L24W02, 2K Serial EEPROM

Internally organized with 256 8-bit words, the 2K requires an 8-bit data word address for random word addressing.

Device operations

- Clock and data transition

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in data line while the clock line is high will be interpreted as a START or STOP condition.

- Start condition

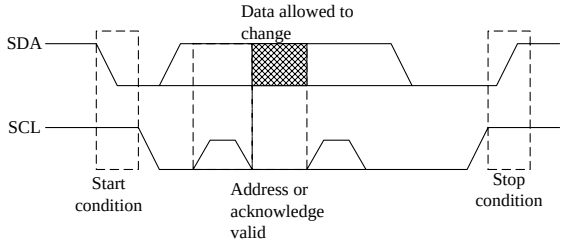
A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

- Stop condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

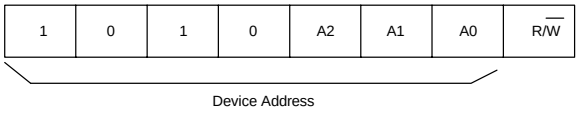
- Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.



The 2K EEPROM devices require an 8-bit device address word following a start condition to enable the

chip for a read or write operation. The device address word consists of a mandatory one, zero sequence for the first four most significant bits (refer to diagram showing the Device Address). This is common to all EEPROM devices.
The next three bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These three bits must compare to their corresponding hard-wired input pins.
The 8th bit of device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.
If the comparison of the device address succeeds the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



Write operations

- Byte write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a micro- controller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the non-volatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until the write is completed (refer to Byte write timing).

- Page write

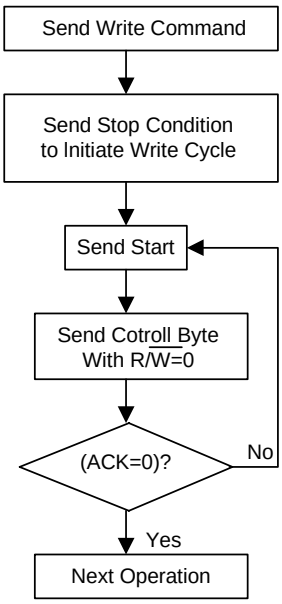
The 2K EEPROM is capable of 8-byte page writes.

A page write is initiated the same as byte write, but the micro controller does not sand a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the micro controller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The micro controller must terminate the page write sequence with a stop condition.

The data word address lower three (2K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location (refer to Page write timing).

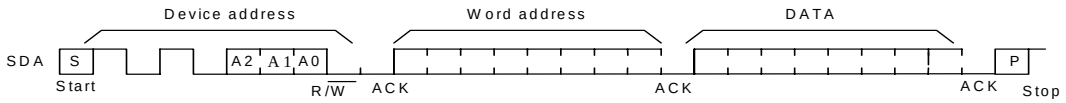
- Acknowledge polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is completed, then the device will return the ACK and the master can then proceed with the next read or write command.

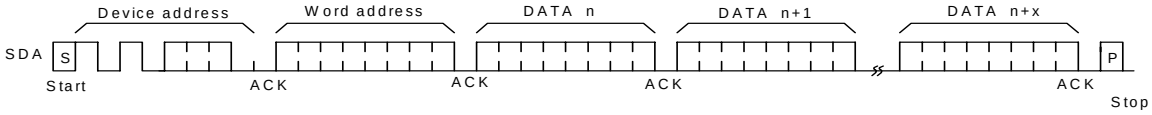


Acknowledge polling flow

Byte write timing



Page write timing



- Write protect

The L24W02 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be writing protected.

- Read operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

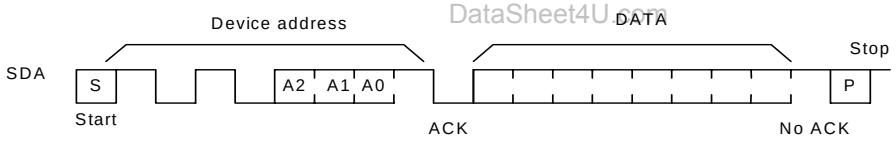
- Current address read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The addresses roll over during read from the last byte of the last memory page to the first byte of the first page. The addresses roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The micro controller does not respond with an input zero but generates a following stop condition (refer to Current read timing).

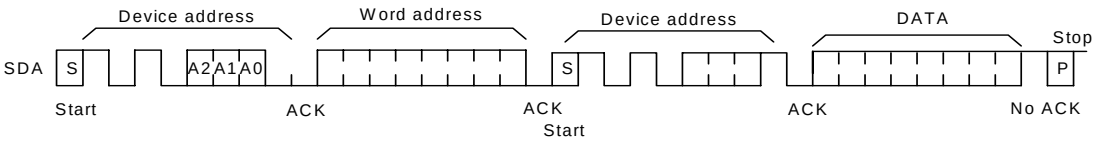
- Random read

A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The micro controller must then generate another start condition. The micro controller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The micro controller does not respond with a zero but does generate a following stop condition (refer to Random read timing).

Current read timing



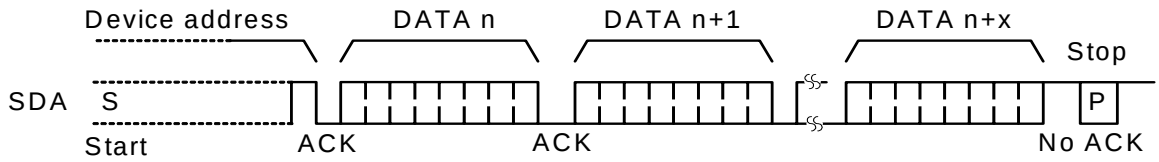
Random read timing



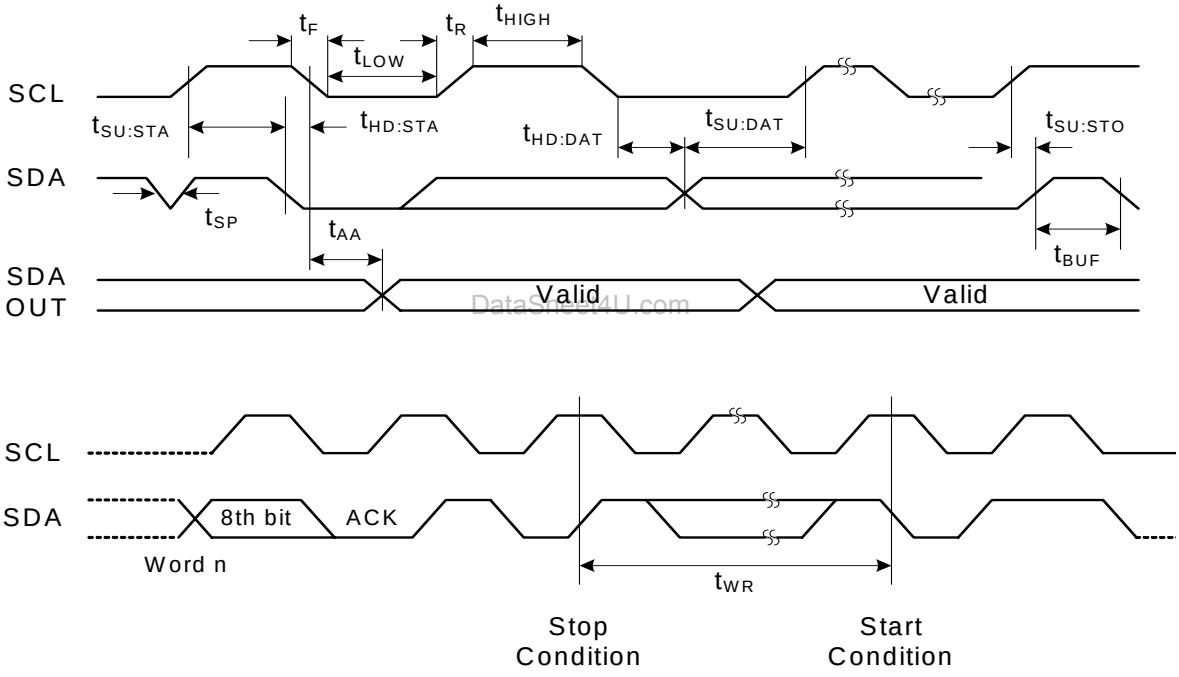
- Sequential read

Sequential reads are initiated by either a current address read or a random address read. After the micro controller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the micro controller does not respond with a zero but generates a following stop condition.

Sequential read timing

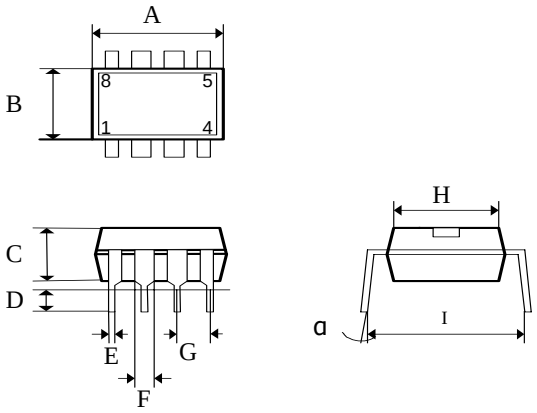


Timing Diagrams



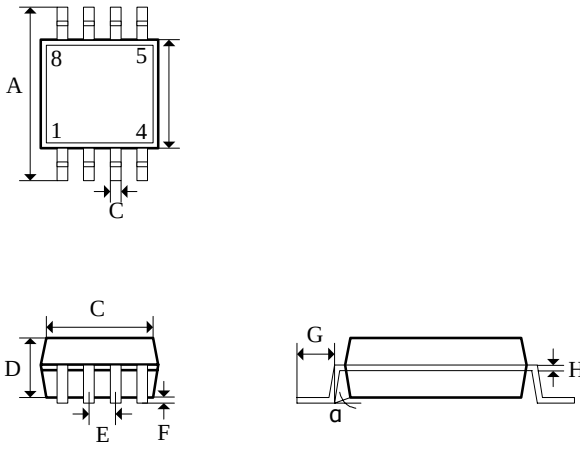
Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

Package Information
8-pin DIP (300mil) Outline Dimensions



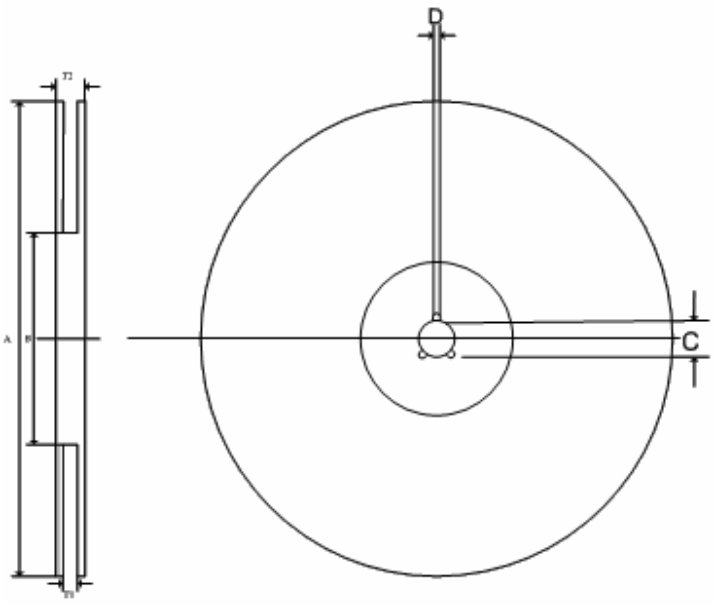
Symbol	Dimensions in mil		
	Min.	Nom	Max
A	355	-	375
B	240	-	260
C	125	-	135
D	125	-	145
E	16	-	20
F	50	-	70
G	-	100	-
H	295	-	315
I	335	-	375
α	0°	-	15°

8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom	Max
A	228	-	244
B	149	-	157
C	14	-	20
C ′	189	-	197
D	53	-	69
E	-	50	-
F	4	-	10
G	22	-	28
H	4	-	12
α	0°	-	10°

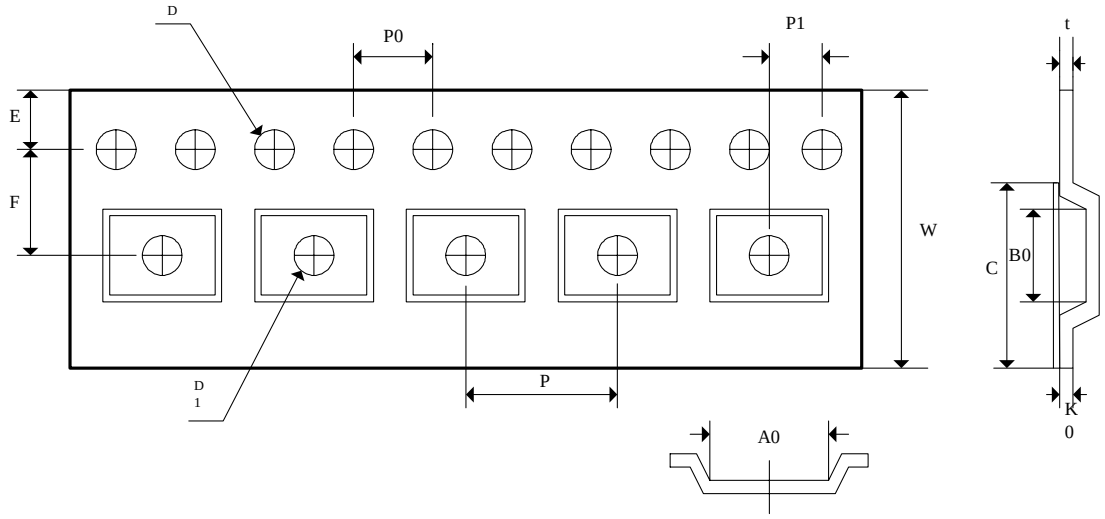
Product Tape and Reel Specifications
Reel Dimensions



SOP 8PIN

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 -0.2
D	Key Slit Width	2.0±0.15
T1	Space Between Flange	12.8+0.3 -0.2
T2	Reel Thickness	12.8±0.2

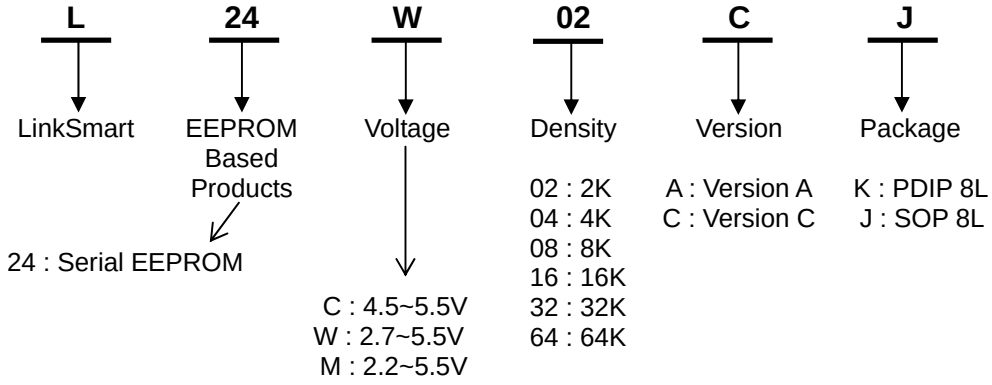
Carrier Tape Dimensions



SOP 8PIN

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

Part Number Information



Application

Serial EEPROM are ideal non-volatile cost effective memory solutions in applications that require:

- Low voltage and current for handheld battery applications as in a keyless entry transmitter
- Small footprint and board space as in cellular phone applications
- BYTE level ERASE, WRITE, and READ of data as in a TV tuner
- Multiple non-volatile functions in the same application such as a VCR
- Low availability of microcontroller I/O lines

The typical functions that serial EEPROM are utilized for are:

- Memory storage of channel selectors or analog controls (volume, tone, etc.) in consumer electronics products e.g. DVD, VCD, CD…
- Electronic real time event or maintenance logs such as page counting in office automation products. Also, configuration or DIP switch storage in office automation products
- Power down storage and retrieval of events such as fault detection or error diagnostics in automotive products
- Last number redial storage and speed dial number storage in telecom products
- User in-circuit reprogrammable looks up tables such as bar code readers, point-of-sale terminals, environmental controls and other industrial products.

Other application examples include:

- Data storage from a learn function as in a remote control transmitter
- Reprogrammable calibration data for test equipment or analog interface products
- ID number storage for security or remote access for electronic keys and entry databases

Serial EEPROM Selection Guide

P/N	Density (Int. Organization)	Page Write Mode	Write Cycle Time (max)	Endurance	Operating Voltage	Package
L24C02	2K-bits (256x8)	8-bytes	5ms	10^6	4.5V~5.5V	SOP/DIP/TSSOP
L24W02	2K-bits (256x8)	8-bytes	5ms	10^6	3V~5.5V	SOP/DIP/TSSOP
L24M04	4K-bits (512x8)	16-bytes	5ms	10^6	2.2V~5.5V	SOP/DIP/TSSOP
L24W04	4K-bits (512x8)	16-bytes	5ms	10^6	3V~5.5V	SOP/DIP/TSSOP
L24M08	8K-bits (1,024x8)	16-bytes	5ms	10^6	2.2V~5.5V	SOP/DIP/TSSOP
L24W08	8K-bits (1,024x8)	16-bytes	5ms	10^6	3V~5.5V	SOP/DIP/TSSOP
L24W16	16K-bits (2,048x8)	32-bytes	10ms	10^5	2.7V~5.5V	SOP/DIP/TSSOP
L24W32	32K-bits (4,096x8)	32-bytes	10ms	10^5	2.7V~5.5V	SOP/DIP/TSSOP
L24W64	64K-bits (8,192x6)	32-bytes	10ms	10^5	2.7V~5.5V	SOP/DIP/TSSOP