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Product Functional Specification

13.3 inch XGA Color TFT/LCD Module
Model Name:L133X3-1

(◆) Preliminary Specification
( ) Final Specification

Note: This Specification is subject to change without notice.

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ii Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 '00/10/05	All	First Edition for Customer	All	
0.2 '00/11/07	6		Wet bulb temperature chart	Add
0.3 '00/11/22	4	Weight 450 Max.	Weight 460 Typ.	
	19, 20		Update mechanical drawing	

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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2.0 General Description

This specification applies to the 13.3 inch Color TFT/LCD Module L133X3.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	338(13.3")
Active Area	[mm]	270.336(H) x 202.752(V)
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.264(per one triad) x 0.264
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance	[cd/m^2]	150
Contrast Ratio		200 : 1 Typ.
Optical Rise Time/Fall Time	[msec]	30 Typ., 50 Max.
Nominal Input Voltage VDD	[Volt]	+3.3 V
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.0(w/o Inverter, All black pattern)
Weight	[Grams]	450 Typ.
Physical Size	[mm]	284(W) x 214.5(H) x 5.5(D)
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60

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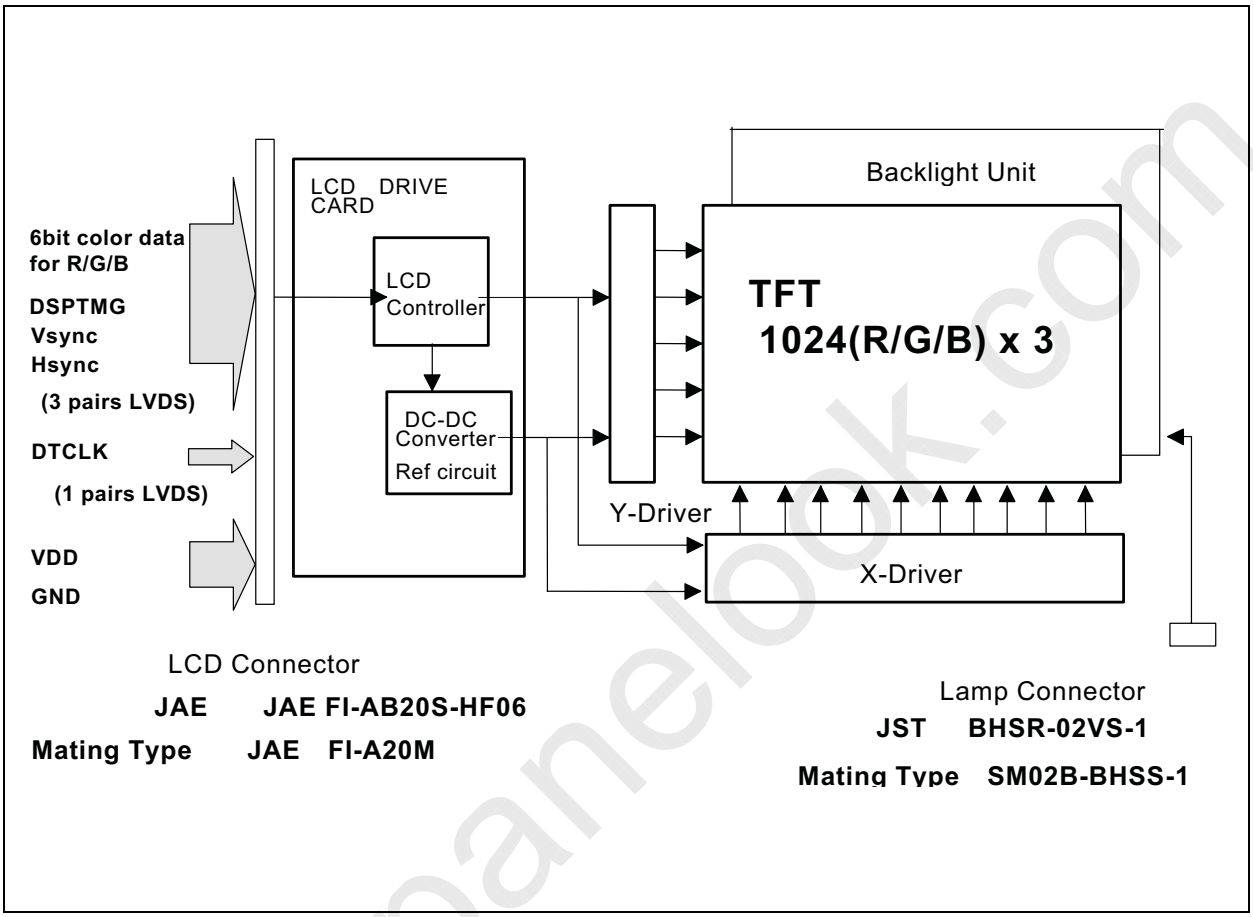
2.2 Functional Block Diagram



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3.0 Absolute Maximum Ratings

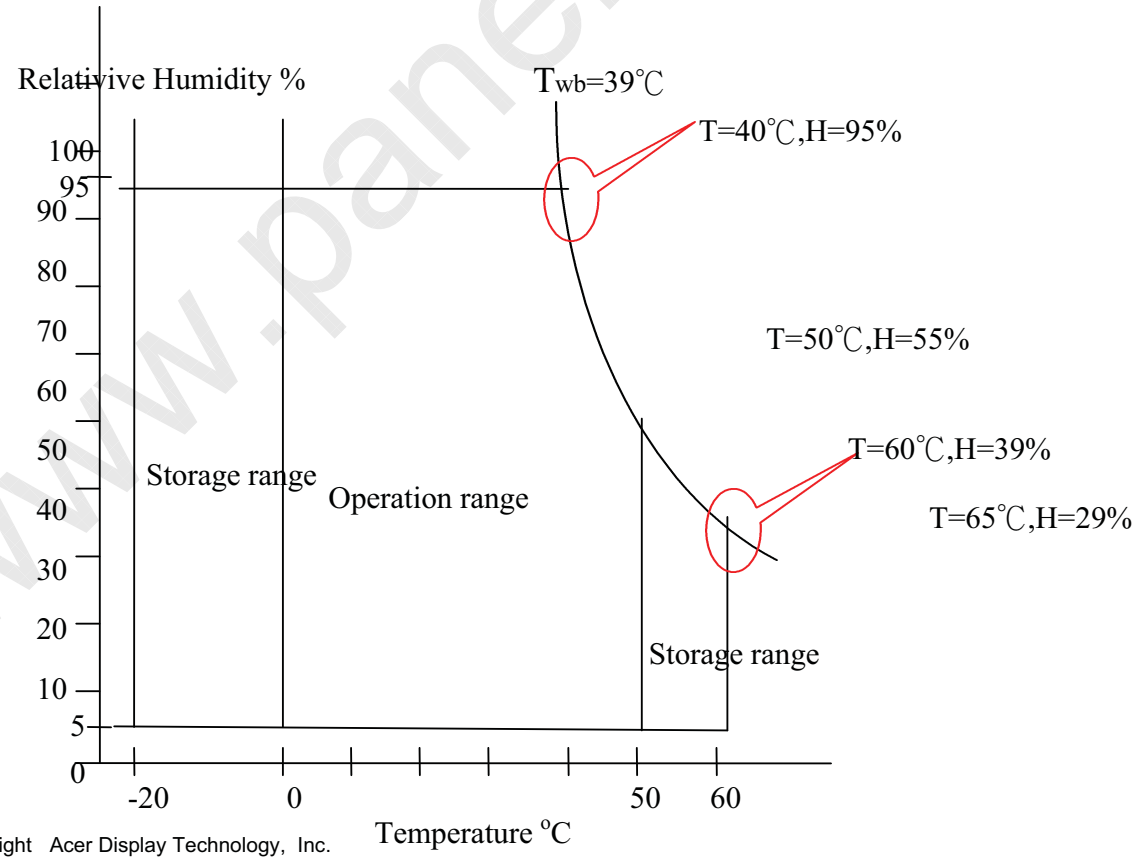
Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	Vss-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin			[Volt]	
CCFL Inrush current	ICFLL	-	20	[mA]	Note 2
CCFL Current	ICFL	-	7.5	[mA] rms	
Operating Temperature	TOP	0	+50	[°C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Humidity	HST	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[°C]	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18 180 3	G ms G ms	Rectangle wave Half sine wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

Note 2 : Duration=50 msec.

Wet bulb temperature chart



4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item		Conditions	Min.	Typ.	Max.
Viewing Angle	[degree]	Horizontal (Right)	40		
	[degree]	K = 10 (Left)	40		
K: Contrast Ratio	[degree]	Vertical (Upper)	10	20	
	[degree]	K = 10 (Lower)	30	35	
Contrast ratio				200	
Response Time	[msec]	Rising		20	30
	[msec]	Falling		30	50
Color / Chromaticity Coordinates (CIE)		Red x	0.537	0.577	0.617
		Red y	0.308	0.338	0.368
		Green x	0.280	0.310	0.340
		Green y	0.533	0.563	0.593
		Blue x	0.128	0.158	0.188
		Blue y	0.117	0.157	0.197
		White x	0.283	0.313	0.343
		White y	0.299	0.329	0.359
White Luminance CCFL 6mA	[cd/m^2]		120	150	

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5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-AB20S-HF06
Mating Housing/Part Number	FI-A20H

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	VDD	2	VDD
3	GND	4	GND
5	Rxin0-	6	Rxin0+
7	GND	8	Rxin1-
9	Rxin1+	10	GND
11	Rxin2-	12	Rxin2+
13	GND	14	Rxclk-
15	Rxclk+	16	GND
17	NC	18	Reserved
19	GND	20	GND

5.3 Signal Description

The module using a LVDS receiver SN75LVDS86DGG(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84DGG(negative edge sampling) or compatible.

Pin#	Signal Name	Description
1	VDD	+3.3V Power Supply
2	VDD	+3.3V Power Supply
3	GND	Ground
4	GND	Ground
5	Rxin0-	Negative LVDS differential data input (R0-R5, G0)
6	Rxin0+	Positive LVDS differential data input (R0-R5, G0)
7	GND	Ground
8	Rxin1-	Negative LVDS differential data input (G1-G5, B0-B1)
9	Rxin1+	Positive LVDS differential data input (G1-G5, B0-B1)
10	GND	Ground
11	Rxin2-	Negative LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG)
12	Rxin2+	Positive LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG)
13	GND	Ground
14	Rxclk-	Negative LVDS differential clock input
15	Rxclk+	Positive LVDS differential clock input
16	GND	Ground
17	NC	Reserved for future use
18	Reserved	Reserved for LVDS MFG test
19	GND	Ground
20	GND	Ground

Internal circuit of LVDS inputs are as following.

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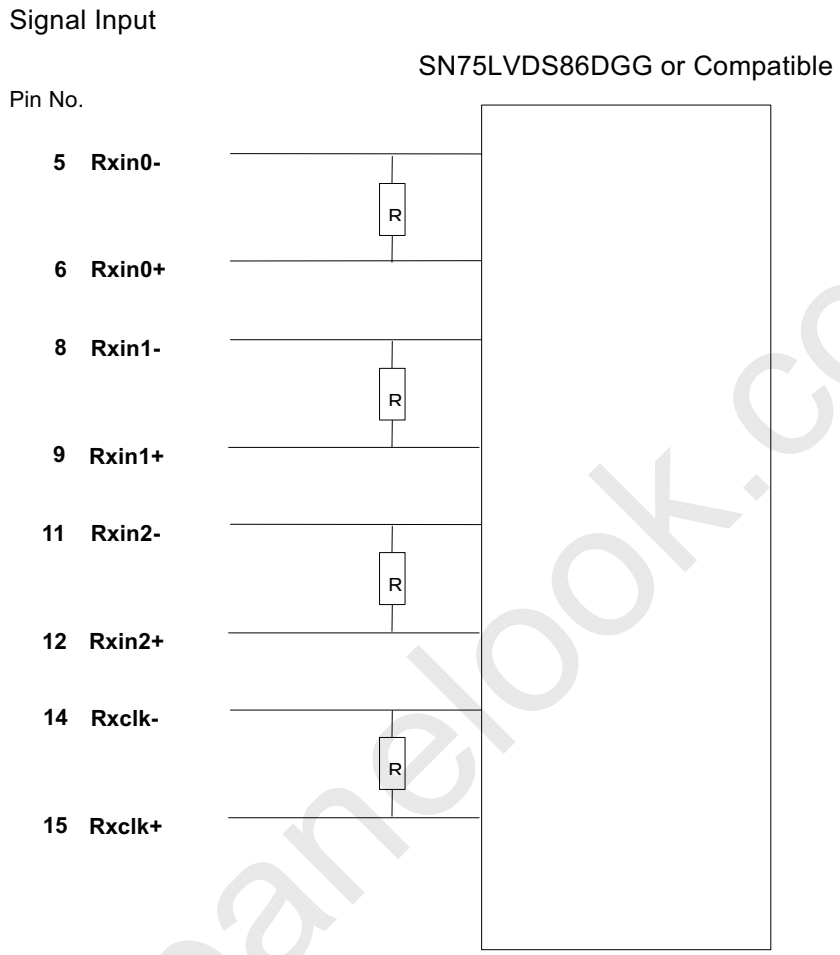

The module uses a 100 ohm resistor between positive and negative data lines of each receiver input.

Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4	Green Data 5 (MSB) Green Data 4	

+GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Each signal characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

Note: It is recommended to refer the specifications to SN75LVDS86DGG (Texas Instruments) in detail.

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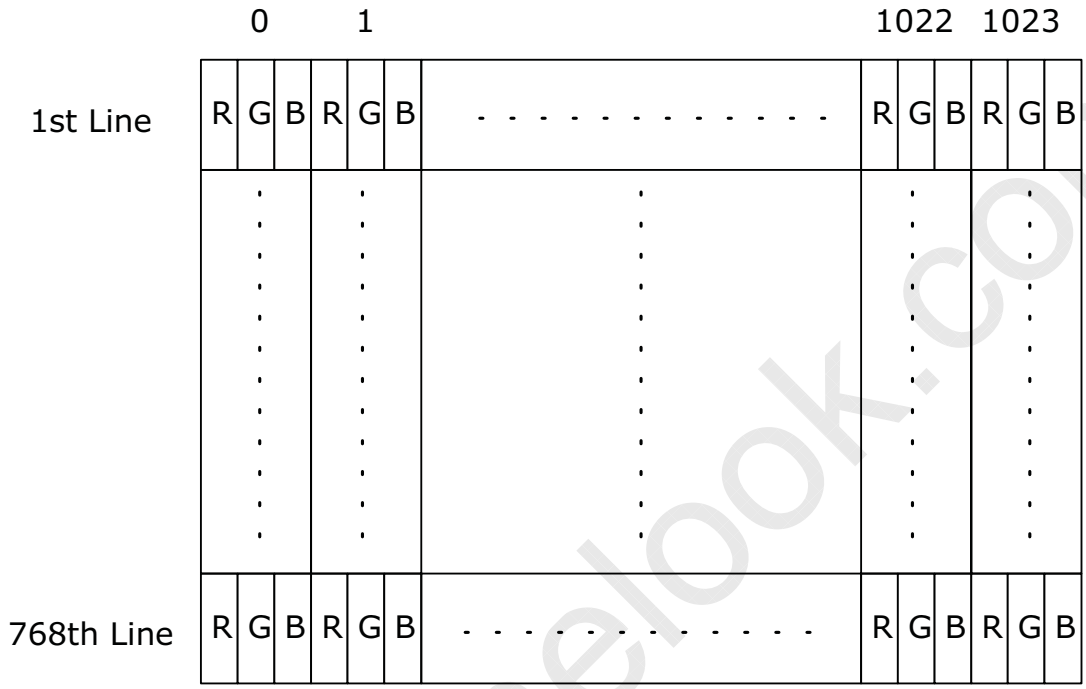
6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Backlight Characteristics

7.1 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

7.2 Parameter guide line for CFL Inverter

Symbol	Parameter	Min	D.P Note 1	Max	Units	Condition
(L63)	White Luminance	120	150	-	[cd/m^2]	(Ta=25℃)
ICFL	CCFL current	2.0	6.0	7.5	[mA] rms	(Ta=25℃)
ICFLL	CCFL Inrush current	-	-	20	[mA]	**Note 2**
fCFL	CCFL Frequency	40	50	60	[KHz]	(Ta=25℃) **Note 3**
ViCFL	CCFL Ignition Voltage			1220	[Volt] rms	(Ta= 0℃) **Note 5**
VCFL	CCFL Discharge Voltage (Reference)		601		[Volt] rms	(Ta=25℃) **Note 4**
PCFL	CCFL Power consumption		3.6		[Watt]	(Ta=25℃) **Note 4**

Note 1: Design Point-2 ; At White Luminance 150 cd/m^2, PCFL=3.6W is required.
Note 2: Duration=50 [msec]
Note 3: CCFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD
Note 4: Calculator value for reference (ICFL×VCFL=PCFL)
Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 880 voltage. Lamp units need 880 voltage minimum for ignition.

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8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86DGG (Texas Instruments) or equivalent.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency		65.00		[MHz]
tck	DTCLK cycle time		15.38		[nsec]
tx	X total time	1206	1344	2047	[tck]
tacx	X active time	129	1024		[tck]
tbkx	X blank time	90	320		[tck]
Hsync	H frequency		48.363		[KHz]
Hsw	H-Sync width	2	136		[tck]
Hbp	H back porch	1	160		[tck]
Hfp	H front porch	0	24		[tck]
ty	Y total time	771	806	1023	[tx]
tacy	Y active time		768		[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	2	6		[tx]
Vfp	V-sync front porch	1	3		[tx]
Vbp	V-sync back porch	7	29	63	[tx]

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition

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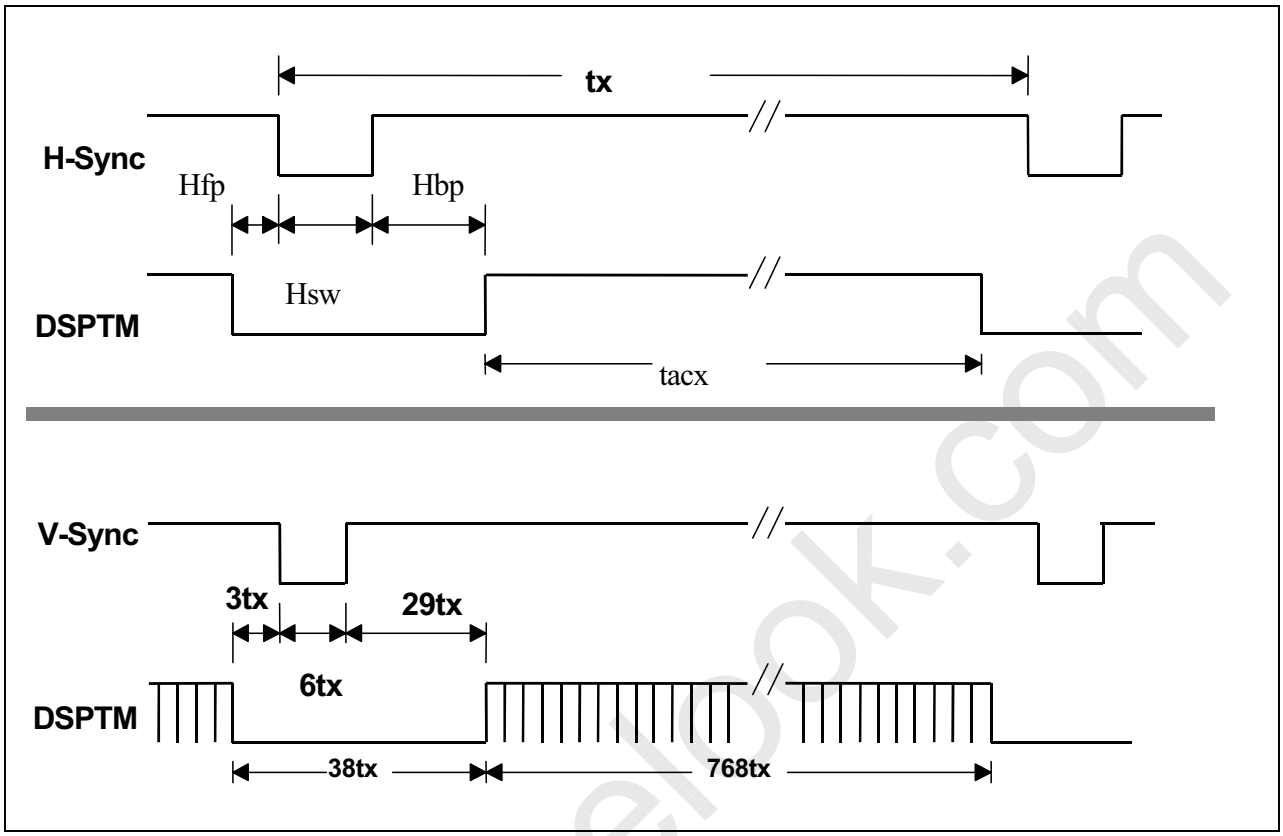

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9.0 Power Consumption

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 100uF typ.
PDD	VDD Power		1.2	1.3	[Watt]	All Black Pattern
PDDmax	VDD Power max			1.60	[Watt]	Sub-pixel checker
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

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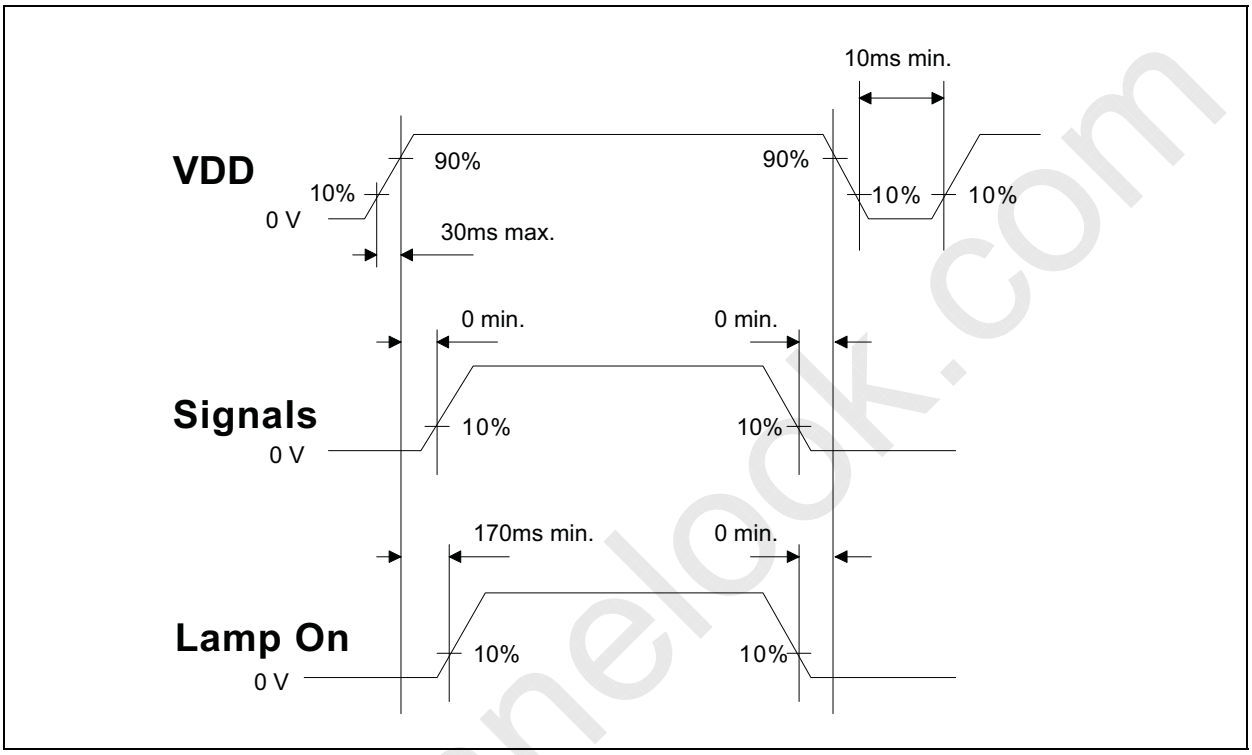
10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



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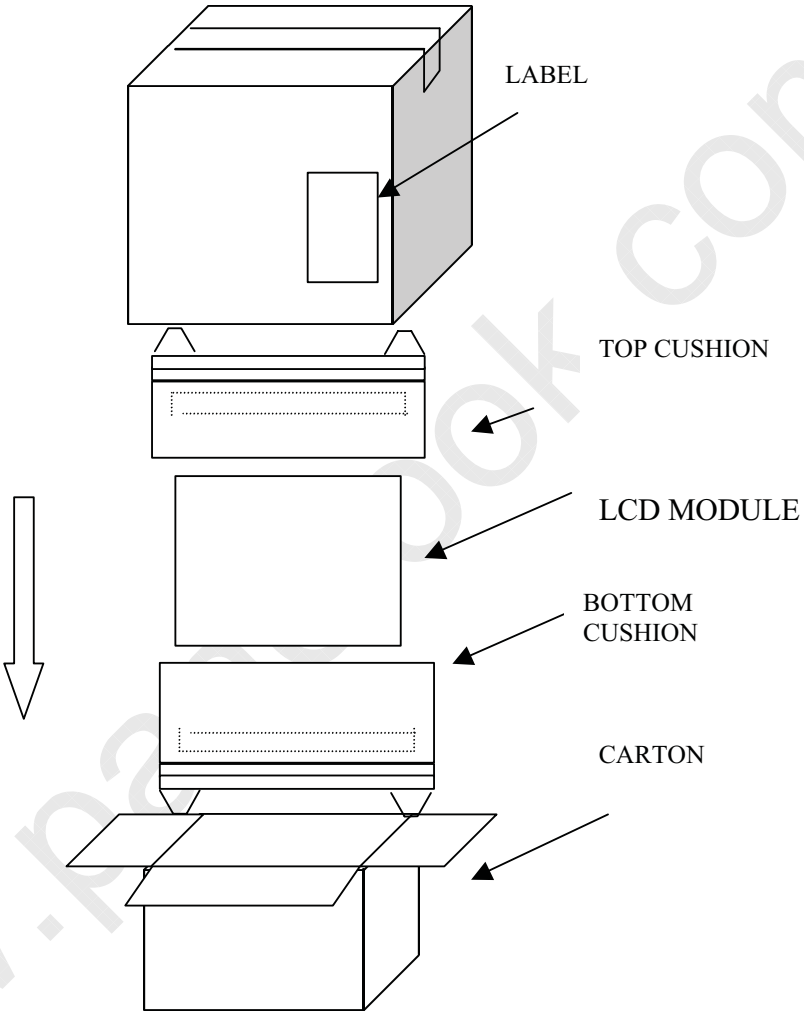
11.0 Packing dimension

Module weight : less than 480 gm.

Carton dimension: The outside dimension of carton is 390 ^{L} mm x 360 ^{W} mm x 455 ^{H} mm

Shipping Weight: less than 8.5 Kg for each carton.



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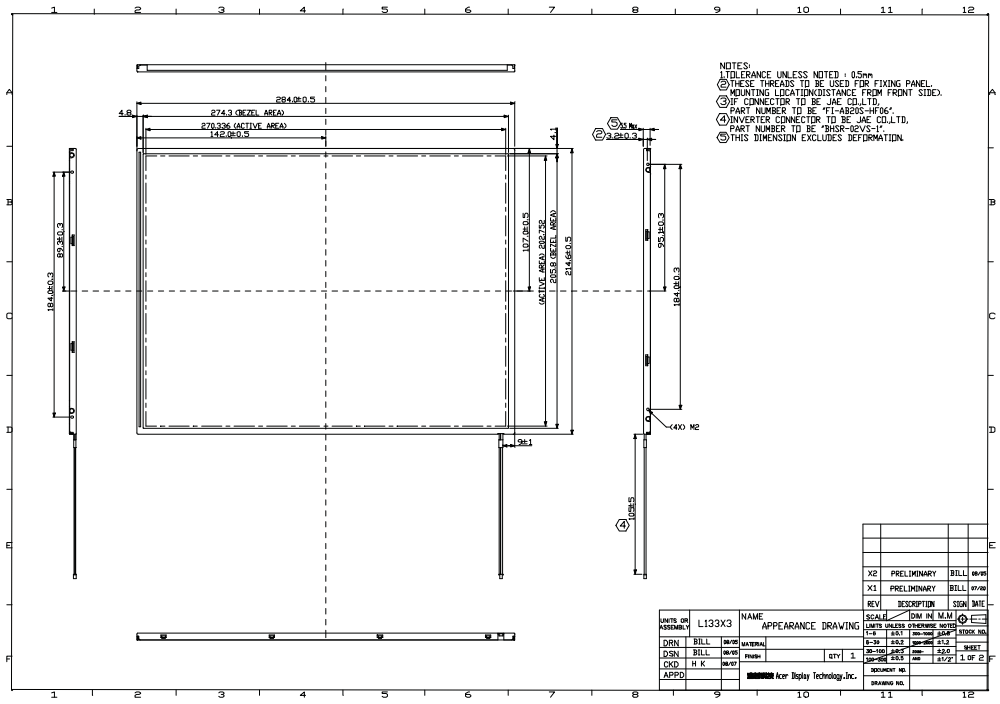

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