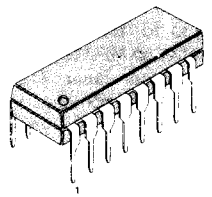
8-BIT ADDRESSABLE LATCHED DRIVER

16 DIP



The KT8518 is an 8-Bit addressable latched driver with three address inputs (A0, A1, A2), a data input (D), an active low enable input (EN), an active low clear input (CLR) and eight high current parallel latch outputs (Q0 ~ Q7) which sink current to ground.
When the enable (EN) is high and the clear (CLR) is low all outputs (Q0 ~ Q7) are high (OFF). Eight-channel demultiplexing or active low 1-of-8 decoding with output enable operation occurs when the clear (CLR) and the enable (EN) inputs are low.
When the clear (CLR) input is high and the enable (EN) input is low the selected output (Q0 ~ Q7), determined by the address inputs (A0, A1, A2), follows the data (D) input (D = 0 turns "OFF" and D = 1 turns "ON" the addressed high current output).
When the enable (EN) input goes high, the contents of the latch are stored.

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8518	16DIP	0° ~ 70°C

BLOCK DIAGRAM

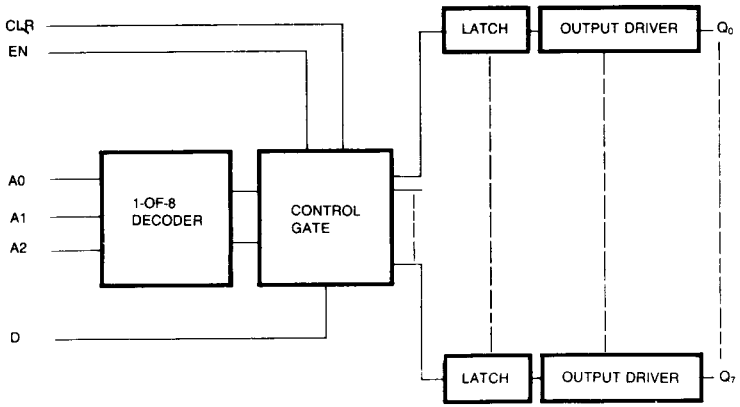


Fig. 1

PIN CONFIGURATION

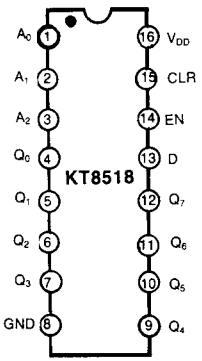


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	Description
1, 2, 3	A0, A1, A2	address inputs
4, 5, 6, 7, 9, 10, 11, 12*	Q0 - Q7	high current parallel latch output
13	D	data input
14	EN	enable (active low)
15	CLR	clear input (active low)
8	GND	Power
16	VDD	

MODE SELECTION

EN	CLR	Mode
L	H	Addressable Latch
H	H	Latch
L	L	1-of-8 Decoding
H	L	All Outputs OFF

TRUTH TABLE

INPUTS						OUTPUTS								MODE
CLR	EN	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	ALL OUTPUT OFF
L	L	L	L	L	L	H	H	H	H	H	H	H	H	1-OF-8 DECODING
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	-	LATCH
H	L	L	L	L	L	H	Qn-1	-	-	-	-	-	-	ADDRESSABLE LATCH
H	L	H	L	L	L	L	Qn-1	-	-	-	-	-	-	
H	L	L	H	L	L	Qn-1	H	Qn-1	-	-	-	-	-	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
\	\	\	\	\	\	\	\	\	\	\	\	\	\	
H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	H	
H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	L	

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 ~ 7.0	V
Input Voltage Range	V_I	−0.5 ~ 7.0	V
Output Voltage	V_O	0 ~ 7.0	V
Continuous Output Current (Each Driver)	$I_{O(CON)}$	100	mA
Operating Temperature Range	T_{OPR}	0 ~ 70	°C
Storage Temperature Range	T_{STG}	−25 ~ 150	°C

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0°C ~ 70°C)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IH}		2.0			V
		V_{IL}				0.8	
Input Damp Diode Voltage		$V_{I(D)}$	V_{CC} = min I_{IN} = −18mA		−0.65	−1.5	V
Input Current		I_{IH}	$V_{IN} = V_{DD}$			1	μA
		I_{IL}	V_{IN} = GND			−1	
Output Voltage 1		V_{OL1}	I_{OL} = 80mA Each Driver			0.5	V
Output Voltage 2		V_{OL2}	I_{OL} = 40mA All Outputs Low			0.4	V
Operating Current	All Outputs Low	I_{DDL}	No Output Load			10	μA
	All Outputs High	I_{DDH}				10	
Clamp Diode Leakage Current		$I_{LKG(CD)}$				100	μA
Clamp Diode Forward Voltage		V_F				1.5	V

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, C_L = 45pF, R_L = 330Ω)

Characteristic		Symbol	Min	Typ	Max	Unit
PROPAGATION DELAY TIME						nS
	Any Input to Output	$t_{D(P)LH}$		45	90	
		$t_{D(P)HL}$		25	50	
	EN Pulse Width	$t_{W(EN)}$	15			
	CLR Pulse Width	$t_{W(CLR)}$	15			
	Set Up Time (D to EN)	$t_{SU(D-EN)}$	10			
	Hold Time (D to EN)	t_{HD}	0			
	Set Up Time (ADD to EN)	$t_{H(ADD-EN)}$	10			
	Hold Time (ADD to EN)	$t_{H(ADD-EN)}$	0			

6

TIMING DIAGRAM

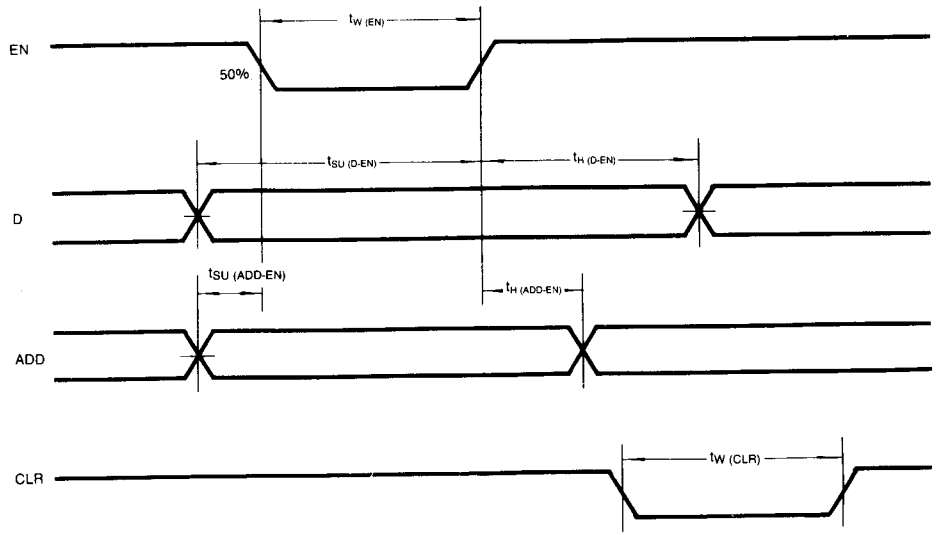


Fig. 3