

isc Silicon NPN Power Transistor**KSH340****DESCRIPTION**

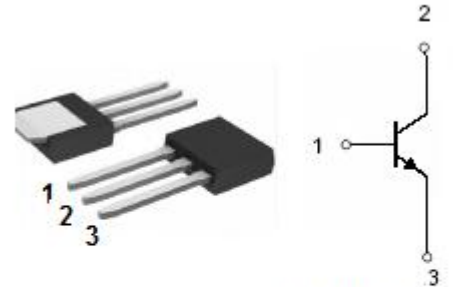
- Lead formed for surface mount applications(NO suffix)
- Straight lead(IPAK, “—I” suffix)
- DPAK for surface mount applications
- 100% avalanche tested
- Minimum Lot-to-Lot variations for robust device performance and reliable operation

APPLICATIONS

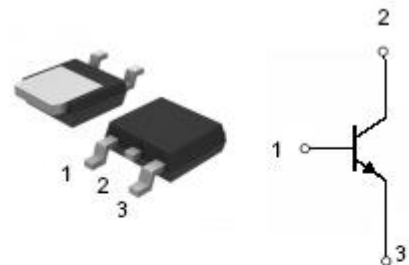
- High voltage power transistors

ABSOLUTE MAXIMUM RATINGS($T_a=25^\circ\text{C}$)

SYMBOL	PARAMETER	VALUE	UNIT
V_{CBO}	Collector-Base Voltage	300	V
V_{CEO}	Collector-Emitter Voltage	300	V
V_{EBO}	Emitter-Base Voltage	3	V
I_C	Collector Current-Continuous	0.5	A
P_C	Total Power Dissipation @ $T_a=25^\circ\text{C}$	1.56	W
P_C	Total Power Dissipation @ $T_c=25^\circ\text{C}$	15	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{stg}	Storage Temperature Range	-55~150	$^\circ\text{C}$

**IPAK**

**PIN : 1 Base
2 Collector
3 Emitter
TO-251 Package**

**DPAK**

**PIN : 1 Base
2 Collector
3 Emitter
TO-252 Package**

isc Silicon NPN Power Transistor**KSH340****ELECTRICAL CHARACTERISTICS**T_c=25°C unless otherwise specified

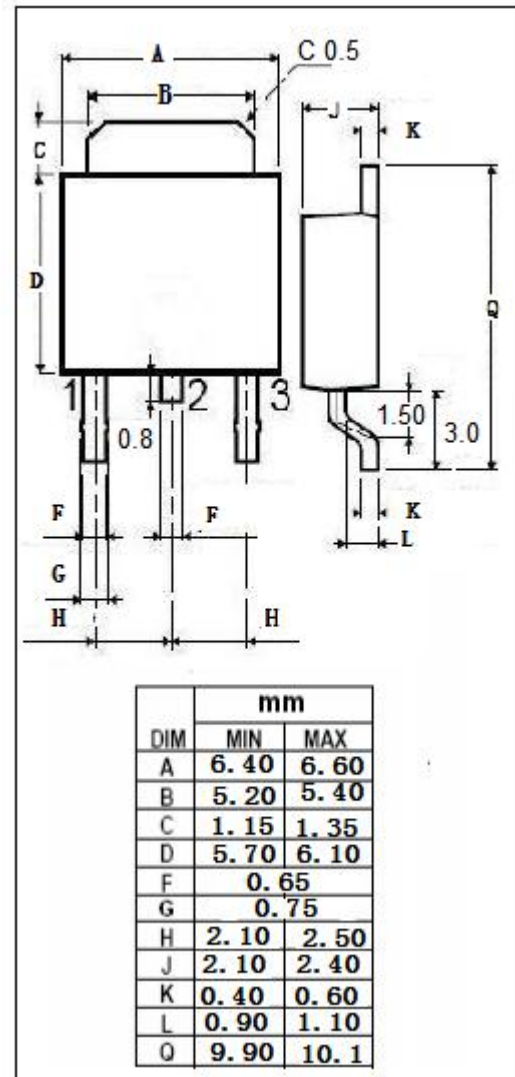
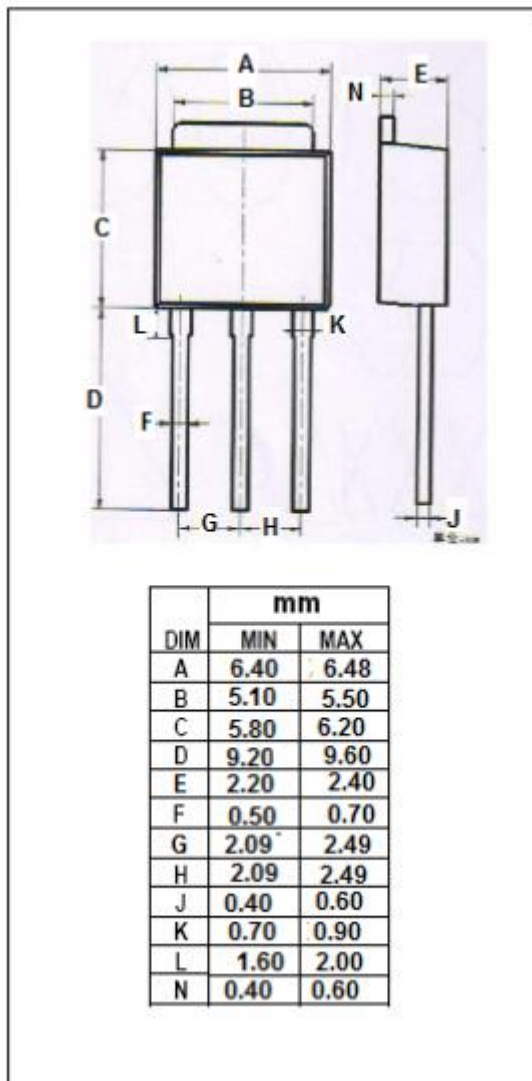
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{(BR)CEO} *	Collector-Emitter Breakdown Voltage	I _C = 1mA; I _B = 0	300			V
I _{CBO}	Collector Cutoff Current	V _{CB} = 300V; I _E = 0			100	uA
I _{EBO}	Emitter Cutoff Current	V _{EB} =3V; I _C = 0			100	uA
h _{FE1} *	DC Current Gain	I _C = 50mA; V _{CE} = 10V	30		240	

*:Pulse test PW≤300us,duty cycles≤2%

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KSH340

Outline Drawing



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