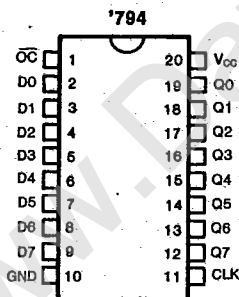
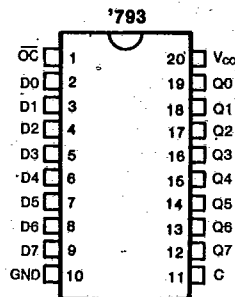


KS54AHCT 793/794**8-Bit Latch/Register
with Readback****Preliminary Specifications**

T-46-07-05

FEATURES

- I/O port configuration enables output data back onto input bus
- Latch ('793) and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5\text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^{\circ}\text{C}$
KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATIONS**DESCRIPTION**

These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The Data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when C is high, and it is latched when C goes low. The output control ($\overline{OC}$) is used to enable data on the D0-D7 pins. when $\overline{OC}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OC}$ is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'793

C	$\overline{OC}$	Q	D
L	L	Q_0^{**}	Output, Q
L	H	Q_0^{**}	Input
H†	L	D^*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

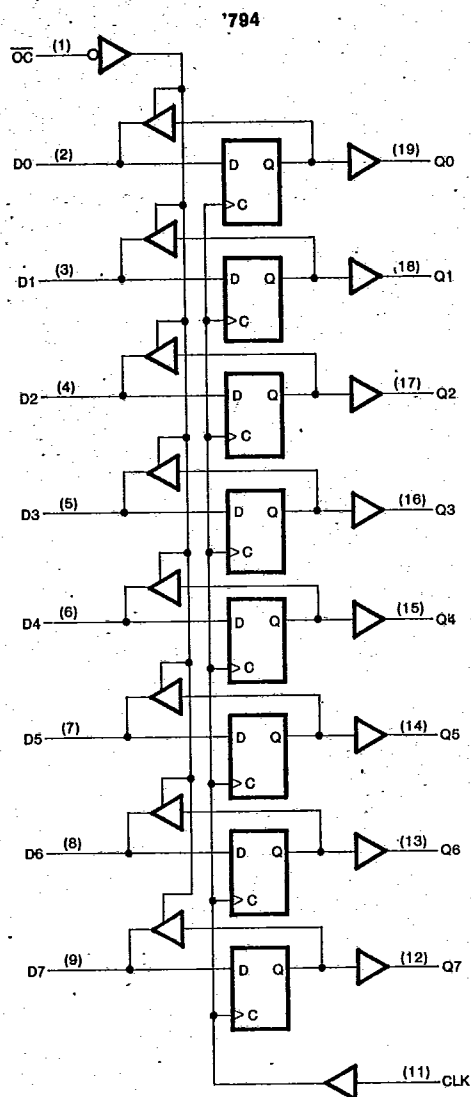
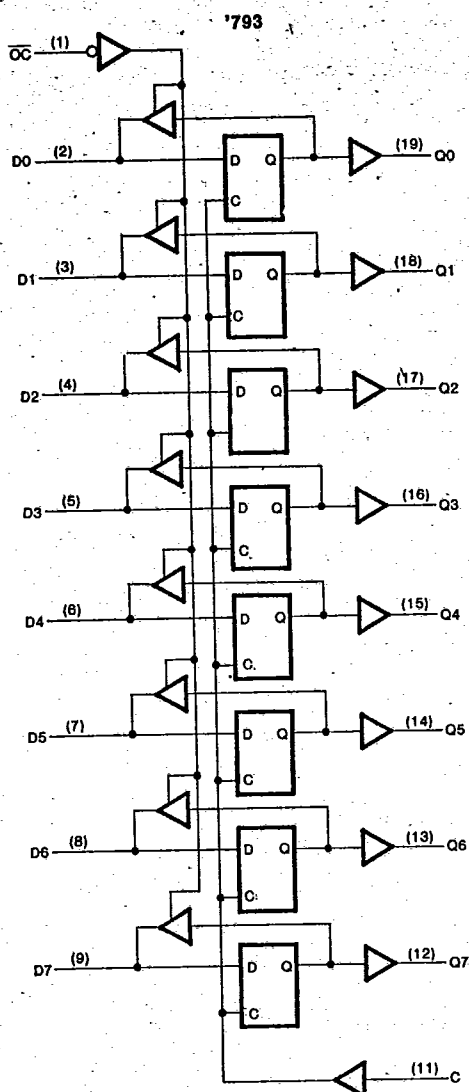
'794

CLK	$\overline{OC}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0 .

KS54AHCT
KS74AHCT**793/794****8-Bit Latch/Register
with Readback**

T-46-D7-05

LOGIC DIAGRAMS

SAMSUNG SEMICONDUCTOR

KS54AHCT 793/794
KS74AHCT**8-Bit Latch/Register
with Readback**

T-46-07-05

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} ... -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating ConditionsSupply Voltage, V_{CC} 4.5V to 5.5VDC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}

Operating Temperature

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT	Unit
				Typ	T _a = -40°C to +85°C	T _a = -55°C to +125°C	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-6mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I _{OZ}	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



KS54AHCT 793/794
KS74AHCT
8-Bit Latch/Register
with Readback

T-46-07-05

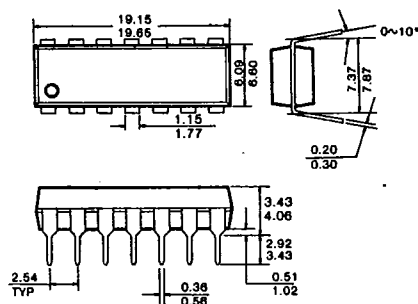
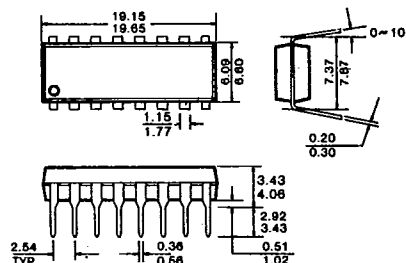
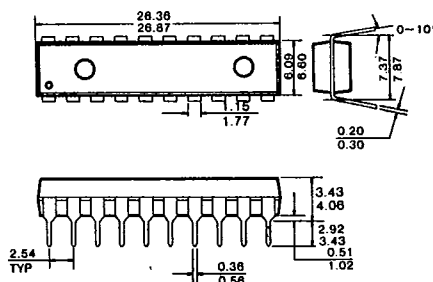
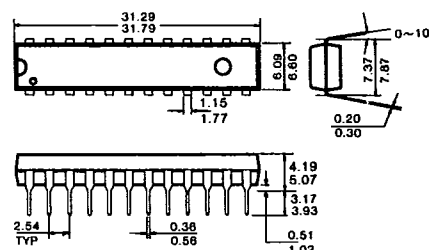
AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT793, AHCT794

Characteristic	Symbol	Conditions ¹	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency (794 only)	f_{max}	$C_L = 50\text{pF}$	60	40		35		MHz
Propagation Delay D to Any Q (793 only)	t_{PLH}	$C_L = 50\text{pF}$	10		16		19	ns
		$C_L = 150\text{pF}$	13		21		25	
	t_{PHL}	$C_L = 50\text{pF}$	10		16		19	ns
		$C_L = 150\text{pF}$	13		21		25	
Propagation Delay CLK/C to Any Q	t_{PLH}	$C_L = 50\text{pF}$	12		20		24	ns
		$C_L = 150\text{pF}$	15		25		30	
	t_{PHL}	$C_L = 50\text{pF}$	12		20		24	ns
		$C_L = 150\text{pF}$	15		25		30	
Enable Time, OC to D	t_{pZH}	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	14		23		28	
	t_{pZL}	$C_L = 50\text{pF}$ (for 793)	11		18		22	ns
		$C_L = 150\text{pF}$	13		23		28	
Disable Time OC to D	t_{pHZ}	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$	11		18		22	ns
	t_{pLZ}	$C_L = 50\text{pF}$ (C=Low for 793)	11		18		22	
Pulse Width, CLK/C High or low	t_w		9	14		19		ns
Setup time D before C $\uparrow$ (793) D before CLK $\uparrow$ (794)	t_{su}		6	10		12		ns
			10	15		20		
Hold Time D after C $\downarrow$ (793) D after CLK $\downarrow$ (794)	t_h		9	10		12		ns
			-3	0		0		
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	OC=GND	10					pF
Power Dissipation Capacitance*	C_{PD}							ns

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

7

**SAMSUNG SEMICONDUCTOR**

1675

A-04

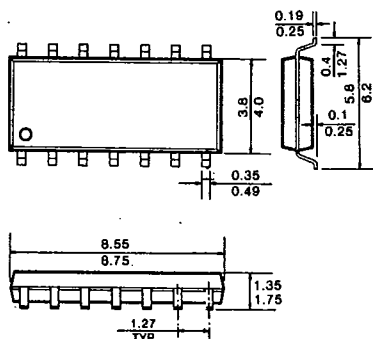
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PACKAGE DIMENSIONS

T-90-20

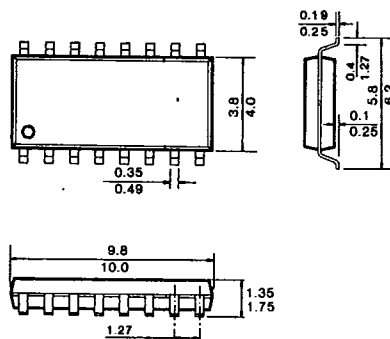
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Unit: mm



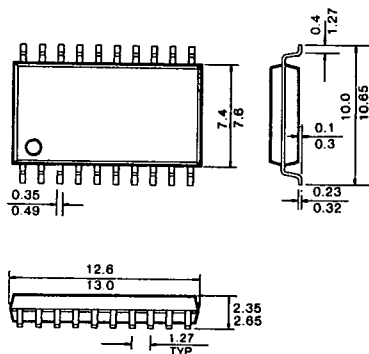
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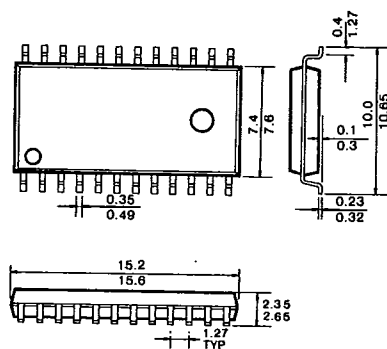
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Unit: mm



24-Pin SOP

Unit: mm



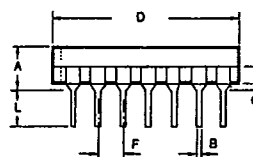
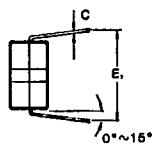
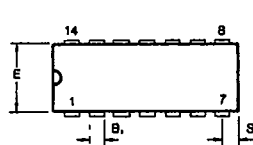
SAMSUNG SEMICONDUCTOR

1676

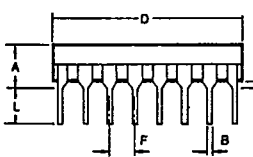
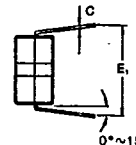
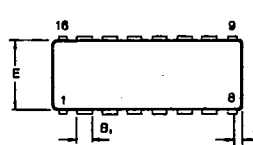
A-05

PACKAGE DIMENSIONS

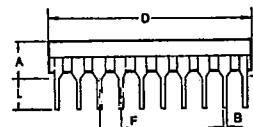
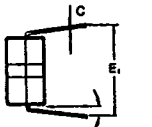
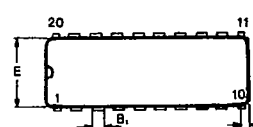
T-90-20

2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

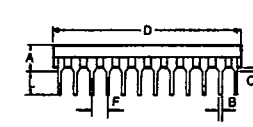
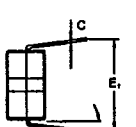
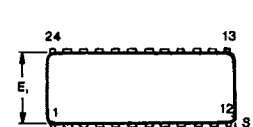
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93



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A-06

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