

**KS54AHCT 78**  
**KS74AHCT****Dual J-K Flip-Flops with Preset,  
Common Clear & Common Clock**

T-46-07-07

**FEATURES**

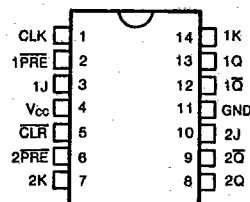
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA}$  @  $V_{OL} = 0.5 \text{ V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

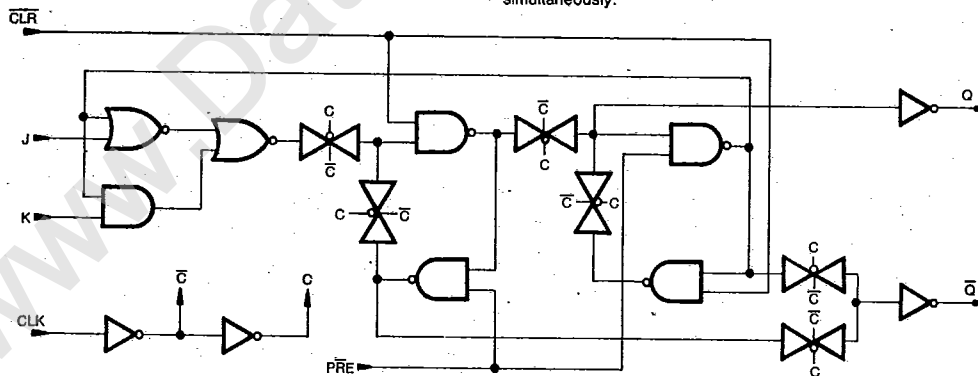
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION****FUNCTION TABLE**

| Inputs |     |     |   |   | Outputs |             |
|--------|-----|-----|---|---|---------|-------------|
| PRE    | CLR | CLK | J | K | Q       | $\bar{Q}$   |
| L      | H   | X   | X | X | H       | L           |
| H      | L   | X   | X | X | L       | H           |
| L      | L   | X   | X | X | H*      | H*          |
| H      | H   | ↓   | L | L | $Q_0$   | $\bar{Q}_0$ |
| H      | H   | ↓   | H | L | H       | L           |
| H      | H   | ↓   | L | H | L       | H           |
| H      | H   | ↓   | H | H | TOGGLE  | TOGGLE      |
| H      | H   | H   | X | X | $Q_0$   | $\bar{Q}_0$ |

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

**LOGIC DIAGRAM**

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Common Clear & Common Clock**

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**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

| Characteristic                       | Symbol           | Test Conditions                                                                                                           | KS74AHCT               |                                 |                                  | Unit                        |    |
|--------------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------|------------------------|---------------------------------|----------------------------------|-----------------------------|----|
|                                      |                  |                                                                                                                           | T <sub>a</sub> = 25°C  | T <sub>a</sub> = -40°C to +85°C | T <sub>a</sub> = -55°C to +125°C |                             |    |
|                                      |                  |                                                                                                                           | Typ                    | Guaranteed Limits               |                                  |                             |    |
| Minimum High-Level Input Voltage     | V <sub>IH</sub>  |                                                                                                                           |                        | 2.0                             | 2.0                              | 2.0                         | V  |
| Maximum Low-Level Input Voltage      | V <sub>IL</sub>  |                                                                                                                           |                        | 0.8                             | 0.8                              | 0.8                         | V  |
| Minimum High-Level Output Voltage    | V <sub>OH</sub>  | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> =-20μA<br>I <sub>O</sub> =-4mA                      | V <sub>CC</sub><br>4.2 | V <sub>CC</sub> -0.1<br>3.98    | V <sub>CC</sub> -0.1<br>3.84     | V <sub>CC</sub> -0.1<br>3.7 | V  |
| Maximum Low-Level Output Voltage     | V <sub>OL</sub>  | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> =20μA<br>I <sub>O</sub> =4mA<br>I <sub>O</sub> =8mA | 0                      | 0.1<br>0.26<br>0.39             | 0.1<br>0.33<br>0.5               | 0.1<br>0.4                  | V  |
| Maximum Input Current                | I <sub>IN</sub>  | V <sub>IN</sub> =V <sub>CC</sub> or GND                                                                                   |                        | ±0.1                            | ±1.0                             | ±1.0                        | μA |
| Maximum Quiescent Supply Current     | I <sub>CC</sub>  | V <sub>IN</sub> =V <sub>CC</sub> or GND<br>I <sub>OUT</sub> =0μA                                                          |                        | 4.0                             | 40.0                             | 80.0                        | μA |
| Additional Worst Case Supply Current | ΔI <sub>CC</sub> | per input pin<br>V <sub>I</sub> =2.4V<br>other inputs:<br>at V <sub>CC</sub> or GND<br>I <sub>OUT</sub> =0μA              |                        | 2.7                             | 2.9                              | 3.0                         | mA |



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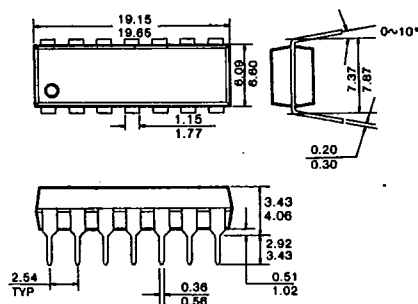
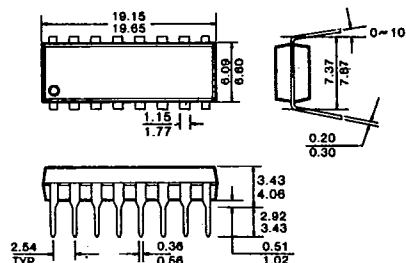
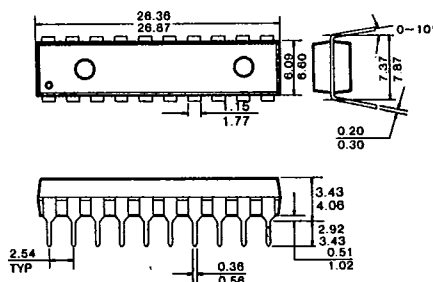
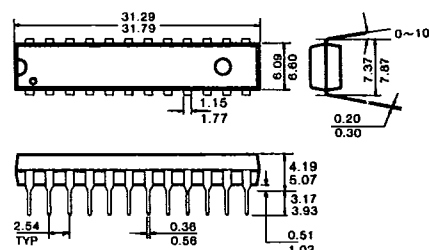
**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT78

| Characteristic                                     | Symbol              | Conditions†           | T <sub>a</sub> = 25°C<br>V <sub>CC</sub> = 5.0V | KS74AHCT<br>T <sub>a</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 5.0V ± 10% |     | KS54AHCT<br>T <sub>a</sub> = -55°C to +125°C<br>V <sub>CC</sub> = 5.0V ± 10% |     | Unit |
|----------------------------------------------------|---------------------|-----------------------|-------------------------------------------------|-----------------------------------------------------------------------------|-----|------------------------------------------------------------------------------|-----|------|
|                                                    |                     |                       | Typ                                             | Min                                                                         | Max | Min                                                                          | Max |      |
| Maximum Clock Frequency                            | f <sub>max</sub>    | C <sub>L</sub> = 50pF | 45                                              | 30                                                                          |     | 25                                                                           |     | MHz  |
| Propagation Delay,<br>CLK to Q or $\bar{Q}$        | t <sub>PLH</sub>    |                       | 10                                              |                                                                             | 17  |                                                                              | 20  | ns   |
|                                                    | t <sub>PHL</sub>    |                       | 10                                              |                                                                             | 17  |                                                                              | 20  |      |
| Propagation Delay,<br>PRE or CLR to Q or $\bar{Q}$ | t <sub>PLH</sub>    |                       | 10                                              |                                                                             | 17  |                                                                              | 20  | ns   |
|                                                    | t <sub>PHL</sub>    |                       | 10                                              |                                                                             | 17  |                                                                              | 20  |      |
| Setup Time<br>before CLK↓                          | J or K              | t <sub>su</sub>       | 10                                              | 17                                                                          |     | 20                                                                           |     | ns   |
|                                                    | PRE or CLR Inactive |                       | 10                                              | 17                                                                          |     | 20                                                                           |     |      |
| Hold Time, J or K after CLK↓                       | t <sub>h</sub>      |                       | -3                                              | 0                                                                           |     | 0                                                                            |     | ns   |
| Pulse Width                                        | CLK High or Low     | t <sub>w</sub>        | 8                                               | 13                                                                          |     | 15                                                                           |     | ns   |
|                                                    | PRE or CLR Low      |                       | 8                                               | 13                                                                          |     | 15                                                                           |     |      |
| Input Capacitance                                  | C <sub>IN</sub>     |                       | 5                                               |                                                                             |     |                                                                              |     | pF   |
| Power Dissipation Capacitance*                     | C <sub>PD</sub>     | (per flip-flop)       | 40                                              |                                                                             |     |                                                                              |     | pF   |

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.



**PACKAGE DIMENSIONS***T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

7

**SAMSUNG SEMICONDUCTOR**

1675

A-04

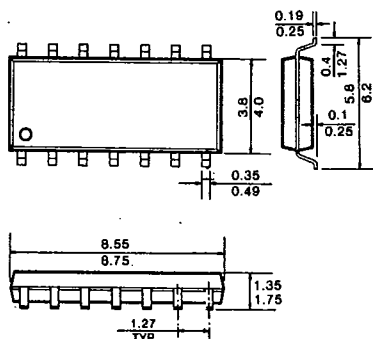
781

# PACKAGE DIMENSIONS

T-90-20

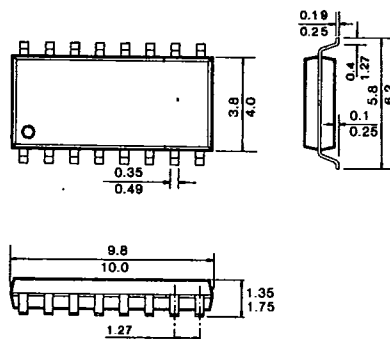
14-Pin SOP

Unit: mm



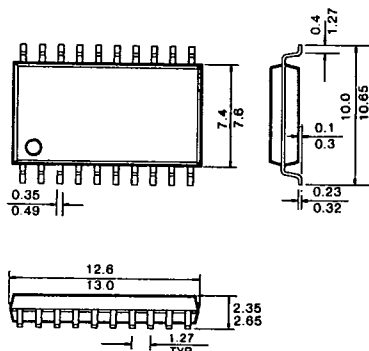
16-Pin SOP

Unit: mm



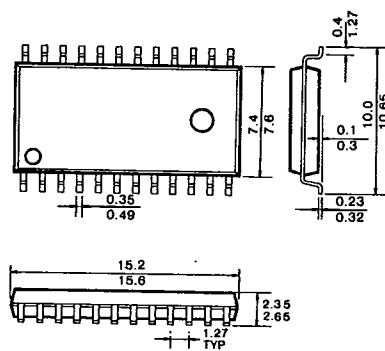
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm



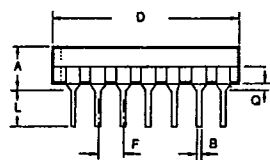
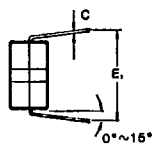
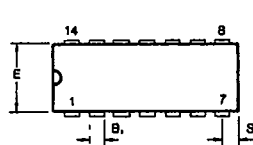
SAMSUNG SEMICONDUCTOR

1676

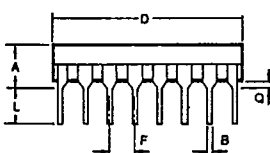
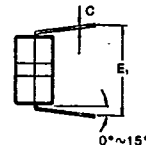
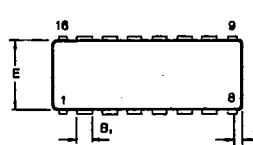
A-05

**PACKAGE DIMENSIONS**

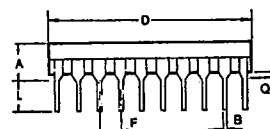
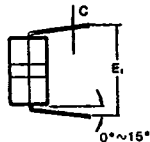
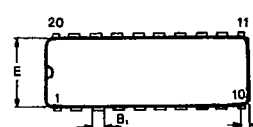
T-90-20

**2. CERAMIC PACKAGES****14-Pin Ceramic DIP Units: mm**

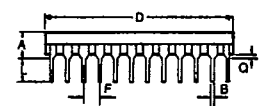
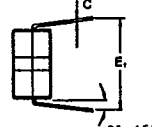
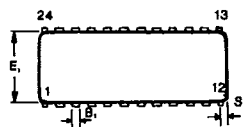
| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | —           | 5.08  |
| B              | 0.38        | 0.58  |
| B <sub>1</sub> | 1.40        | 1.78  |
| C              | 0.20        | 0.38  |
| D              | 18.16       | 19.56 |
| E              | 8.10        | 7.49  |
| E <sub>1</sub> | 7.62        | 10.03 |
| F              | 2.54        |       |
| L              | 3.18        | 4.19  |
| Q              | 0.51        | 1.02  |
| S              | 1.91        | 2.29  |

**16-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | —           | 5.08  |
| B              | 0.38        | 0.58  |
| B <sub>1</sub> | 1.40        | 1.78  |
| C              | 0.20        | 0.38  |
| D              | 19.05       | 19.94 |
| E              | 8.10        | 7.49  |
| E <sub>1</sub> | 7.62        | 10.03 |
| F              | 2.54        |       |
| L              | 3.18        | 4.19  |
| Q              | 0.51        | 1.02  |
| S              | 0.51        | 1.14  |

**20-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | 4.06        | 5.08  |
| B              | 0.38        | 0.53  |
| B <sub>1</sub> | 1.14        | 1.52  |
| C              | 0.20        | 0.38  |
| D              | 25.78       | 26.93 |
| E              | 8.10        | 8.60  |
| E <sub>1</sub> | 7.77        | 7.98  |
| F              | 2.54        |       |
| L              | 3.73        | 4.01  |
| Q              | 0.38        | 0.89  |
| S              | 0.51        | 1.14  |

**24-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | 4.06        | 5.08  |
| B              | 0.38        | 0.53  |
| B <sub>1</sub> | 1.14        | 1.52  |
| C              | 0.20        | 0.38  |
| D              | 31.50       | 32.84 |
| E              | 7.24        | 7.75  |
| E <sub>1</sub> | 7.77        | 7.98  |
| F              | 2.54        |       |
| L              | 3.73        | 4.01  |
| Q              | 0.508       | 1.778 |
| S              | 1.85        | 1.93  |

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SAMSUNG SEMICONDUCTOR

1677

A-06

783