KS54AHCT 646/648
KS74AHCT

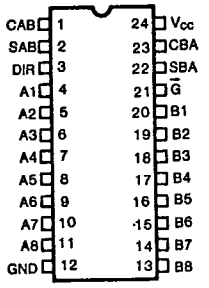
Octal 3-State Bus Transceivers with Registers

T-52-31

FEATURES

- 8 bi-directional data paths
- Transmits direct or stored data in either direction
- 24-pin slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to + 85°C
  KS54HACT: −55°C to + 125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

$\overline{G}$ (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.

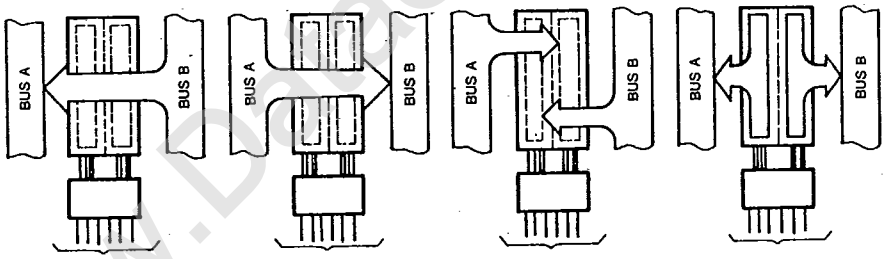
DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.

SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.

CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the $\overline{G}$ and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

Real-Time transfer bus B to bus A

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

Real-Time transfer bus A to bus B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Storage from A AND/OR B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

Transfer stored data to A AND/OR B

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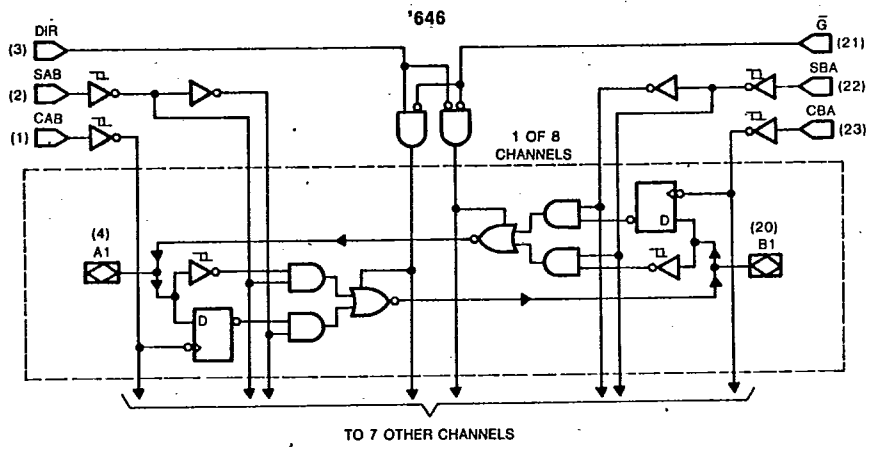
Octal 3-State Bus Transceivers with Registers

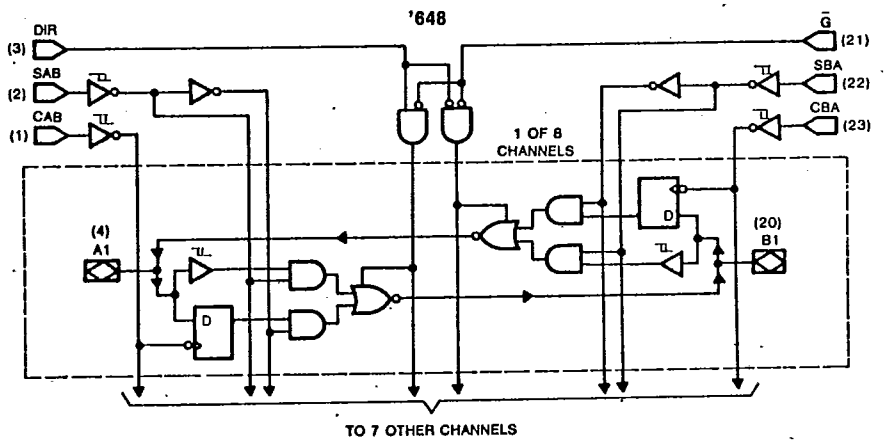
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
X	X	↑	X	X	X	Input	Input'	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B data to A bus	Real-Time $\bar{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\bar{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-Time A data to B bus	Real-Time $\bar{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\bar{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\bar{G}$ and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS





KS54AHCT KS74AHCT 646/648 — Octal 3-State Bus Transceivers with Registers

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT646, AHCT648

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Frequency	f_{max}	C_L=50pF	45		30		25	MHz
Propagation Delay, A or B Input to B or A Output	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or High)	t_{PLH}	C_L=50pF C_L=150pF	16 19		27 33		32 38	ns
	t_{PHL}	C_L=50pF C_L=150pF	16 19		27 33		32 38	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or Low)	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Out Enable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PZH}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	14 17		22 27		26 32	ns
	t_{PZL}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	14 17		22 27		26 32	
Output Disable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PHZ}	R_L=1kΩ, C_L=50pF	13		22		26	ns
	t_{PLZ}		13		22		26	
Pulse Duration, Clocks High or low	t_w		8	12		15		ns
Set up Time, A before CABt or B before CBAt	t_{su}		8	12		15		ns
Hold Time, A after CABt or B after CBAt	t_h		−3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

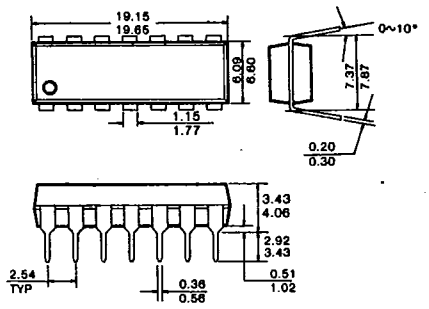
†† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PACKAGE DIMENSIONS

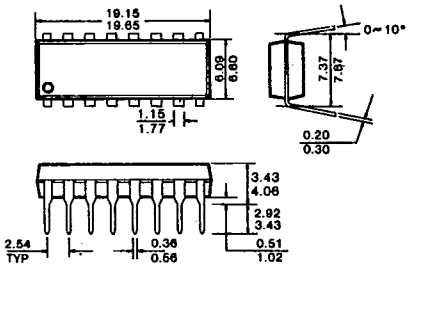
T-90-20

1. PLASTIC PACKAGES

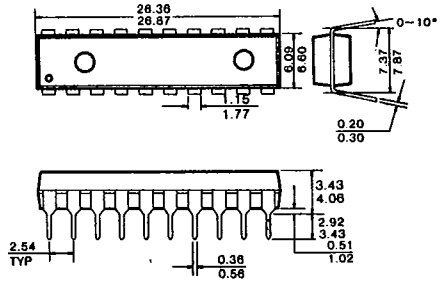
14-Pin Plastic DIP **Units: mm**



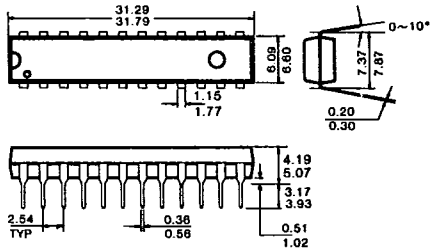
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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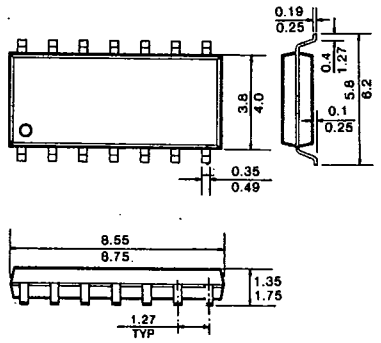
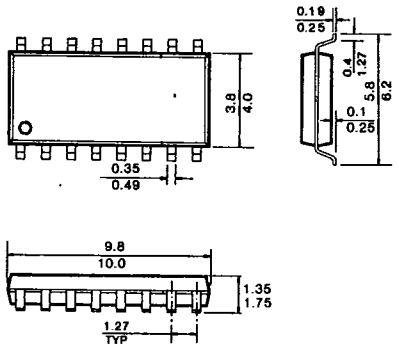
14-Pin SOP

Unit: mm



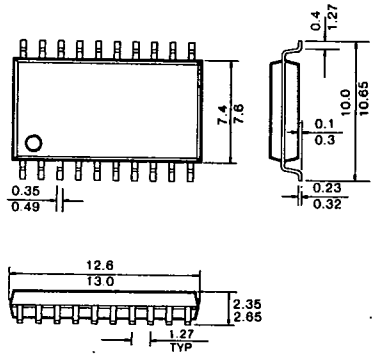
16-Pin SOP

Unit: mm



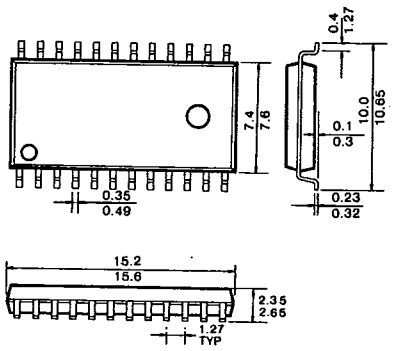
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

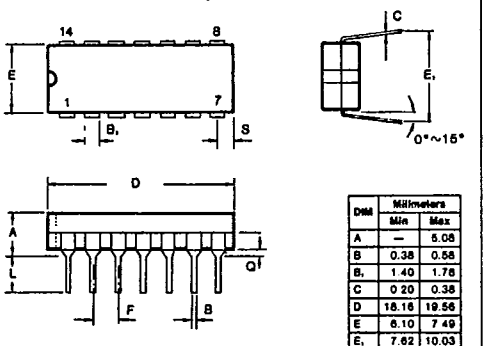


PACKAGE DIMENSIONS

T-90-20

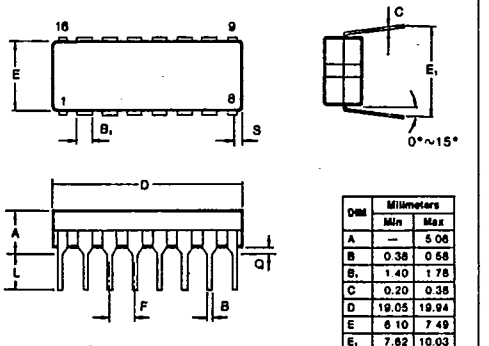
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



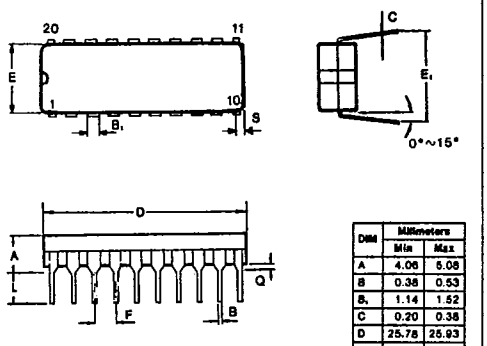
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



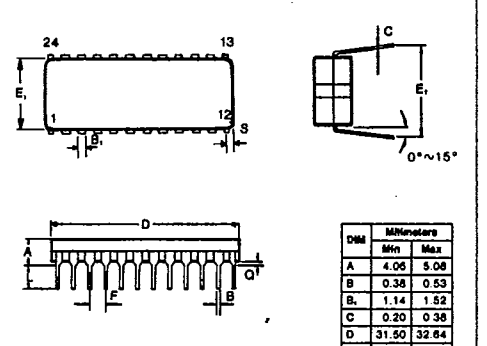
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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