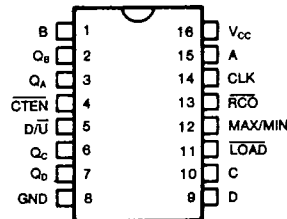


KS54AHCT 190
KS74AHCT
Synchronous 4-Bit Up/Down
Decade Counters

T-45-23-09

FEATURES

- Single down/up count control line
- Look-ahead circuit enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5 \text{ V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to $+85^{\circ}\text{C}$
 KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	LOAD	D/U	CTEN	CLK	Input	Qa	Qb
parallel load	L	X	X	X	L	L	H
		X	X	X	H	H	L
count up	H	L	I	↑	X	count up	
count down	H	H	I	↑	X	count down	
hold (do nothing)	H	X	H	X	X	no change	

RCO AND MAX/MIN FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
D/U	CTEN	CLK	Qa	Qb	Qc	Qd	MAX/MIN	RCO
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	↑	H	X	X	H	L	↑
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	↑	L	L	L	L	L	↑

H = HIGH voltage level
 L = LOW voltage level
 I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
 X = Don't care
 ↑ = LOW-to-HIGH CLK transition
 ↑ = one LOW level pulse
 ↓ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up (D/U) input. When D/U is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/U) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.



SAMSUNG SEMICONDUCTOR

KS54AHCT 190
KS74AHCT**Synchronous 4-Bit Up/Down
Decade Counters****T-45-23-09****Absolute Maximum Ratings***

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{stg} -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating ConditionsSupply Voltage, V_{CC} 4.5V to 5.5VDC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT		Unit
					T _a = -40°C to +85°C	T _a = -55°C to +125°C		
			Typ	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0		2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8		0.8	V
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84		V _{CC} -0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0		±1.0	μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0		160.0	μA
Additional Worst Case Supply Current	ΔI _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9		3.0	mA



SAMSUNG SEMICONDUCTOR

KS54AHCT
KS74AHCT

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Synchronous 4-Bit Up/Down
Decade Counters

T-45-23-09

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leq 2$ ns), AHCT190

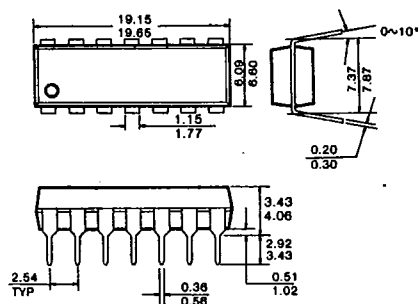
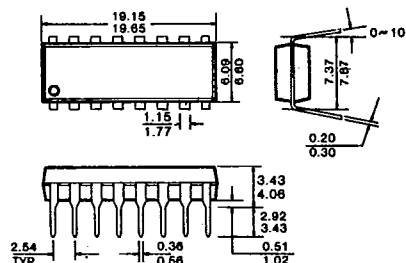
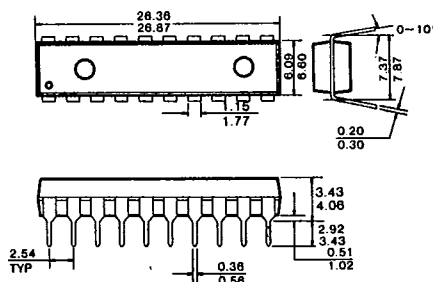
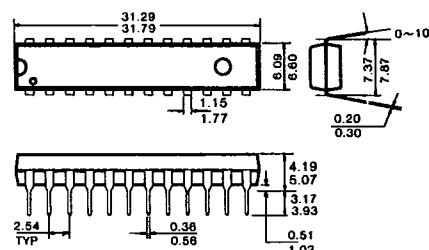
Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f _{max}	C _L = 50pF	50	30		25		MHz
Propagation Delay, LOAD to any Q	t _{PLH}		18		30		36	ns
	t _{PHL}		18		30		36	
Propagation Delay, A,B,C, D to any Q	t _{PLH}		13		21		25	ns
	t _{PHL}		13		21		25	
Propagation Delay, CLK to RCO	t _{PLH}		12		20		24	ns
	t _{PHL}		12		20		24	
Propagation Delay, CLK to any Q	t _{PLH}		11		18		22	ns
	t _{PHL}		11		18		22	
Propagation Delay, CLK to MAX/MIN	t _{PLH}		19		31		37	ns
	t _{PHL}		19		31		37	
Propagation Delay, D/U to RCO	t _{PLH}		19		32		38	ns
	t _{PHL}		19		32		38	
Propagation Delay, D/U to MAX/MIN	t _{PLH}		15		25		30	
	t _{PHL}		15		25		30	
Propagation Delay, CTEN to RCO	t _{PLH}		11		18		22	ns
	t _{PHL}		11		18		22	
Pulse Width	CLK High or Low	t _w	10		17		20	ns
	LOAD Low		12		20		25	
Setup Time	Data before LOAD†	t _{su}	10	17		20		ns
	CTEN before CLK†		10	17		20		
	D/U before CLK†		10	17		20		
	LOAD Inactive before CLK†		10	17		20		
Hold Time	Data after LOAD†	t _h	2	4		5		ns
	CTEN after CLK†		-3	0		0		
	D/U after CLK†		-3	0		0		
Input Capacitance	C _{IN}		5					pF
Power Dissipation Capacitance*	C _{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}.

† For AC switching test circuits and timing waveforms see section 2.



SAMSUNG SEMICONDUCTOR

PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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**SAMSUNG SEMICONDUCTOR**

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A-04

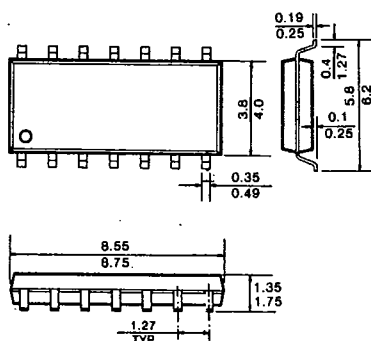
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PACKAGE DIMENSIONS

T-90-20

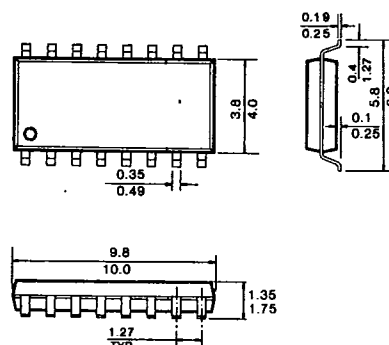
14-Pin SOP

Unit: mm



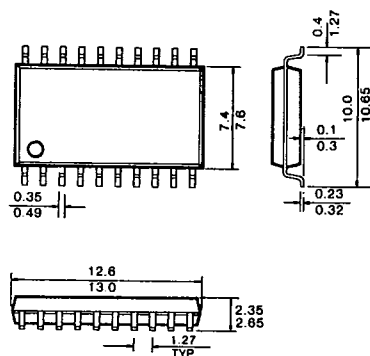
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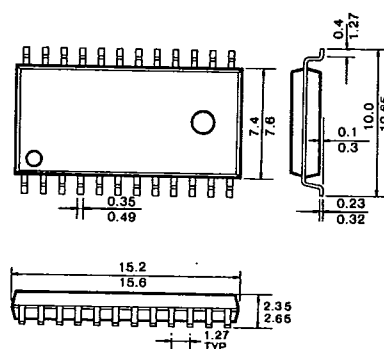
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm



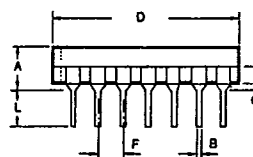
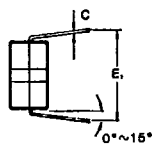
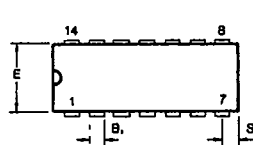
SAMSUNG SEMICONDUCTOR

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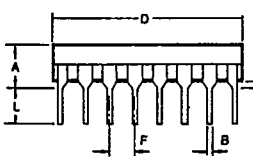
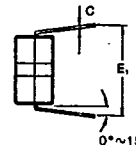
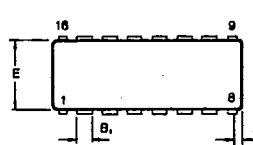
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PACKAGE DIMENSIONS

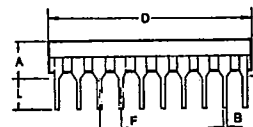
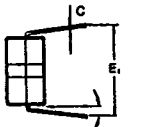
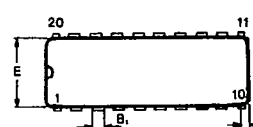
T-90-20

2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

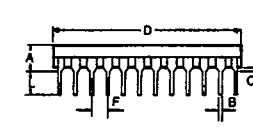
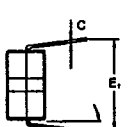
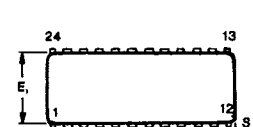
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93



SAMSUNG SEMICONDUCTOR

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