KS54AHCT 168/169
KS74AHCT 168/169

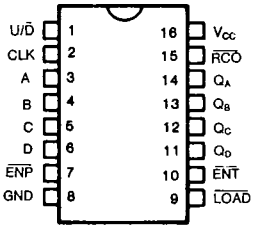
Synchronous 4-Bit Up/Down Decade and Binary Counters

T-45-23-09

FEATURES

- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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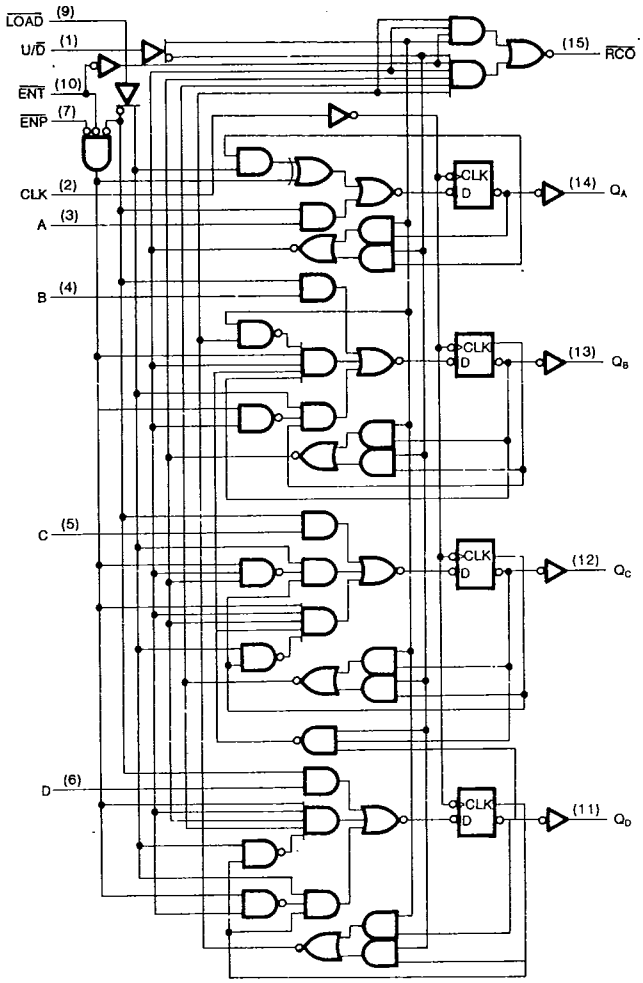
LOGIC DIAGRAMS

'168



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KS74AHCT

Synchronous 4-Bit Up/Down Decade and Binary Counters

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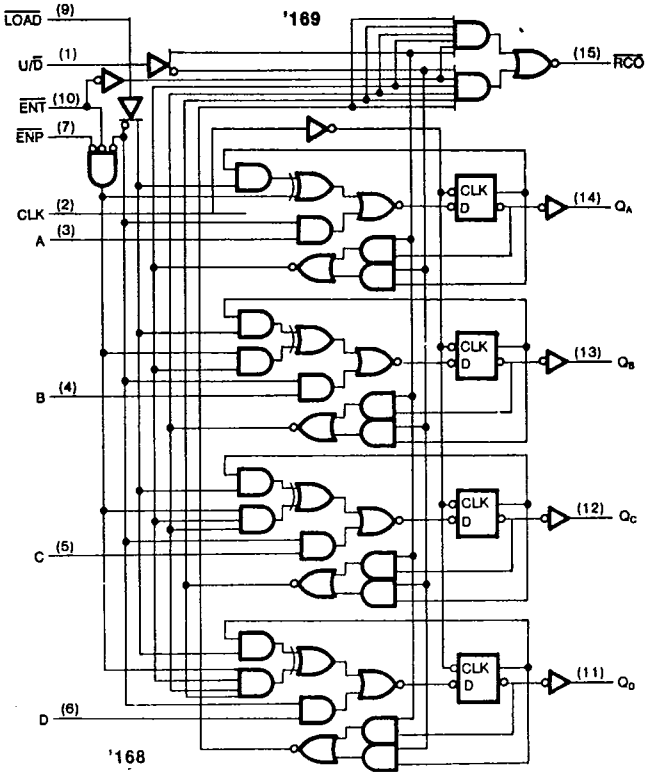
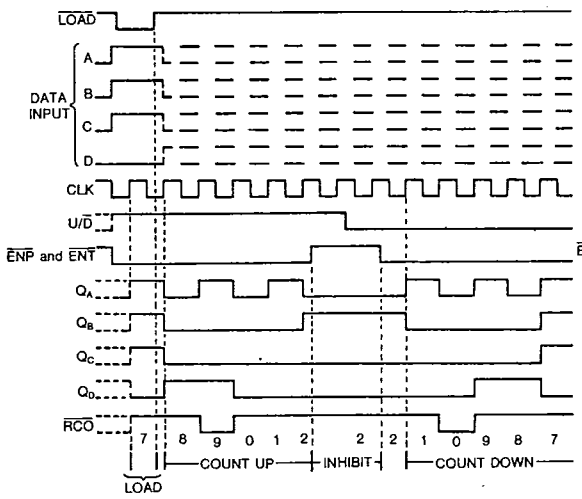
LOGIC DIAGRAMS (continued)

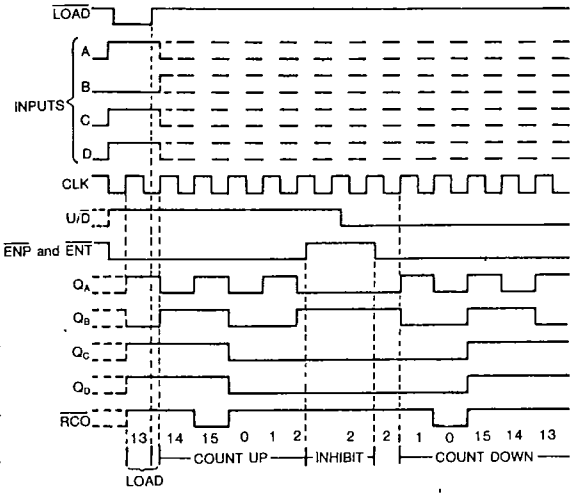




Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight and seven

'169



Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

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FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CLK	U/$\overline{D}$	$\overline{ENP}$	$\overline{ENT}$	$\overline{LOAD}$	D_n	Q_n	$\overline{RCO}$
Parallel Load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H=HIGH voltage level steady state
h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L=LOW voltage level steady state
l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X=Don't care
q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑=LOW-to-HIGH clock transition

NOTE:

1. The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.
   The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

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Synchronous 4-Bit Up/Down Decade and Binary Counters

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DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT168, AHCT169

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Maximum Operating Frequency		f_{max}	C_L=50pF	50	30		25		MHz
Propagation Delay, CLK to $\overline{RCO}$		t_{PLH}		19		28		32	ns
		t_{PHL}		19		28		32	
Propagation Delay, CLK to Any Q		t_{PLH}		12		18		22	ns
		t_{PHL}		12		18		22	
Propagation Delay, $\overline{ENT}$ to $\overline{RCO}$		t_{PLH}		10		16		19	ns
		t_{PHL}		10		16		19	
Propagation Delay, U/$\overline{D}$ to $\overline{RCO}$		t_{PLH}		14		23		25	ns
		t_{PHL}		14		23		25	
Pulse Duration, CLK high or low		t_w		10	16		20		ns
Setup Time, Before CLK↑	A, B, C or D			9	15		20		ns
	$\overline{ENP}$ or $\overline{ENT}$			12	20		25		
	$\overline{LOAD}$			9	15		20		
	U/$\overline{D}$			9	15		20		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

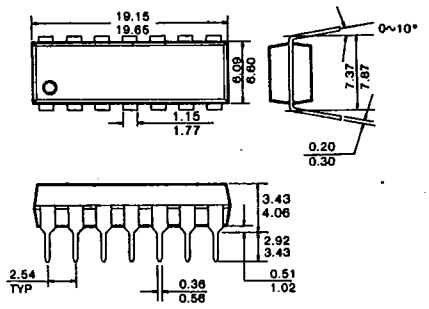
* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

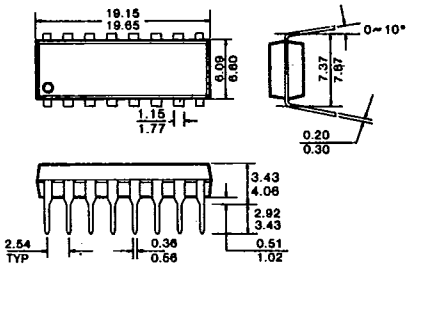
T-90-20

1. PLASTIC PACKAGES

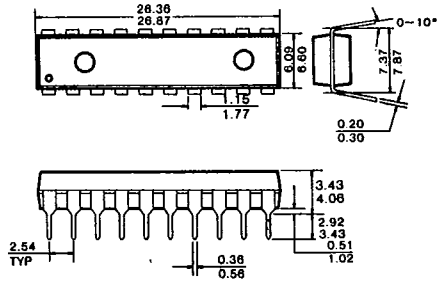
14-Pin Plastic DIP **Units: mm**



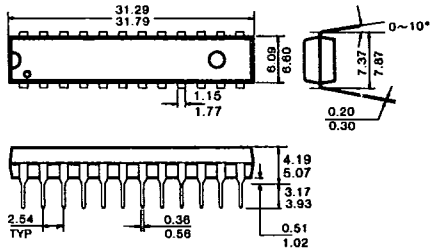
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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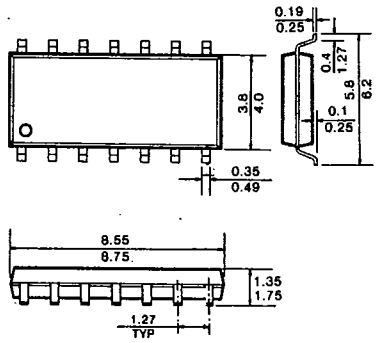
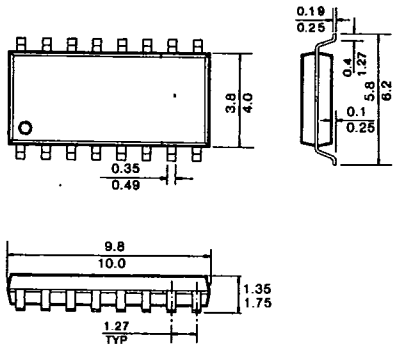
14-Pin SOP

Unit: mm



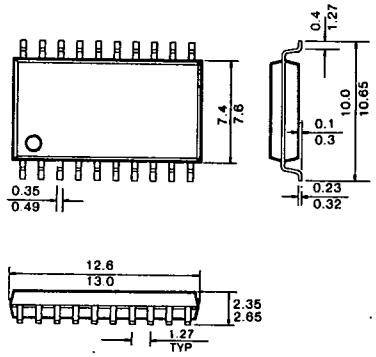
16-Pin SOP

Unit: mm



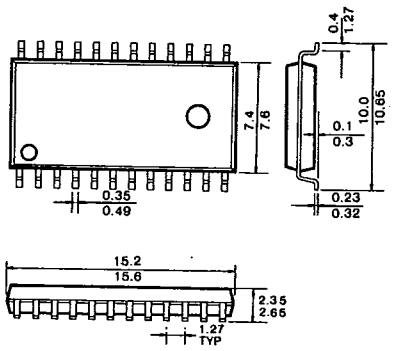
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

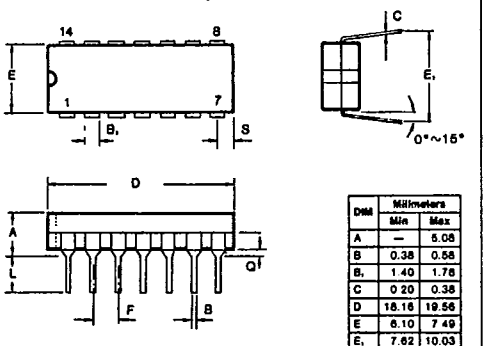


PACKAGE DIMENSIONS

T-90-20

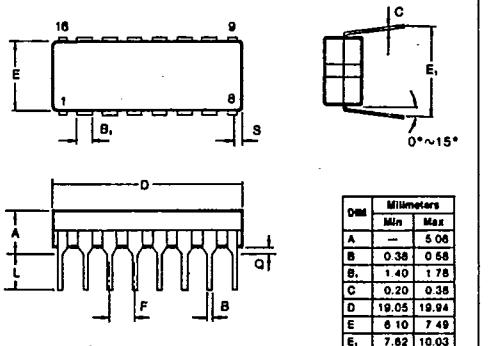
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



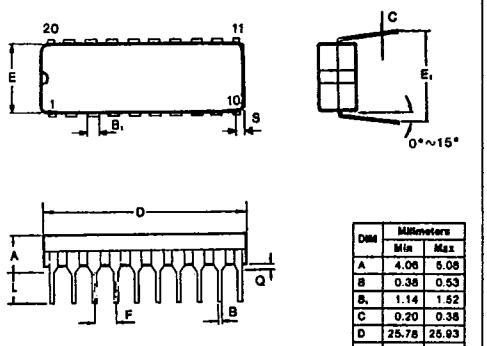
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



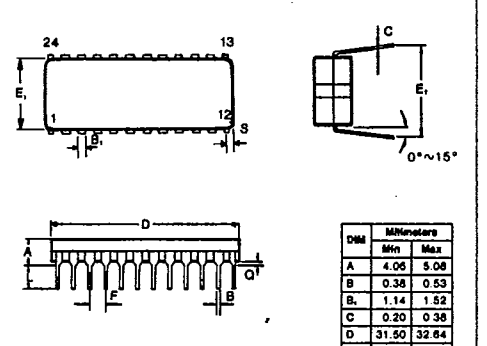
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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