

KS54AHCT
KS74AHCT **155**

Dual 2-to-4 Line Decoders/Demultiplexers

T-67-21-55

FEATURES

- Typical applications:
Dual 2-to-4 line decoder
Dual 1-to-4 line demultiplexer
3-to-8 line decoder
1-to-8 line demultiplexer
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA}$ @ $V_{OL} = 0.5 \text{ V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^{\circ}\text{C}$
KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

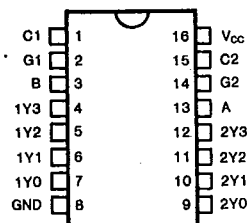
DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

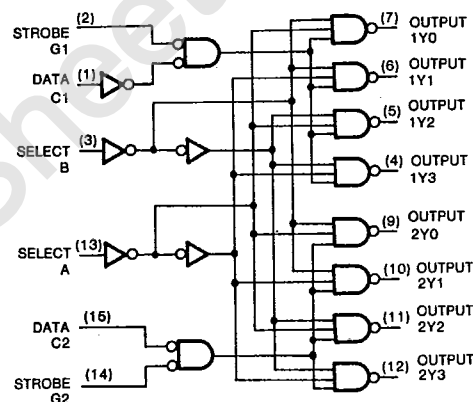
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



SAMSUNG SEMICONDUCTOR

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FUNCTION TABLES

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

Inputs				Outputs			
Select	Strobe	Data					
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

Inputs		Outputs							
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
ICB A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H	H	H	H	H	H	H	H	H
L L L	L	L	H	H	H	H	H	H	H
L L H	L	H	L	H	H	H	H	H	H
L H L	L	H	H	L	H	H	H	H	H
L H H	L	H	H	H	L	H	H	H	H
H L L	L	H	H	H	H	L	H	H	H
H L H	L	H	H	H	H	H	L	H	H
H H L	L	H	H	H	H	H	H	L	H
H H H	L	H	H	H	H	H	H	H	L

IC = Inputs C1 and C2 connected together

IG = Inputs G1 and G2 connected together

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V to +7VDC Input Diode Current, I_{IK} $(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ± 20 mADC Output Diode Current, I_{OK} $(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ± 20 mAContinuous Output Current Per Pin, I_O $(-0.5V < V_O < V_{CC} + 0.5V)$ ± 35 mA

Continuous Current Through

 V_{CC} or GND pins ± 125 mAStorage Temperature Range, T_{stg} -65°C to +150°CPower Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5VDC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}

Operating Temperature

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



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DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		T _a = -40°C to +85°C	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC} 4.2	V _{CC} - 0.1 3.98	V _{CC} - 0.1 3.84	V _{CC} - 0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI _{CC}	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

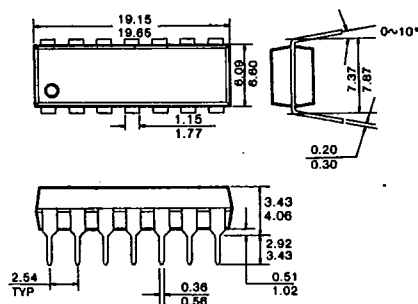
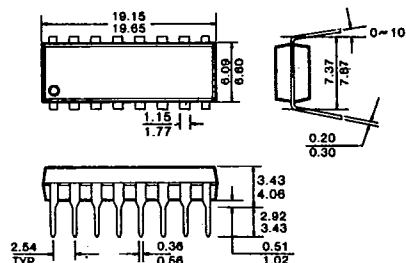
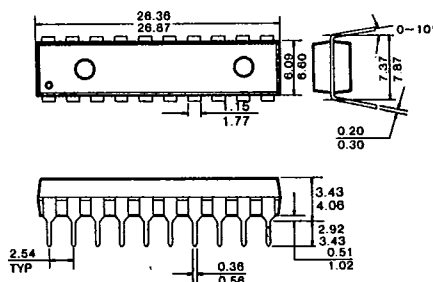
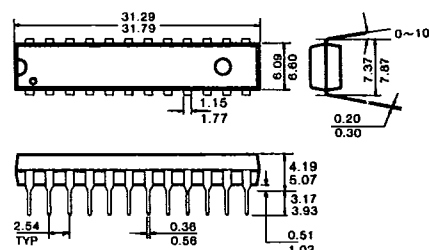
AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2\text{ ns}$, AHCT155)

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	t_{PLH}	$C_L = 50\text{pF}$	12		20		24	ns
	t_{PHL}		12		20		24	
Maximum Propagation Delay, A or B to any Y (3 levels of logic)	t_{PLH}		14		23		28	ns
	t_{PHL}		14		23		28	
Maximum Propagation Delay, C1 to any Y	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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**SAMSUNG SEMICONDUCTOR**

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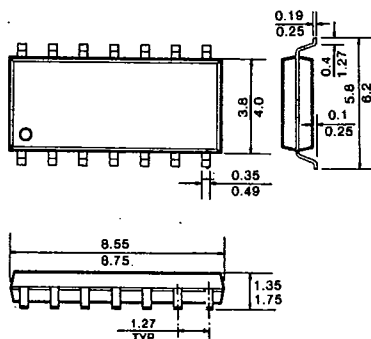
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PACKAGE DIMENSIONS

T-90-20

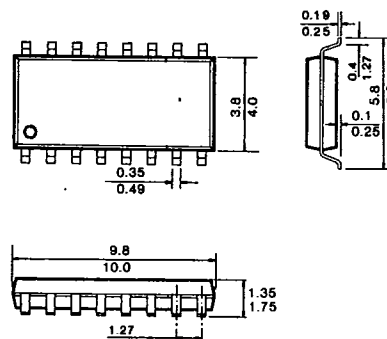
14-Pin SOP

Unit: mm



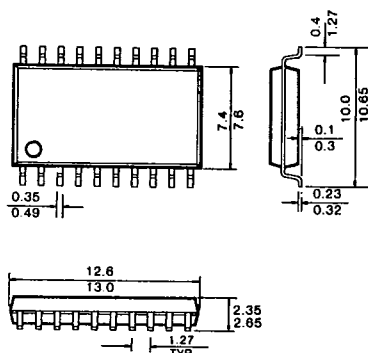
16-Pin SOP

Unit: mm



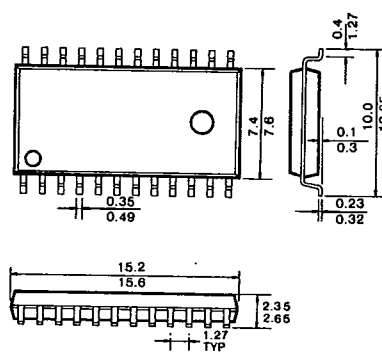
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm



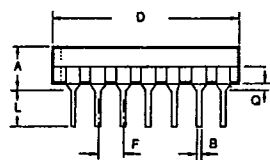
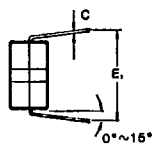
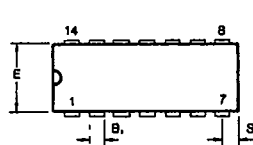
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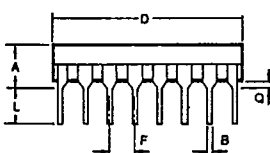
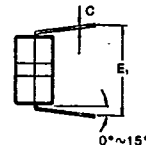
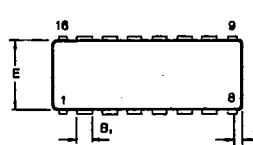
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PACKAGE DIMENSIONS

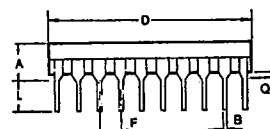
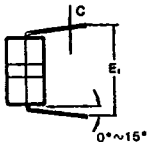
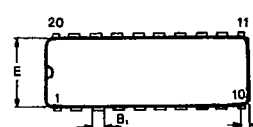
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2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

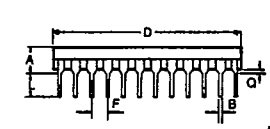
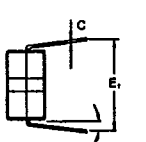
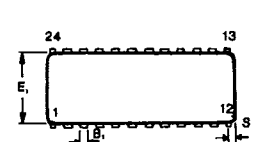
Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93

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