

Keyboard Encoder Read Only Memory

FEATURES

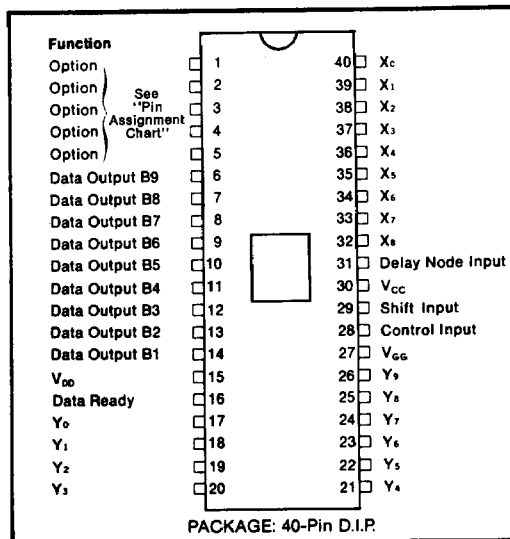
- Data output directly compatible with TTL
- N Key rollover or lockout operation
- Quad mode
- Lockout/rollover selection externally selected as option
- On chip-master/slave oscillator
- All 10 output bits available
- Fully buffered data outputs
- Output enable provided as option
- Data complement provided as option
- Pulse or level data ready output signal provided as an option
- Any key down output provided as an option
- Contact bounce circuit provided to eliminate contact bounce
- Static charge protection on all input/outputs
- Pin for Pin replacement for GI AY-5-3600

GENERAL DESCRIPTION

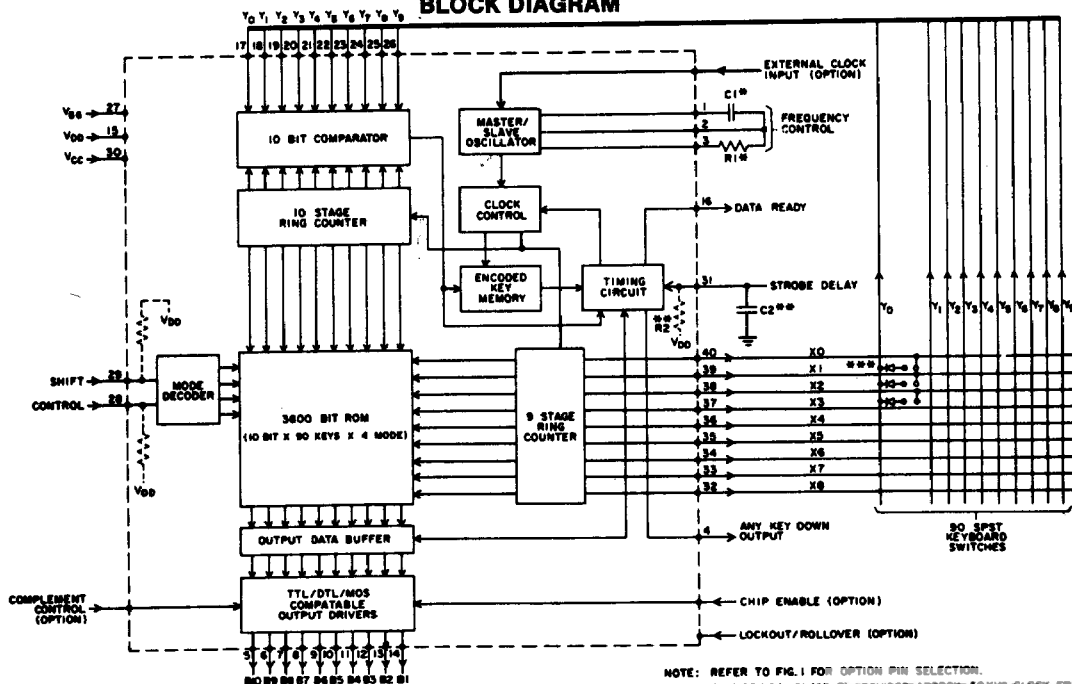
The SMC Microsystems KR3600-XX is a Keyboard Encoder containing a 3600 bit read only memory and all the logic necessary to encode single pole single throw keyboard closures into a 10 bit code.

The KR3600-XX is fabricated with a low voltage p channel technology and contains the equivalent of 5000 transistors on a monolithic chip in a 40 lead dip ceramic package.

PIN CONFIGURATION



BLOCK DIAGRAM



NOTE: REFER TO FIG. 1 FOR OPTION PIN SELECTION.

*R1 (100KΩ), C1 (45pF) PROVIDES APPROXIMATELY 400ns DELAY.
**C2 (300ns DELAY/CP1) PROVIDES APPROXIMATELY 400ns DELAY.
***DIODES NECESSARY FOR COMPLETE N KEY ROLLOVER OPERATION.

DESCRIPTION OF OPERATION

The KR3600 contains a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby conditions, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y0-Y9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER — When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT — When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

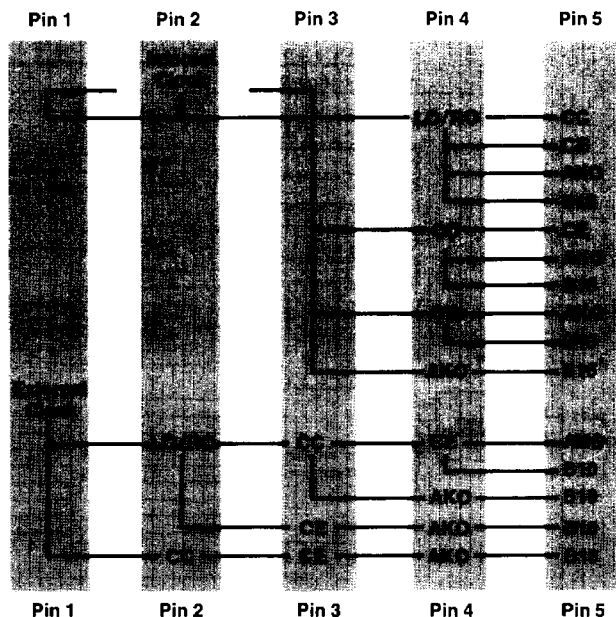
SPECIAL PATTERNS — Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the KR3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes.

CUSTOM CODING INFORMATION

The custom coding information for SMC's 3600 Bit Keyboard Encoder ROM should be transmitted to SMC. The Truth Table should be completed on the format supplied.

LEGEND

CC = Complement Control
 AKO = Any Key Down Output
 B10 = B10 (Data) Output
 LO/RO = Lockout/Rollover
 CE = Chip Enable
 Internal Clock = Self Contained Oscillator
 External Clock = External Frequency Source



OPTION SELECTION/PIN ASSIGNMENT

FIGURE 1

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	-25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

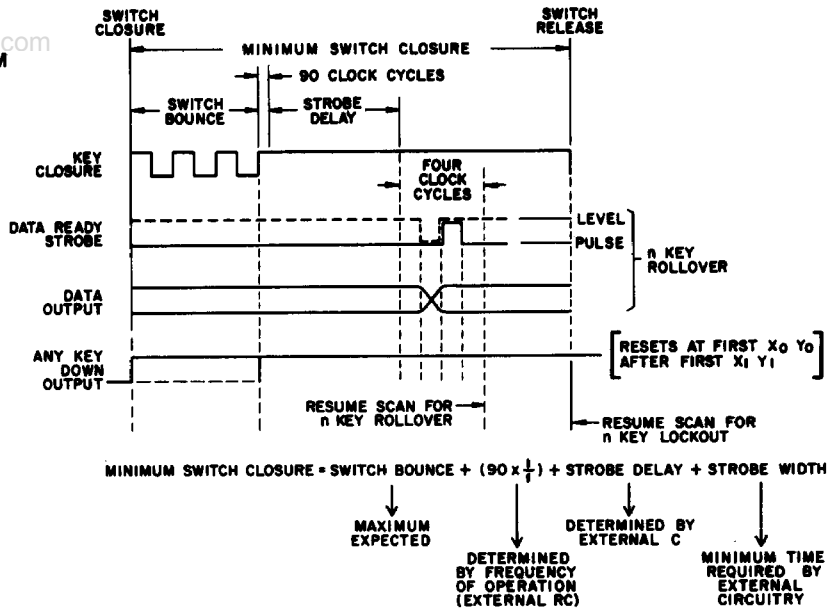
($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 5\%$, $V_{GG} = -12\text{V} \pm 1.0\text{V}$, $V_{DD} = \text{GND}$, unless otherwise noted)

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Frequency	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width	7	—	—	μs	
Data & Clock Input (Shift, Control, Compliment Control, Lockout/Rollover, Chip Enable & External Clock)					
Logic "0" Level	V_{GG}	—	+0.8	V	
Logic "1" Level	$V_{CC}-1.5$	—	$V_{CC}+0.3$	V	
Shift & Control Input Current	75	150	220	μA	$V_{IN} = +5\text{V}$
X Output (X_0-X_9)					
Logic "1" Output Current	40 600 900 1500 3000	250 1300 2000 2000 10,000	500 4000 6500 14,000 23,000	μA μA μA μA μA	$V_{OYT} = V_{CC}$ (See Note 2) $V_{OUT} = V_{CC}-1.3\text{V}$ $V_{OUT} = V_{CC}-2.0\text{V}$ $V_{OUT} = V_{CC}-5\text{V}$ $V_{OUT} = V_{CC}-10\text{V}$
Logic "0" Output Current	8 6 5 2 —	30 25 20 10 0.5	60 50 45 30 5	μA μA μA μA μA	$V_{OUT} = V_{CC}$ $V_{OUT} = V_{CC}-1.3\text{V}$ $V_{OUT} = V_{CC}-2.0\text{V}$ $V_{OUT} = V_{CC}-5\text{V}$ $V_{OUT} = V_{CC}-10\text{V}$
Y Input (Y_0-Y_9)					
Trip Level	$V_{CC}-5$	$V_{CC}-3$	$V_{CC}-2$	V	Y Input Going Positive (See Note 2)
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	18 14 13 5	100 80 50 40	170 150 130 110	μA μA μA μA	$V_{IN} = V_{CC}$ $V_{IN} = V_{CC}-1.3\text{V}$ $V_{IN} = V_{CC}-2.0\text{V}$ $V_{IN} = V_{CC}-4.0\text{V}$
Unselected Y Input Current	9 7 6 3 —	40 30 25 15 0.5	80 70 60 40 20	μA μA μA μA μA	$V_{IN} = V_{CC}$ $V_{IN} = V_{CC}-1.3\text{V}$ $V_{IN} = V_{CC}-2.0\text{V}$ $V_{IN} = V_{CC}-5\text{V}$ $V_{IN} = V_{CC}-10\text{V}$
Input Capacitance	—	3	10	pF	at 0V (All Inputs)
Switch Characteristics					
Minimum Switch Closure	—	—	—	—	See Timing Diagram
Contact Closure Resistance	—	—	300	Ω	Z_{CC}
	1×10^7	—	—	Ω	Z_{CO}
Strobe Delay					
Trip Level (Pin 31)	$V_{CC}-4$	$V_{CC}-3$	$V_{CC}-2$	V	
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)	-3	-5	-9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready					
Logic "0"	—	—	0.4	V	$I_{OL} = 1.6\text{mA}$
Logic "1"	$V_{CC}-1$ $V_{CC}-2$	— —	— —	V V	$I_{OH} = 1.0\text{mA}$ $I_{OH} = 2.2\text{mA}$
Power					
I_{CC}	—	12	25	mA	$V_{CC} = +5\text{V}$
I_{GG}	—	12	25	mA	$V_{GG} = -12\text{V}$

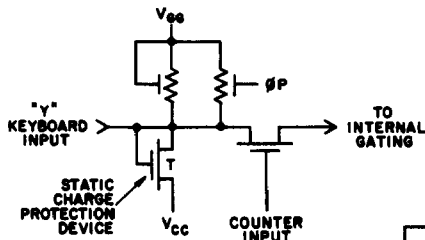
**Typical values are at $+25^\circ\text{C}$ and nominal voltages.

NOTE

1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

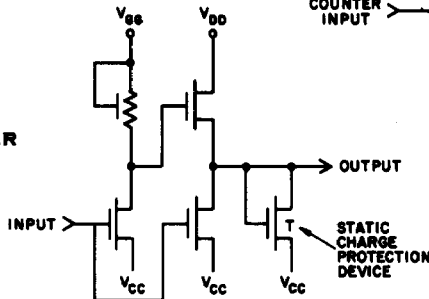


"Y" INPUT STAGE FROM KEYBOARD

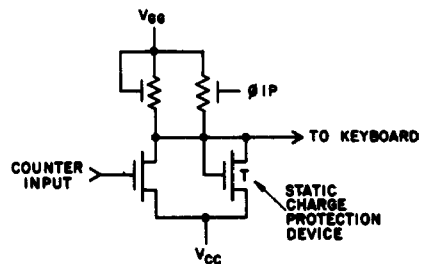


OUTPUT DRIVER

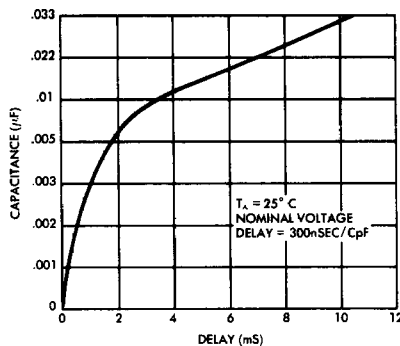
NOTE: Output driver capable of driving one TTL load with no external resistor. Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}



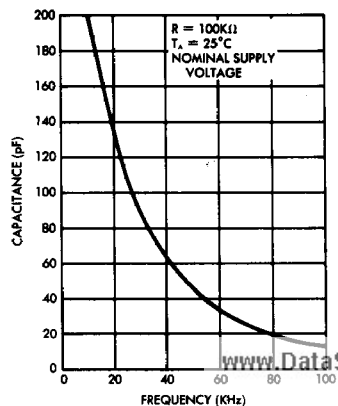
"X" OUTPUT STAGE TO KEYBOARD



STROBE DELAY vs. C₂



OSCILLATOR FREQUENCY vs. C₁



KR3600-STD

XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	1 1000111001	< 0011111001	1 1000111011	SUB 0101100001
01	q 1000110101	Q 1000110101	Q 1000111111	DLE 0000100001
02	a 1000010101	A 1000000101	a 1000011111	@ 0000000101
03	Z 0101110101	Z 0101100101	Z 0101111111	P 0000100101
04	HT 1001000001	HT 1001000001	HT 1001000001	I 1001000101
05	H 0001000010	H 0001000010	H 0001000010	H 0001000111
06	+ 1101011001	+ 1101011001	+ 1101011001	+ 1101011011
07	SO 0111000001	> 0111111001	SO 0111000001	SO 0111000011
08	p 0000110101	@ 0000000101	SOH 1000000001	NUL 0000000001
09	1 1000111001	! 1000111001	2 0100111011	SOH 1000000001
10	2 0100111001	@ 0000000101	w 1101011111	ETB 1110100001
11	w 1101010101	W 1101010101	s 1100111111	A 0011100101
12	s 1100110101	S 1100100101	x 0001111111	A 1000000101
13	x 0001110101	X 0001001010	RS 0111100001	Q 1000100101
14	RS 0111100001	RS 0111100001	% 1010011001	FS 0011100001
15	% 1010011001	% 1010011001	CR 1011000001	% 1010011011
16	m 1011010101	J 1011001010	SI 1111000001	CR 1011000001
17	SI 1111000001	SI 1111000001	SO 0111000001	SI 1111000011
18	n 0111010101	A 0111001010	STX 0100000001	SO 0111000001
19	2 0100111001	" 0100011001	e 1010011111	STX 0100000001
20	3 1100111001	# 1100011001	d 0010011111	NAK 1010100001
21	e 1010010101	E 1010000010	o 1000111111	DC3 1100100001
22	d 0010010101	D 0010000101	— 1111100100	B 0100000101
23	C 1100010101	C 1100000101	\$ 0010011011	R 0100100101
24	— 1111100100	— 1111100100	L 0011000010	A 0111100100
25	\$ 0010011001	\$ 0010011001	US 1111100001	\$ 0010011011
26	L 0011000010	L 0011000010	ACK 0110000001	L 0011000111
27	US 1111100001	US 1111100001	DEL 1111111101	US 1111100011
28	6 0110111001	& 0110011001	4 0010111011	ACK 0110000001
29	k 1101010101	I 1101100101	f 0100111111	DEL 1111111101
30	4 0010111001	\$ 0010011001	f 0100111111	DC4 0010100001
31	r 0100110101	R 0100100101	SP 0000011000	ENQ 1010000001
32	f 0110001010	F 0110000101	CAN 0001101000	C 1100000101
33	SP 0000011000	SP 0000011000	CR 1011000001	SP 0000011000
34	CAN 0001101000	(0001011000	VT 1101000000	BS 0001000000
35	CR 1011000001	CR 1011000001	BEL 1110000001	M 1011000101
36	I 1101111101	I 1101111101	" 0100011001	K 1101000101
37	VT 1101000000	VT 1101000000	5 1010111011	VT 1101000010
38	7 1110111001	" 1110011001	T 0010111111	BEL 1110000001
39	" 0100011001	" 0100011001	G 1110011111	" 0100011011
40	5 1010111001	% 1010011001	v 0110111111	STX 0100000001
41	t 0010110101	T 0010100101	ETX 1100000001	EOT 0010000001
42	g 1110000101	g 1110000101	? 1111111001	D 0010000101
43	v 0110110101	V 0110100101	— 1011111001	S 1100100101
44	ETX 1100000001	ETX 1100000001	) 1001011001	ETX 1100000001
45	I 1011111101	I 1011111101	> 0111111001	N 0111000101
46	? 1111111001	? 1111111001	Y 1001100101	[1101100101
47	— 1011011001	— 1011111001	b 0100000101	— 1011011011
48	) 1001011001	) 1001011001	h 0001011111	) 1001011011
49	SP 0000011001	SP 0000011001	> 0111111001	SP 0000011011
50	6 0110111001	> 0111111001	* 0101011001	SOH 1000000001
51	y 1001110101	Y 1001100101	! 1000011001	DC1 1000100001
52	h 0001010101	H 0001000101	7 1110111011	E 1010000101
53	b 0100010101	B 0100000101	u 1010111111	T 0010100101
54	> 0101111001	> 0101011001	j 0101011111	SYN 0110100001
55	> 0111111001	> 0111111001	n 0111011111	Z 0101100101
56	* 1101111001	* 1101011001	= 1011111010	Y 1001100101
57	NUL 0000000001	NUL 0000000001	< 0011111011	NUL 0000000001
58	* 0101011001	* 0101011001	p 0000110101	* 0101011011
59	! 1000011001	! 1000011001	o 0000110101	! 1000011011
60	7 1110111011	& 0110011001	# 1100011001	ETX 1100000001
61	u 1010101010	U 1010100101	* 0101011001	BEL 1110000001
62	j 0101010101	J 0101000101	8 0001111011	F 0110000101
63	n 0111010101	N 0111000101	i 1001011111	U 1010100101
64	= 1011111000	= 1011111000	m 1011011111	— 0111111100
65	< 0011111001	< 0011111001	/ 1111011001	W 1110100101
66	p 0000110101	P 0000110101	" 1100011001	J 0101000101
67	o 0000110101	) 1001011001	0 0000111001	DC2 0100100001
68	& 0110011001	& 0110011001	1 1000111001	& 0110011011
69	# 1100011001	# 1100011001	2 0100111011	# 1100011011
70	8 0001111001	* 0101011001	3 1100111001	ESC 1101100001
71	i 1001010101	I 1001000101	4 0001111011	ACK 0110000001
72	k 1101010101	K 1101000101	5 1010111111	G 1110000101
73	m 1011010101	M 1011000101	6 0110111111	V 1010100101
74	/ 1111011001	? 1111111001	7 1110111011	" 1110011001
75	" 1110011001	" 0100011001	8 0001111011	" 0100011001
76	LF 0101000000	LF 0101000000	9 1001111011	GS 1011100000
77	= 1011111001	+ 1101011001	0 0000111001	+ 1101011001
78	FF 0011000101	< 0011111001	1 1001111011	FF 0011000011
79	(0001011001	(0001011001	2 0100111011	0001011011
80	9 1001111011	(0001011001	3 1100111011	EM 1001100001
81	o 1111010101	O 1111000101	4 0001111011	I 1011000101
82	i 1001010101	L 0011000101	5 1010111111	X 0001100101
83	. 0011011001	. 0011011001	6 0110111111	. 0011011011
84	. 0111011001	. 0111011001	7 1110111111	. 0111011011
85	. 1101111001	. 0101111001	8 0001111011	. 0101111001
86	] 1011100101	] 1101100101	9 1001111011	[1101100101
87	- 1011011001	- 1111100101	0 0000111001	- 1111100101
88	0 0000111001	0 0000111001	1 1001000001	0 0000111001
89	9 1001111001	] 1001011001		HT 1001000001

Options:

Internal oscillator (pins 1, 2, 3)

Any key down (pin 4) positive output

N key rollover only

Pulse data ready signal

Internal resistor to VDD on shift and control pins

KR3600-STD outputs provides ASCII bits 1-6 on B1-B6, and bit 7 on B8

KR 3600-ST

XY	Normal B-123456789	Shift B-123456789	Control B-123456789	Shift/Control B-123456789
00	\ 000001101	~ 011111101	NUL 000000001	RS 011110001
01	= 101111010	+ 110101001	GS 101110001	VT 110100010
02	DC3 110010010	DC3 110010010	DC3 110010010	DC3 110010010
03	- 101101001	- 111101011	CR 101100010	US 111100010
04	BS 000100010	BS 000100010	BS 000100010	BS 000100010
05	0 000011001	0 000011001	0 000011001	0 000011001
06	• 011101001	• 011101001	• 011101001	• 011101001
07	000000000	000000000	000000000	000000000
08	000000000	000000000	000000000	000000000
09	000000000	000000000	000000000	000000000
10	/ 111101010	? 111111001	ST 111100001	US 111100010
11	• 011101001	> 011111010	SO 011100010	RS 011100010
12	? 001101010	< 001111001	FF 001100001	FS 001100010
13	m 101101110	M 101100101	CR 101100010	CR 101100010
14	n 101101110	N 011100101	SO 011100010	SO 011100010
15	b 010001110	B 010001001	STX 010000010	STX 010000010
16	v 010111101	V 011011010	SYN 011010010	SYN 011010010
17	x 100001101	C 110000110	ETX 110000001	ETX 110000001
18	x 000111101	X 000101010	CAN 000110001	CAN 000110001
19	Z 010111110	Z 010101010	SUB 010110010	SUB 010110010
20	LF 010100001	LF 010100001	LF 010100001	LF 010100001
21	\ 001110101	: 001111110	FS 001110010	FS 001110010
22	DEL 111111110	DEL 111111110	DEL 111111110	DEL 111111110
23	] 110110110	] 101110110	ESC 110110001	GS 101110001
24	7 110110101	7 110110101	7 110110101	7 110110101
25	8 000111010	8 000111010	8 000111010	8 000111010
26	9 100111001	9 100111001	9 100111001	9 100111001
27	000000000	000000000	000000000	000000000
28	000000000	000000000	000000000	000000000
29	000000000	000000000	000000000	000000000
30	: 110111010	: 010111001	ESC 110110001	SUB 010110010
31	: 001101101	L 001100110	FF 001100001	FF 001100001
32	k 110101110	K 110100101	VT 110100010	VT 110100010
33	j 010101101	J 010100110	LF 010100001	LF 010100001
34	n 000101110	H 000100101	BS 000100010	BS 000100010
35	g 111001110	G 111000101	BEL 111000010	BEL 111000010
36	f 011001101	F 011000110	ACK 011000001	ACK 011000001
37	d 001001110	D 001000101	EOT 001000010	EOT 001000010
38	s 110011110	S 110010101	DC3 110010010	DC3 110010010
39	a 100001110	A 100000101	SOH 100000010	SOH 100000010
40	000000000	000000000	000000000	000000000
41	: 110111101	: 101111001	ESC 110110001	GS 101110001
42	GR 101100010	GR 101100010	GR 101100010	GR 101100010
43	" 111001001	" 010001001	BEL 111000010	STX 010000010
44	4 001011010	4 001011010	4 001011010	4 001011010
45	5 101011001	5 101011001	5 101011001	5 101011001
46	6 011011001	6 011011001	6 011011001	6 011011001
47	000000000	000000000	000000000	000000000
48	000000000	000000000	000000000	000000000
49	000000000	000000000	000000000	000000000
50	p 000011110	P 000010101	DEL 000010010	DEL 000010010
51	o 111101101	O 111100110	SI 111100001	SI 111100001
52	i 100101101	I 100100110	HT 100100001	HT 100100001
53	u 101011110	U 101010101	NAK 101010010	NAK 101010010
54	y 100111110	Y 100110101	EM 100110010	EM 100110010
55	t 001011101	T 001010110	DC4 001010010	DC4 001010010
56	r 010011101	R 010010110	DC2 010010001	DC2 010010001
57	e 101001101	E 101000110	ENQ 101000001	ENQ 101000001
58	w 111011101	W 111010110	ETB 111010001	ETB 111010001
59	q 100011101	Q 100010110	DC1 100010001	DC1 100010001
60	000000000	000000000	000000000	000000000
61	000000000	000000000	000000000	000000000
62	DC2 010010001	DC2 010010001	DC2 010010001	DC2 010010001
63	000000000	000000000	000000000	000000000
64	1 100011010	1 100011010	1 100011010	1 100011010
65	2 010011010	2 010011010	2 010011010	2 010011010
66	3 110011001	3 110011001	3 110011001	3 110011001
67	000000000	000000000	000000000	000000000
68	000000000	000000000	000000000	000000000
69	000000000	000000000	000000000	000000000
70	0 000011001	) 100101010	DLE 000100101	HT 100100001
71	9 100111001	(000101001	EM 100110010	BS 000100010
72	8 000111010	- 010101010	CAN 000110001	LF 010100001
73	7 111011010	& 011001010	ETB 111010001	ACK 011000001
74	6 011011001	^ 011110110	SYN 011010010	RS 011110001
75	5 101011001	% 101001010	NAK 101010010	ENQ 101000001
76	4 001011010	\$ 001001001	DC4 001010001	EOT 001000010
77	3 110011001	# 110001010	DC3 110010010	ETX 110000001
78	2 010011010	@ 000001010	DC2 010010001	NUL 000000010
79	1 100011010	! 100001001	DC1 100010001	SOH 110000010
80	000000000	000000000	000000000	000000000
81	000000000	000000000	000000000	000000000
82	000000000	000000000	000000000	000000000
83	000000000	000000000	000000000	000000000
84	000000000	000000000	000000000	000000000
85	SP 000001010	SP 000001010	NUL 000000001	NUL 000000001
86	000000000	000000000	000000000	000000000
87	DC1 100010001	DC1 100010001	DC1 100010001	DC1 100010001
88	HT 100100001	HT 100100001	HT 100100001	HT 100100001
89	ESC 110110001	ESC 110110001	ESC 110110001	ESC 110110001

Options: Pin 1, 2, 3—Internal oscillator
Pin 4—Lockout (logic 1), rollover (logic 0)
Pin 5—Any key down output

All outputs complemented
Level data ready

KR 3600-PRO

XY	Normal	Shift	Control	Shift/Control
00	00000000	00100000	01000000	01100000
01	00000001	00100001	01000001	01100001
02	00000010	00100010	01000010	01100010
03	00000011	00100011	01000011	01100011
04	00000100	00100100	01000100	01100100
05	00000101	00100101	01000101	01100101
06	00000110	00100110	01000110	01100110
07	00000111	00100111	01000111	01100111
08	00001000	00101000	01001000	01101000
09	00001001	00101001	01001001	01101001
10	00001010	00101010	01001010	01101010
11	00001011	00101011	01001011	01101011
12	00001100	00101100	01001100	01101100
13	00001101	00101101	01001101	01101101
14	00001110	00101110	01001110	01101110
15	00001111	00101111	01001111	01101111
16	00010000	00101000	01001000	01101000
17	00010001	00101001	01001001	01101001
18	00010010	00101010	01001010	01101010
19	00010011	00101011	01001011	01101011
20	00010100	00101100	01001100	01101100
21	00010101	00101101	01001101	01101101
22	00010110	00101110	01001110	01101110
23	00010111	00101111	01001111	01101111
24	00011000	00101000	01001000	01101000
25	00011001	00101001	01001001	01101001
26	00011010	00101010	01001010	01101010
27	00011011	00101011	01001011	01101011
28	00011100	00101100	01001100	01101100
29	00011101	00101101	01001101	01101101
30	00011110	00101110	01001110	01101110
31	00011111	00101111	01001111	01101111
32	00010000	00100000	01010000	01110000
33	00010001	00100001	01010001	01110001
34	00010010	00100010	01010010	01110010
35	00010011	00100011	01010011	01110011
36	00010100	00100100	01010100	01110100
37	00010101	00100101	01010101	01110101
38	00010110	00100110	01010110	01110110
39	00010111	00100111	01010111	01110111
40	00011000	00101000	01011000	01111000
41	00011001	00101001	01011001	01111001
42	00011010	00101010	01011010	01111010
43	00011011	00101011	01011011	01111011
44	00011100	00101100	01011100	01111100
45	00011101	00101101	01011101	01111101
46	00011110	00101110	01011110	01111110
47	00011111	00101111	01011111	01111111
48	00011000	00110000	01011000	01111000
49	00011001	00110001	01011001	01111001
50	00011010	00110010	01011010	01111010
51	00011011	00110011	01011011	01111011
52	00011100	00110100	01011100	01111100
53	00011101	00110101	01011101	01111101
54	00011110	00110110	01011110	01111110
55	00011111	00110111	01011111	01111111
56	00011000	00111000	01011000	01111000
57	00011001	00111001	01011001	01111001
58	00011010	00111010	01011010	01111010
59	00011011	00111011	01011011	01111011
60	00011100	00111100	01011100	01111100
61	00011101	00111101	01011101	01111101
62	00011110	00111110	01011110	01111110
63	00011111	00111111	01011111	01111111
64	10000000	10100000	11000000	11100000
65	10000001	10100001	11000001	11100001
66	10000010	10100010	11000010	11100010
67	10000011	10100011	11000011	11100011
68	10000100	10100100	11000100	11100100
69	10000101	10100101	11000101	11100101
70	10000110	10100110	11000110	11100110
71	10000111	10100111	11000111	11100111
72	10001000	10100100	11000100	11100100
73	10001001	10100101	11000101	11100101
74	10001010	10100110	11000110	11100110
75	10001011	10100111	11000111	11100111
76	10001100	10100100	11000100	11100100
77	10001101	10100101	11000101	11100101
78	10001110	10100110	11000110	11100110
79	10001111	10100111	11000111	11100111
80	10001000	10101000	11001000	11101000
81	10001001	10101001	11001001	11101001
82	10001010	10101010	11001010	11101010
83	10001011	10101011	11001011	11101011
84	10001100	10101100	11001100	11101100
85	10001101	10101101	11001101	11101101
86	10001110	10101110	11001110	11101110
87	10001111	10101111	11001111	11101111
88	10001000	10101000	11001000	11101000
89	10001001	10101001	11001001	11101001

Options:
Internal oscillator (pins 1, 2, 3)
Lockout/rollover (pin 4), with internal resistor to VDD
Lockout is logic 1

Any key down (pin 5), positive output
Pulse data ready
Internal resistor to VDD on shift & control pins

DESCRIPTION

The KR 3600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR 3600 parts, the KR 3600 PRO contains all of the logic to de-bounce and encode keyswitch closures, while providing either a 2-key or N-key rollover.

The output of the KR 3600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR 3600 is shown in Table I. The format is simple: output bits, 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256x8 PROM, and Figure 2 a full 90 key, 4 mode application, utilizing a 512x8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

