STANDARD MICROSYSTEMS CORPORATION

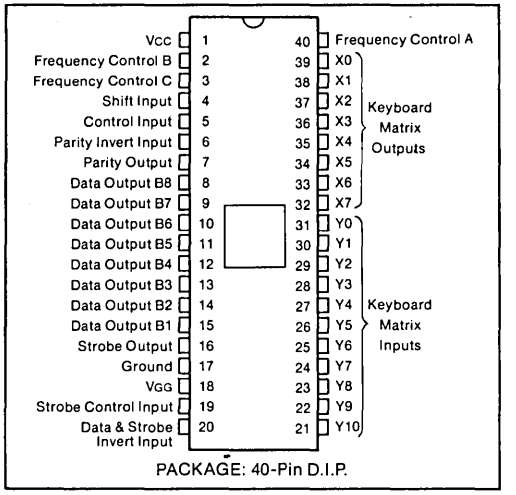
KR2376-XX

Keyboard Encoder Read Only Memory

FEATURES

- ☐ Outputs directly compatible with TTL/DTL or MOS logic arrays.
- ☐ External control provided for output polarity selection.
- ☐ External control provided for selection of odd or even parity.
- ☐ Two key roll-over operation.
- ☐ N-key lockout.
- ☐ Programmable coding with a single mask change.
- ☐ Self-contained oscillator circuit.
- ☐ Externally controlled delay network provided to eliminate the effect of contact bounce.
- ☐ One integrated circuit required for complete keyboard assembly.
- ☐ Static charge protection on all input and output terminals.
- ☐ Entire circuit protected by a layer of glass passivation.

PIN CONFIGURATION



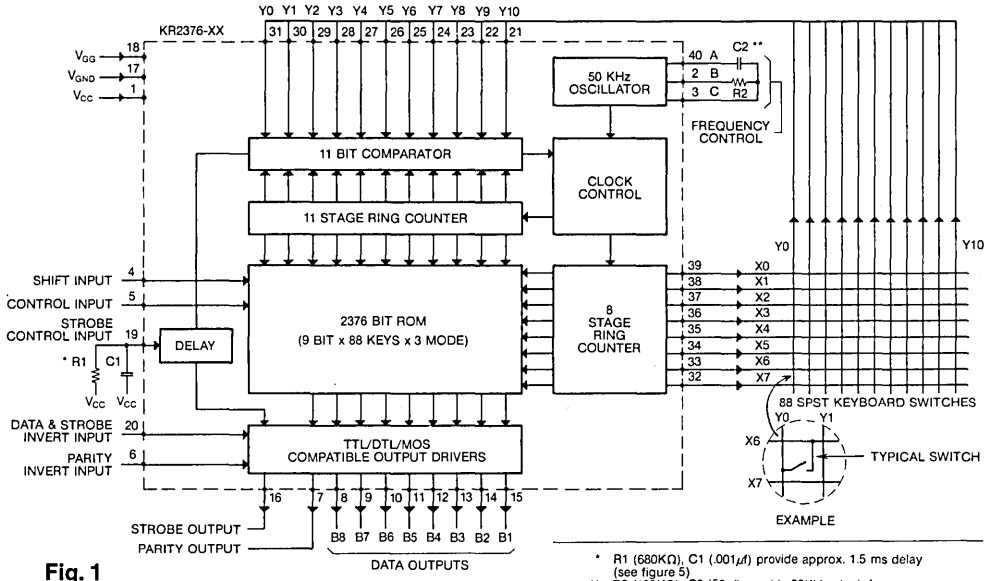
PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC KR2376-XX is a 2376-bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The KR2376-XX is fabricated with low threshold, P-channel technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip, available in a 40 pin dual-in-line package.

TYPICAL CONNECTION OF KR2376-XX



* R1 (680KΩ), C1 (.001μf) provide approx. 1.5 ms delay (see figure 5)

** R2 (100KΩ), C2 (50pf) provide 50KHz clock frequency (see figure 6)

Fig. 1

MAXIMUM GUARANTEED RATINGS†

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −65° C to +150° C
GND and V_{GG}, with respect to V_{CC} ..... −20V to +0.3V
Logic Input Voltages, with respect to V_{CC} ..... −20V to +0.3V

† Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0° C to +70° C, V_{CC} = +5V ±0.5V, V_{GG} = −12V ±1.0V, unless otherwise noted)

Characteristics	Min	Typ	Max	Unit	Conditions
CLOCK	20	50	100	KHz	see fig.1 footnote (**) for typical R-C values
DATA INPUT					
Logic "0" Level			+0.8	V	
Logic "1" Level	V_{CC}-1.5			V	
Input Capacitance			10	pf	
INPUT CURRENT					
*Control, Shift & Y0 thru Y10	10	100	140	μA	V_{IN} = +5.0V
*Control, Shift & Y0 thru Y10	5	30	50	μA	V_{IN} = Ground
Data Invert, Parity Invert		.01	1	μA	V_{IN} = −5.0V to +5.0V
DATA OUTPUT & X OUTPUT					
Logic "0" Level			+0.4	V	I_{OL} = 1.6mA (see fig. 7)
Logic "1" Level	V_{CC}-1.0			V	I_{OH} = 100 μA
POWER CONSUMPTION		140	200	mW	Nom. Power Supp. Voltages (see fig. 8)
SWITCH CHARACTERISTICS					
Minimum Switch Closure	see timing diagram-fig. 2				
Contact Closure Resistance between X1 and Y1			300	Ohm	
Contact Open Resistance between X1 and Y1	1×10^7			Ohm	

*Inputs with Internal Resistor to V_{GG}

DESCRIPTION OF OPERATION

The KR2376-XX contains (see Fig. 1), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9-bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the KR2376-XX ROM covering most popular codes such as ASC11, EBCD1C, Selectric, etc., as well as many specialized codes. The ASC11 code is available as a standard pattern. For special patterns, use Fig. 9.

TIMING DIAGRAM

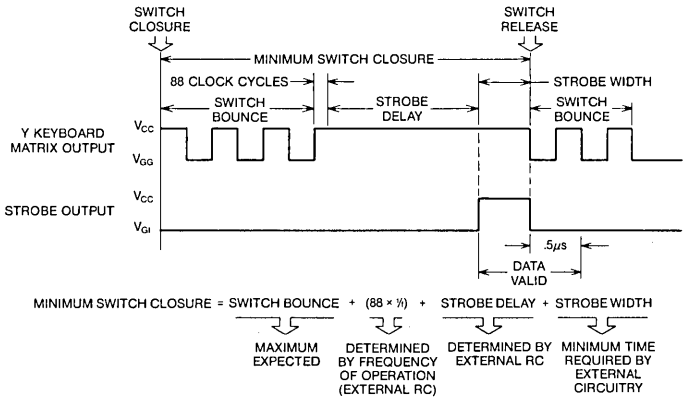
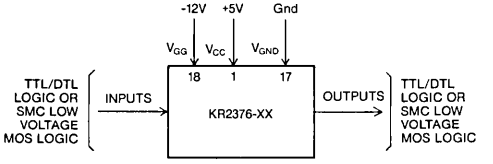


Fig. 2

POWER SUPPLY CONNECTIONS FOR TTL/DTL OPERATION



POWER SUPPLY CONNECTIONS FOR MOS OPERATION

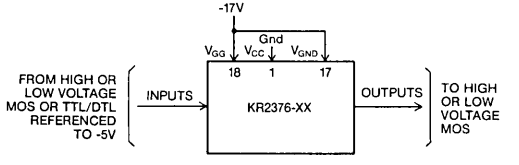
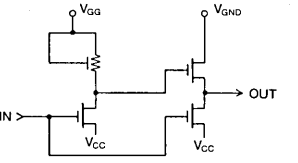


Fig. 3

OUTPUT DRIVER & "X" OUTPUT STAGE TO KEYBOARD



"Y" INPUT STAGE FROM KEYBOARD

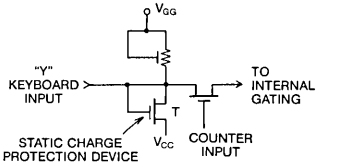


Fig. 4

STROBE DELAY VS. C_1

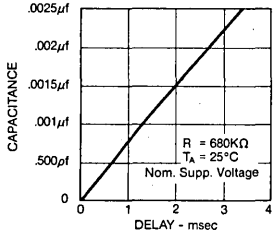


Fig. 5

OSCILLATOR FREQUENCY VS. C_2

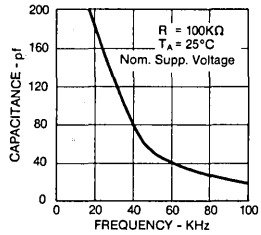


Fig. 6

TYP. OUTPUT ON RESISTANCE VS. GATE BIAS VOLTAGE

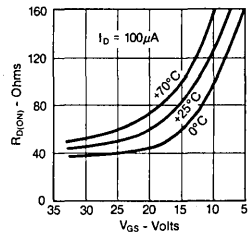


Fig. 7

TYP. POWER CONSUMPTION VS. TEMPERATURE

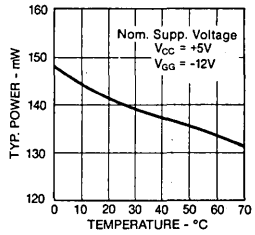


Fig. 8

CODE ASSIGNMENT CHART
KR2376-ST
8 Bit ASCII, odd parity

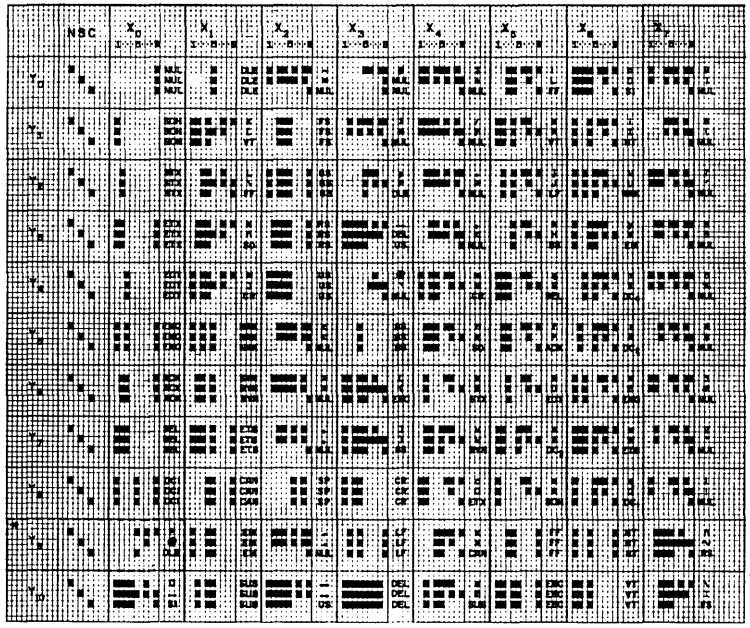


Fig. 9

DATA (B1-B8) INVERT TRUTH TABLE

DATA & STROBE INVERT INPUT (Pin 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

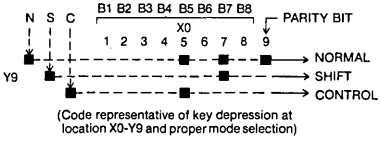
DATA & STROBE INVERT INPUT (Pin 20)	INTERNAL STROBE	STROBE OUTPUT (Pin 16)
1	1	0
0	0	0
1	0	1
0	1	1

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (Pin 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (Pin 7)
1	1	0
0	1	1
1	0	1
0	0	0

MODE SELECTION

$\overline{S}\ \overline{C}$ = N
S $\overline{C}$ = S
$\overline{S}$ C = C
S C = INVALID (SPURIOUS DATA)



(Code representative of key depression at location X0-Y9 and proper mode selection)

N = Normal Mode
S = Shift Mode
C = Control Mode
■ = Output Logic "1" (see data B1-B8)
Logic "1" = +5.0V
Logic "0" = Ground