

Dual N & P-Channel, Logic Level MOSFET

KQS4900

■ Features

● N-Channel

1.3 A, 60 V $R_{DS(ON)} = 0.55 \Omega$ @ $V_{GS} = 10$ V
 $R_{DS(ON)} = 0.65 \Omega$ @ $V_{GS} = 5$ V

● P-Channel

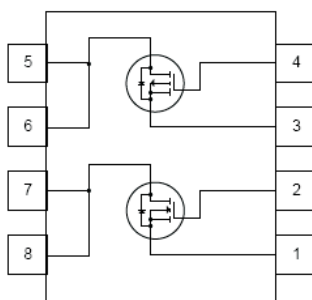
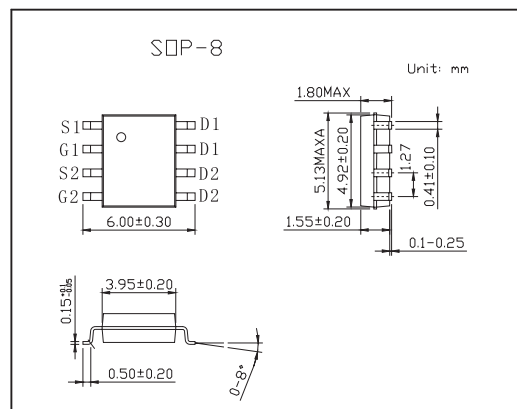
-0.3 A, -300V $R_{DS(ON)} = 15.5 \Omega$ @ $V_{GS} = -10$ V
 $R_{DS(ON)} = 16 \Omega$ @ $V_{GS} = -5$ V

● Low gate charge (typical N-Channel 1.6 nC)

(typical P-Channel 3.6 nC)

● Fast switching

● Improved dv/dt capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DS}	60	-300	V
Gate to Source Voltage	V_{GS}	± 20		V
Drain Current Continuous $T_a = 25^\circ\text{C}$ $T_a = 70^\circ\text{C}$	I_D	1.3 0.82	-0.3 -0.19	A
Drain Current Pulsed *1	I_{DM}	5.2	-1.2	A
Peak Diode Recovery dv/dt	dv/dt	7	4.5	V/ns
Power Dissipation for Single Operation $T_a = 25^\circ\text{C}$ $T_a = 70^\circ\text{C}$	P_D	2 1.3		W
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5		$^\circ\text{C/W}$

*1Repetitive Rating : Pulse width limited by maximum junction temperature

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditions		Min	Typ	Max	Unit	
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μ A	N-Ch	60			V	
		V _{GS} = 0 V, I _D = -250 μ A	P-Ch	-300				
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0 V	N-Ch			1	μ A	
		V _{DS} = 48 V, T _C = 55℃				10		
		V _{DS} = -300 V, V _{GS} = 0 V	P-Ch			-1	μ A	
		V _{DS} = -240 V, T _C = 55℃				-10		
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0 V	N-Ch			±100	nA	
		V _{GS} = ±20 V, V _{DS} = 0 V	P-Ch			±100		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = 4V, I _D = 20mA	N-Ch	1.0		1.95	V	
		V _{DS} = 4V, I _D = -20mA	P-Ch	-1.0		-1.95		
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D =0.65A	N-Ch		0.39	0.55	Ω	
		V _{GS} = 5 V, I _D = 0.65A			0.46	0.65		
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D =-0.15 A	P-Ch		11.2	15.5		
		V _{GS} = -5 V, I _D =-0.15 A			11.4	16		
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 0.65A	N-Ch		1.7		S	
		V _{DS} = -10V, I _D = -0.15A	P-Ch		0.6			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 30 V, I _D = 1.3 A,R _G =25 Ω * P-Channel V _{DD} = -150 V, I _D = -0.3 A,R _G =25 Ω *	N-Ch		5.7	21	ns	
			P-Ch		10	30		
Turn-On Rise Time	t _r		N-Ch		21	50	ns	
			P-Ch		25	60		
Turn-Off Delay Time	t _{d(off)}		N-Ch		11	32	ns	
			P-Ch		35	80		
Turn-Off Fall Time	t _f		N-Ch		17	45	ns	
			P-Ch		47	105		
Total Gate Charge	Q _g	N-Channel V _{DS} =48V,I _D =1.3A,V _{GS} =5V * P-Channel V _{DS} =-240V,I _D =-30.3A,V _{GS} =-5V * P-Channel V _{DS} =-240V,I _D =-30.3A,V _{GS} =-5V *	N-Ch		1.6	2.1	nC	
			P-Ch		3.6	4.7		
Gate-Source Charge	Q _{gs}		N-Ch		0.28		nC	
			P-Ch		0.42			
Gate-Drain Charge	Q _{gd}		N-Ch		0.82		nC	
			P-Ch		2.1			
Maximum Continuous Drain-Source Diode Forward Current	I _S		N-Ch			1.3	A	
			P-Ch			-0.3		
Drain-Source Diode Forward Voltage	V _{SD}		V _{GS} = 0 V, I _S = 1.3A	N-Ch			1.5	V
			V _{GS} = 0 V, I _S = -0.3A	P-Ch			-4.0	

* Pulse Test : Pulse width $\leq$ 300 μ s, Duty cycle $\leq$ 2%