40V, 1A Easy-to-Use High Performance Synchronous Buck Converter

1 Features

- Designed for Reliable and Rugged Applications
  - Wide Input Voltage Range: 6V to 40V
  - 1-A Continuous Output Current
  - 100% Duty Cycle for Low Dropout Operation
  - Support Startup with Pre-biased Output
  - Output OVP and UVP
  - Input OVP and UVLO
  - Over-Temperature Protection
  - ±1% Output Voltage Accuracy
- Integration Reduces Solution Size and Cost
  - Integrated 270-mΩ P-MOSFET Buck Switch Eliminates External Bootstrap Capacitor
  - Integrated 135-mΩ N-MOSFET Synchronous Rectifier Eliminates External Schottky Diode
  - No Loop Compensation Components
  - Internal 2.5-ms Soft Start
  - Fixed 5-V Output (KP521405, KP521405A)
  - Fixed 3.3-V Output (KP521403, KP521403A)
- Suited for Home Appliance
  - Optimized Pin-Out for Single Layer Layout
  - Good EMI Performance

2 Applications

- White Goods, Home Appliances
- Electric Power Tools
- Smart Lighting
- General Purpose Wide VIN Power Supplies

3 Description

The KP52140X(A) is easy-to-use synchronous buck converters capable of driving up to 1-A load current. With a wide input range of 6V to 40V, the device is suitable for a wide range of applications for power conditioning from an unregulated source.

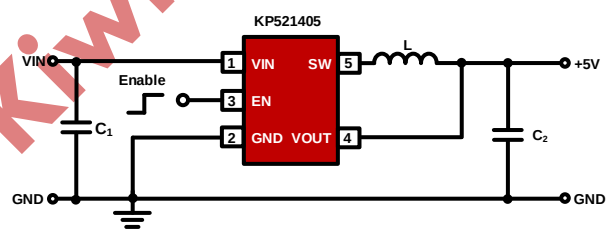
With integrated high-side P-Channel MOSFET and low-side N-Channel MOSFET, the KP52140X(A) eliminates external bootstrap capacitor and Schottky diode. With fixed 5-V or 3.3-V output, the KP52140X(A) require no external feedback resistors. Therefore, the KP52140X(A) can be used with few external components.

The KP52140X(A) adopts low slew rate to turn on and turn off the power MOSFETs, bringing the benefit of good EMI performance.

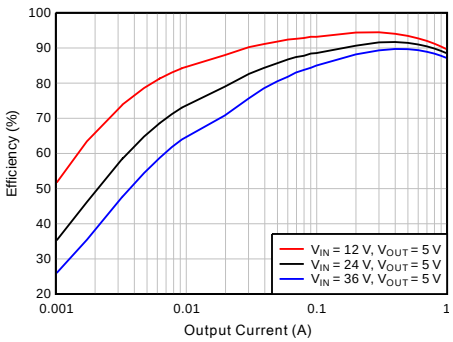
The KP52140X(A) has built-in protection features, such as cycle-by-cycle current limit (OCL), input over-voltage protection and under-voltage lockout, output over-voltage and under-voltage protection, over-temperature protection in case of excessive power dissipation.

The KP52140X(A) is available in TSOT23-5 and TSOT23-6 packages.

Simplified Schematic



Simplified Schematic



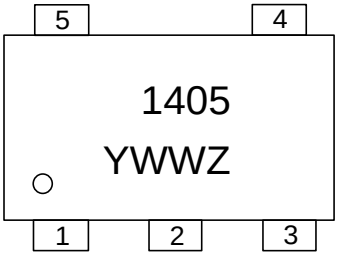
Efficiency vs Load Current

4 Orderable Information

Orderable Device	Output Voltage	Package	Description	Device Marking
KP521405LGA	5 V	TSOT23-5	Halogen Free in T&R, 3000 Pcs/Reel	1405
KP521403LGA	3.3 V	TSOT23-5	Halogen Free in T&R, 3000 Pcs/Reel	1403
KP521405ALGA	5 V	TSOT23-6	Halogen Free in T&R, 3000 Pcs/Reel	1405A
KP521403ALGA	3.3 V	TSOT23-6	Halogen Free in T&R, 3000 Pcs/Reel	1403A

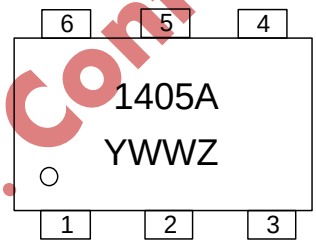
5 Marking Information

Y: Year Code
WW:Week Code, 01-52
Z: Serial Number, 1-9 or A-Z



TSOT23-5

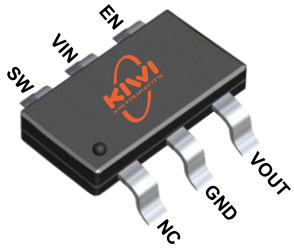
Y: Year Code
WW:Week Code, 01-52
Z: Serial Number, 1-9 or A-Z



TSOT23-6

6 Pin Configuration

TSOT23-5



TSOT23-6

6.1 Pin Function

Pin Number (TSOT23-5)	Pin Number (TSOT23-6)	Pin Name	I/O(1)	Description
1	5	VIN	P	**Supply Voltage.** VIN supplies power to all of the internal control circuitries. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
2	2	GND	G	**System Ground.** GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. Connect the exposed pad to GND plane for optimal thermal performance.
3	4	EN	I/O	**Enable.** Drive EN high or leave it float to enable the device, drive EN low to disable the device. An external pull-down resistor of less than 20kΩ is required to drive EN low effectively.

4	3	VOUT	I	**VOUT.** Connect to the output capacitor directly and keep away from the switch node.
5	6	SW	P	**Switch Node** Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
	1	NC	-	**No Connection.**

(1) I – Input; O – Output; P – Power; G – Ground

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40˚C to 125˚C (unless otherwise noted).

Parameter		Min	Max	Unit
Voltage(1)	VIN, SW	-0.3	44	V
	SW (< 10ns)	-3	44	V
	VOUT	-0.3	6	V
	EN	-0.3	6	V
T_J(2)	Junction Temperature	-40	150	˚C
T_{STG}	Storage Temperature	-55	150	˚C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125˚C, although possible, degrades the lifetime of the device.

7.2 ESD Rating

Paramter			Value	Unit
V_{ESD}	Electrostatic Discharge	Human-body Mode (HBM)(1)	±4000	V
		Charged-device (CDM)(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40˚C to 125˚C (unless otherwise noted).

Parameter		Min	Max	Unit
V_{IN}	Input Supply Voltage Range	6	40	V

I_{OUT}	Output Current Range	0	1	A
Voltage	VIN, SW	-0.3	40	V
	SW (< 10 ns)	-3	40	V
	VOUT	-0.3	5.5	V
	EN	-0.3	5.5	V
T_J	Operating Junction Temperature	-40	125	℃

7.4 Thermal Information

Parameter		KP52140X	KP52140XA	Unit
		TSOT23-5	TSOT23-6	
$R_{\theta JA(EVM)}$ (1)	Junction-to-ambient Thermal Resistance (Specific EVM)	30	29	℃/W

(1) $R_{\theta JA(EVM)}$ are measured on a high effective thermal conductivity 2-layer PCB which is in size of 60mm x 55mm. furthermore, all layers are with 2-Oz Cu. Test Condition: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_A = 25℃. Thermal resistance values may vary depending on the PCB material, layout, and test environmental conditions.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40℃ to +125℃, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25℃, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 6V to 40V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply and Protection						
V_{IN}	Operation Input Voltage		6		40	V
$V_{UVLO(R)}$	VIN UVLO Rising Threshold	VIN Rising		5.4	5.8	V
$V_{UVLO(F)}$	VIN UVLO Falling Threshold	VIN Falling		5.0	5.4	V
$V_{INOVP(R)}$	VIN OVP Rising Threshold	VIN Rising		44		V
$V_{INOVP(F)}$	VIN OVP Falling Threshold	VIN Falling		42		V
$I_{Q(SLEEP)}$	VIN Quiescent Current	Open Loop and Non-switching (V_{EN} = 1.5V, V_{OUT_PIN} = 5.5V, I_{OUT} = 0mA)		320		μA
$I_{Q(SD)}$	VIN Shutdown Current	V_{EN} = 0 V		25	35	μA
Enable and Soft Startup						
$V_{EN(R)}$	EN Voltage Rising Threshold	EN rising, enable switching	1			V
$V_{EN(F)}$	EN Voltage Falling Threshold	EN falling, disable switching			0.4	V

I_{EN}	EN Pin Sourcing Current Pre EN Rising Threshold	V_{EN} = 0 V		13	25	μA
T_{ss}	Soft Start Time	10% to 90% V_{OUT}		2.5		ms
Output and Protection						
V_{OUT}	Output voltage, KP521405/KP521405A	T_J = 25˚C	4.95	5.0	5.05	V
		T_J = -40˚C ~ 125˚C	4.9	5.0	5.1	V
	Output voltage, KP521403/KP521403A	T_J = 25˚C	3.26	3.3	3.34	V
		T_J = -40˚C ~ 125˚C	3.22	3.3	3.38	V
$V_{OVP(R)}$	Output OVP rising threshold	VOUT Rising		110%		V_{OUT}
$V_{OVP(F)}$	Output OVP falling threshold	VOUT Falling		105%		V_{OUT}
$V_{UVP(F)}$	Output UVP falling threshold	VOUT Falling		50%		V_{OUT}
$V_{UVP(R)}$	Output UVP rising threshold	VOUT Rising		55%		V_{OUT}
$t_{HIC(WAIT)}$	Wait time before entering Hiccup			160		μs
$t_{HIC(RE)}$	Hiccup time before restart			40		ms
Power Switches						
$R_{DSON(HS)}$	High-side MOSFET On-resistance	T_J = 25˚C, V_{IN} = 12V		270		mΩ
$R_{DSON(LS)}$	Low-side MOSFET On-resistance	T_J = 25˚C, V_{IN} = 12V		135		mΩ
$t_{ON(min)}$(1)	Minimum ON Pulse Width			200		ns
D_{max}	Maximum Duty Cycle			100		%
Switching Frequency						
f_{SW}	Switching Frequency	I_{OUT} = 0.5A	80	100	120	kHz
Current Limit						
I_{PK}	Peak Current Limit	V_{IN} = 12V	1.5	1.8	2.1	A
Over Temperature Protection(1)						
$T_{J(SD)}$	Thermal Shutdown Threshold			160		˚C
$T_{J(HYS)}$	Thermal Shutdown Hysteresis			50		˚C

(1) Not production test, guaranteed by design.

7.6 Typical Characteristics

Unless otherwise noted, the following conditions apply: V_{IN} = 12V, T_A = 25˚C.

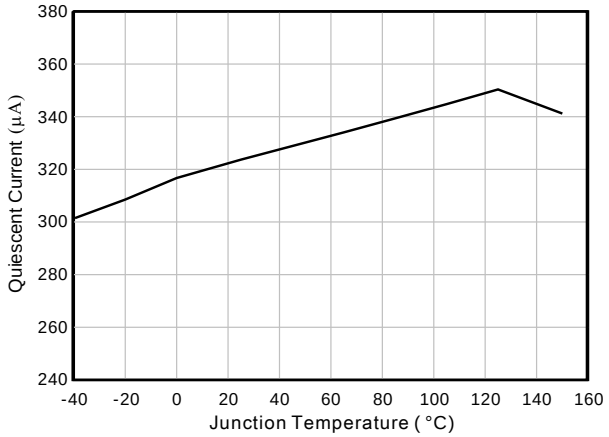


Figure 1. Quiescent Current vs Junction Temperature

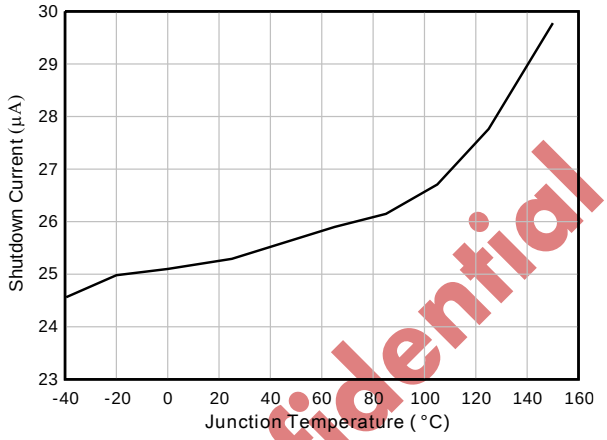


Figure 2. Shutdown Current vs Junction Temperature

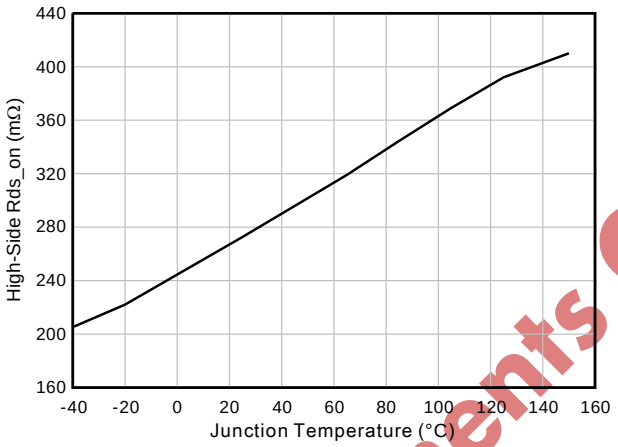


Figure 3. High-side MOSFET On-resistance vs Junction Temperature

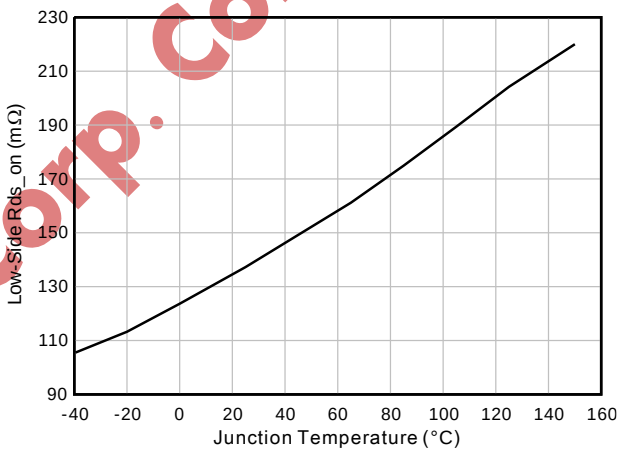


Figure 4. Low-side MOSFET On-resistance vs Junction Temperature

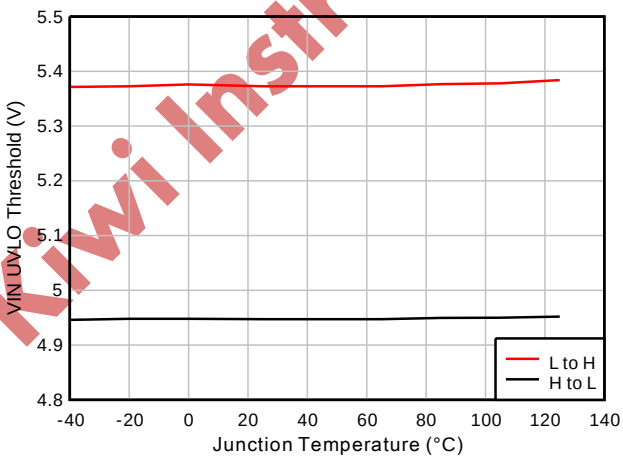


Figure 5. VIN UVLO Threshold vs Junction Temperature

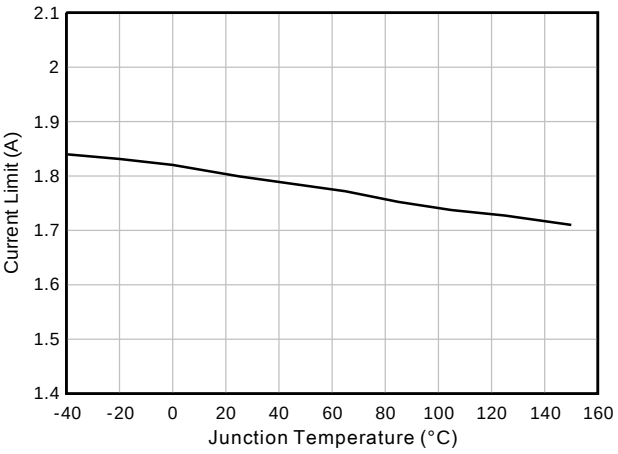
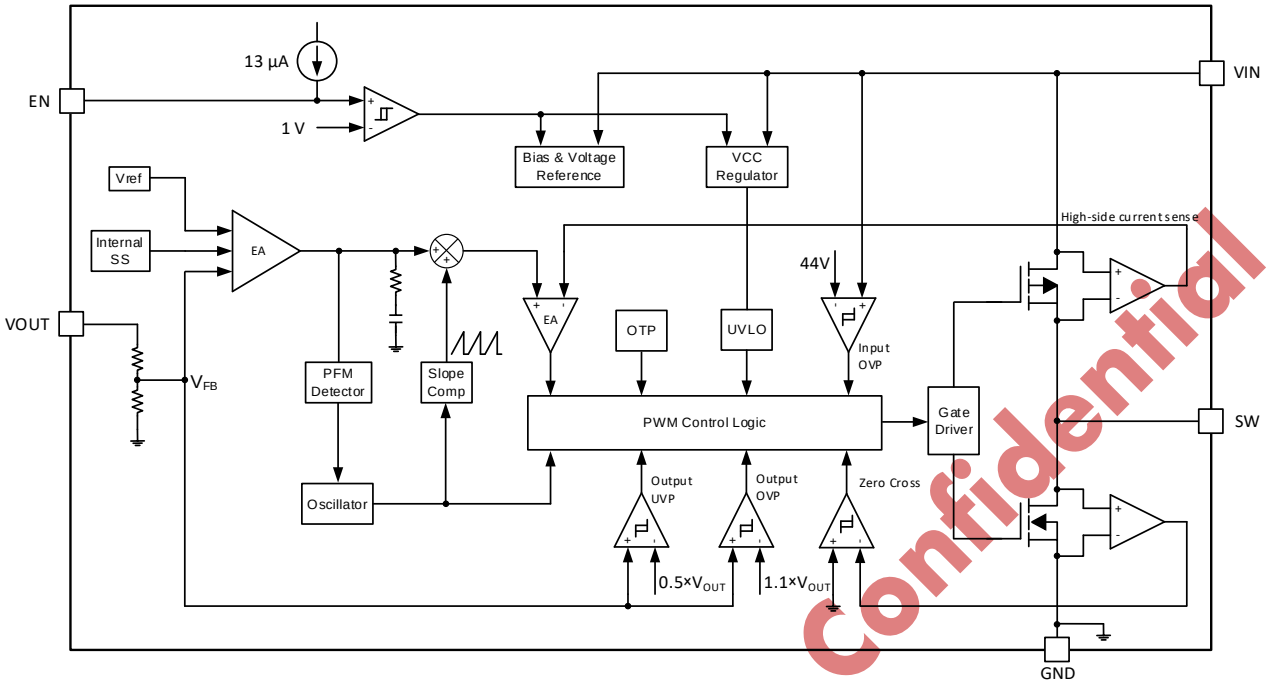


Figure 6. High-side Current Limit Threshold vs Junction Temperature

8 Block Diagram



9 Operation Description

The KP52140X is fully integrated synchronous buck converter that operates from 6-V to 40-V input voltage with fixed output voltage. Peak Current Mode (PCM) control provides fast transient responses with fixed switching frequency under normal load for good EMI performance. Pulse skip mode at light load improves light load efficiency.

9.1 CCM Operation

Continuous Conduction Mode (CCM) operation is employed in the device when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum continuous output current of 1 A can be supplied by the device.

As shown in the **Figure 7**, during CCM operation, the internal clock initiates one pulse, and the high-side MOSFET turns on, with current increasing in the inductor. When the sensed current reaches the control voltage, the high-side MOSFET turns off and the low-side MOSFET turns on until the next rising edge of the clock. The next PWM pulse is generated at the next clock pulse. Thus, the switching frequency depending on the clock is truly fixed.

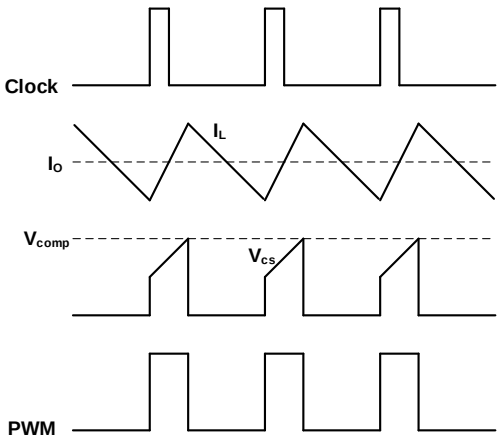


Figure 7. PCM Control Schema Waveform

9.2 DCM and PSM Operation

As the output current decreases from heavy load condition, the inductor current reduces as well and eventually comes to a point that its rippled valley touches zero level, which is the boundary between CCM and DCM. The low-side MOSFET is turned off when the inductor current crossing zero is detected. As the load current further decreases, the converter runs into DCM

As the output load current is lowered, the required peak current on each switching cycle is lessened and the COMP voltage is reduced by the error amplifier in the closed loop system. Once the converter is in regulation and the COMP voltage is lowered to 0.5 V nominal. Pulse skip mode is activated to maintain high efficiency operation. In pulse skip mode, the COMP voltage is clamped at 0.5V which prevents the high side integrated MOSFET from switching. Since the device is not switching, the output voltage will start to decay as energy is drawn from the output capacitors to supply the load current. As the output voltage decreases, the control loop will sense the decreased voltage at VOUT and start to drive the COMP above the pulse skip mode threshold voltage.

9.3 Low Dropout Operation

The KP52140X(A) offers the lowest possible input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel MOSFET is constantly turned on. The minimum input voltage to maintain regulation depends on the load current and output voltage. It can be calculated using equation **(1)**.

$$V_{IN\_MIN} = V_{OUT\_MAX} + I_{OUT\_MAX} \times (R_{DS(ON)_{MAX}} + R_{DCR}) \quad (1)$$

Where,

- I_{OUT_MAX} is maximum output current plus inductor ripple current
- $R_{DS(ON)_{MAX}}$ is maximum high-side MOSFET On- resistance
- R_{DCR} is DC resistance of the inductor
- V_{OUT_MAX} is nominal output voltage plus maximum output voltage tolerance.

9.4 Enable Control

The EN pin provides electrical on and off control for the device. Drive EN high to enable the regulator. Drive EN low to disable it. When the regulator was disabled, the device in shutdown mode with a shutdown current of 25μA (typical).

The EN pin would be charged to 4.5 V roughly by an internal pullup source current of 13μA, which allows user to float the EN pin to enable the device. An external pull-down resistor of less than 20kΩ is required to drive EN low effectively.

9.5 VIN UVLO

The KP52140X(A) implements internal under voltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The UVLO rising threshold is about 5.4 V, while its falling threshold is 5.0V.

9.6 VIN OVP

The KP52140X(A) integrates input over-voltage protection (OVP) to ensure the reliability when the input voltage is unstable with overvoltage spike. The OVP circuitry detects overvoltage condition by monitoring the input voltage. When the VIN is higher than the $V_{INOVP(R)}$, the HSF and LSF are turned off, the device stops working. It resumes operation when the VIN is less than the $V_{INOVP(F)}$.

9.7 Current Limit and Output UVP

The KP52140X(A) implements peak current-mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP high, causing the switch current to increase. The COMP has a maximum clamp internally, which limit the output current.

The KP52140X(A) provides robust protection during short circuits. Overcurrent runaway is possible in the output inductor during a short circuit at the output. The KP52140X(A) solves this issue by increasing the off time during short-circuit conditions by lowering the switching frequency. The switching frequency is divided by 2 as the output voltage is lower than 50% of the target.

There are some important considerations for this

type of overcurrent protection. The load current is higher than the overcurrent threshold by one-half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. When the output voltage falls below the UVP threshold voltage, the UVP comparator detects it. The device shuts down after the UVP delay time (typically 160μs) and re-starts after the hiccup time (typically 40ms). The hiccup behavior helps reduce the device power dissipation under severe overcurrent conditions.

9.8 Output Over-Voltage Protection

The KP52140X(A) integrates output over-voltage protection (OVP) to minimize output voltage overshoot and protect down-stream devices when recovering from output fault conditions or strong unload transients. The OVP circuitry detects overvoltage condition by monitoring the feedback voltage (V_{FB}). When V_{FB} rises above the OVP threshold (V_{OVP}), the OVP comparator output turns high and both high-side and low-side MOSFETs turn off to avoid V_{OUT} further rising higher. Once the V_{OUT} drops below V_{OVP}, the device starts to switching again. This function is a non-latch operation.

9.9 Soft Start and Pre-Biased Soft Start

The KP52140X(A) provides an internal soft-start feature to ensure inrush control and smooth output voltage ramping during power-up, and the output voltage starts to rise after a 300μs delay from EN rising edge.

When the device starts, the soft-start circuitry generates a soft-start voltage (V_{SS}) ramping up from 0V. When it is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF} so the error amplifier and comparator use SS as the reference voltage. The output voltage smoothly ramps up. Once SS rises above V_{REF}, V_{REF} regains control. At this time the soft start process ends and the KP52140X(A) enters steady state operation. The soft start time (T_{SS}) is internal fixed at around 2.5ms (10% to 90%).

If the output capacitor is pre-biased at startup, the KP52140X(A) initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

9.10 Over Temperature Protection

The KP52140X(A) include an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold $T_{J(SD)}$. Once the junction temperature cools down by a thermal shutdown hysteresis $T_{J(HYS)}$, the device will resume normal operation with a complete soft-start.

10 Application Information

The KP52140X(A) only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. The external components should fulfill the needs of the application, but also the stability criteria of the device's control loop. **Figure 31** and **Figure 32** can be used to simplify the output filter component selection.

10.1 Design Example

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in **Table 1** as the design parameters.

Table 1. Design Example Parameters

Parameters	Value
Input Voltage Range	6V to 40V
Output Voltage	5V
Output Current Rating	1A
Output Voltage Ripple	±0.5%
Output Overshoot / Undershoot (0.2A to 0.8A / 0.8A to 0.2A)	±5%

10.2 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use equation **(3)** to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 60%. During an instantaneous over current operation event, the RMS and peak inductor current can be high. The inductor current rating should be a bit higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (2)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (3)$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more inductor core loss since the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 73µH. Choose the standard 100-µH ferrite inductor with a capability of 1.45-A RMS current and 2.4-A saturation current.

It is worth noting that since the maximum input voltage has a great influence on the selection of the minimum inductance, from the perspective of optimizing the inductor size and cost. the corresponding inductance can be selected depending on different input voltage levels as shown in **Table 2.**

Table 2. Recommended Components

V_{OUT} (V)	V_{IN} (V)	L (µH)	C_1	C_{1A} (1)	C_2	C_{2A} (2)
5	12	68	22µF / 25V	1µF / 50V	4 × 22µF / 10V (100µF / 10V, E-cap)	--- (1µF / 10V)
	24	82	22µF / 35V			
	36	100	100µF / 50V, E-cap			
3.3	12	47	22µF / 25V			
	24	56	22µF / 35V			
	36	68	100µF / 50V, E-cap			

(1) If electrolytic capacitor selected for C_1, no less than 1μF ceramic capacitor recommended for C_{1A}. If ceramic capacitor selected for C_1, 0.1μF ceramic capacitor recommended for C_{1A}.

(2) If electrolytic capacitor selected for C_2, no less than 1μF ceramic capacitor recommended for C_{2A}. If ceramic capacitor selected for C_2, no need C_{2A}。

10.3 Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors.

$$\Delta V_{OUT\_ESR} = \Delta i_L \times R_{ESR} = K_{IND} \times I_{OUT} \times R_{ESR} \quad (4)$$

The other is caused by the inductor current ripple charging and discharging the output capacitors. Use equation **(5)** to estimate the output ripple voltage.

$$\Delta V_{OUT\_C} = \Delta i_L \times \frac{(D-0.5)}{4 \times f_{SW} \times C_{OUT}} \quad (5)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs 2 or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for 2 clock cycles to maintain the output voltage within the specified range. equation **(6)** shows the minimum output capacitance needed for specified VOUT overshoot and undershoot.

$$C_{OUT} > \frac{2 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \quad (6)$$

Where,

- I_{OL} is the low level output current during load transient
- I_{OH} is the high level output current during load transient
- V_{OUT_SHOOT} is the target output voltage overshoot or undershoot

KP521405X(A) has an internal zero point to compensate the pole point caused by the output capacitor and load resistor. Therefore, the output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency within $\frac{1}{10} \sim \frac{1}{2}$ of the switching frequency. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation **(7)**, assuming C_{OUT} has small ESR.

$$C_{OUT} > \frac{R_C \times G_M \times G_{MP} \times V_{REF}}{2\pi \times V_{OUT} \times f_C} \quad (7)$$

Where,

- G_M = 10μS, the transfer conductance of the error amplifier
- R_C = 1MΩ, the internal loop compensation resistance
- G_{MP} = 2.3A/V, the gain from internal COMP to inductor current
- V_{REF} = 0.8V, the internal reference voltage
- f_C is the target cross frequency. Select 16kHz for this design example.

For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50 mV, and chose K_{IND} = 0.4. Equation **(4)** yields R_{ESR} no larger than 125 mΩ and Equation **(5)** yields C_{OUT} no smaller than 10 μF. For the target overshoot and undershoot limitation of this design, $\Delta V_{OUT\_SHOOT} = 5\% \times V_{OUT}$ = 250 mV. The C_{OUT} can be calculated to be no smaller than 48μF by Equation **(6)**. Equation **(7)** yields C_{OUT} no smaller than 37μF for loop stability. In summary, the most stringent criteria for the output capacitor is 48μF.

The selected output capacitor must be rated for a voltage greater than the desired output voltage plus half of the ripple voltage. Any derating amount must also be included.

An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation **(8)** can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{COUT(RMS)} = \frac{V_{OUT}\times(V_{IN(MAX)}-V_{OUT})}{\sqrt{12}\times V_{IN(MAX)}\times L\times f_{SW}\times N_C} \quad (8)$$

Where,

- N_C is the number of output capacitor in parallel.

10.4 Input Capacitor Selection

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the step-down converter while also maintaining the DC input voltage. Use low ESR capacitors as close to VIN as possible for the best performance, especially under high switching frequency applications. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. The voltage rate of the input capacitor is recommended to be twice higher than the maximum input voltage. The RMS current through the input capacitor can be calculated with Equation **(9)**.

$$I_{IN\_AC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

With low ESR capacitors, the input voltage ripple can be estimated with Equation **(10)**.

$$\Delta V_{IN} = \frac{I_{OUT}\times V_{OUT}}{f_{sw}\times C_{IN}\times V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

Choose an input capacitor with enough RMS current rating and enough capacitance for small input voltage ripples.

When electrolytic or tantalum capacitors are applied, a small, high-quality ceramic capacitor (i.e.: 0.1μF) should be placed as close to the IC as possible.

10.5 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin.
2. Make VIN, VOUT and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
3. Minimize trace length to the VOUT pin net. If VOUT accuracy at the load is important, make sure VOUT sense is made at the load. Route VOUT sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
5. Provide adequate device heat-sinking. GND, VIN and SW pins provide the main heat dissipation path, make the GND, VIN and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125˚C.

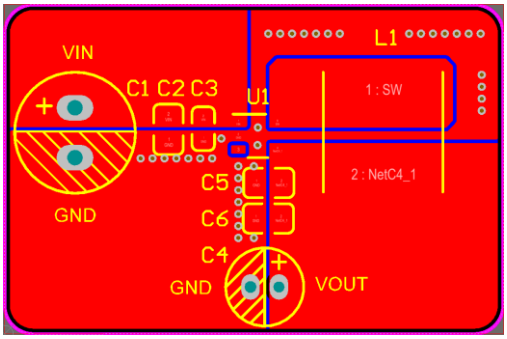


Figure 8. Layout Example

10.6 Application Curves

KP521405, V_{IN} = 12V, T_A = 25˚C, L_1 = 100µH, R_{DCR} = 230mΩ, C_{OUT} = 100µF, unless otherwise noted.

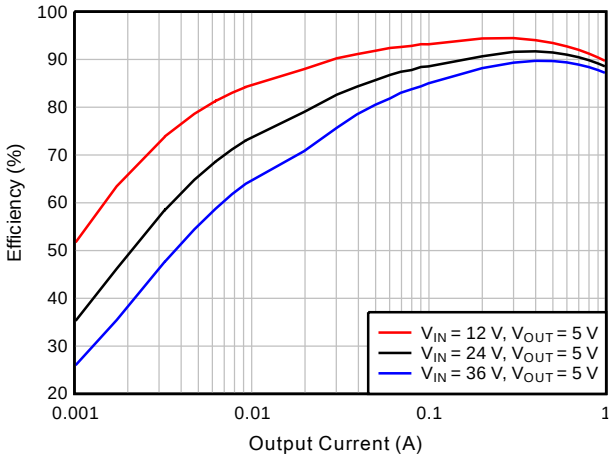


Figure 9. 5V Efficiency, L_1 = 68µH, R_{DCR} = 289mΩ

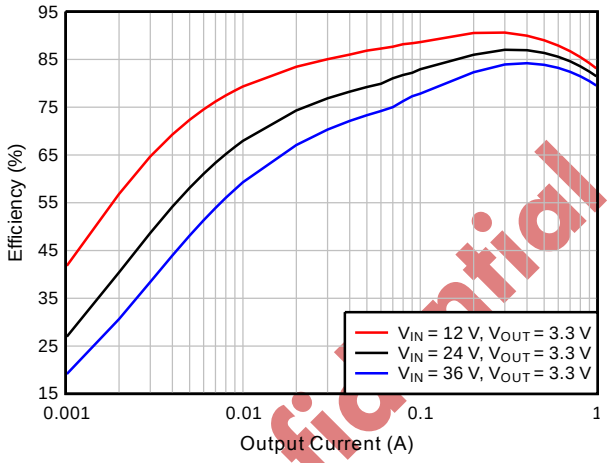


Figure 10. 3.3V Efficiency, L_1 = 68µH, R_{DCR} = 289mΩ

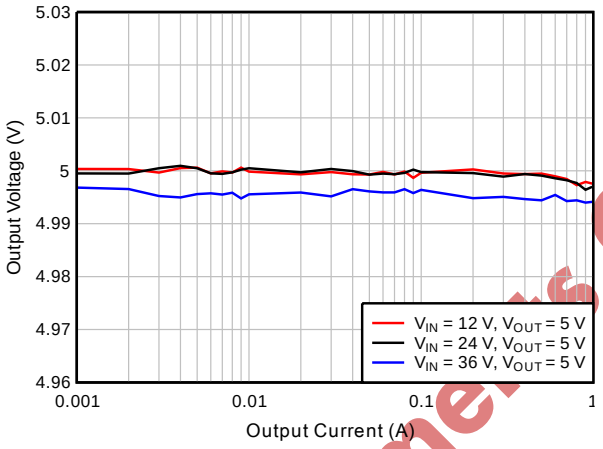


Figure 11. 5V Load Regulation

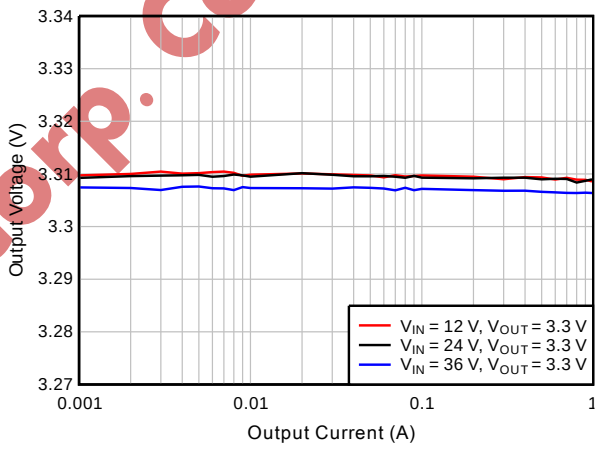


Figure 12. 3.3V Load Regulation

Figure 13. Thermal Performance, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1A

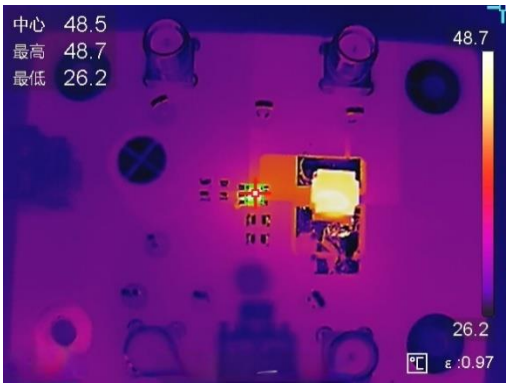


Figure 14. Thermal Performance, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A

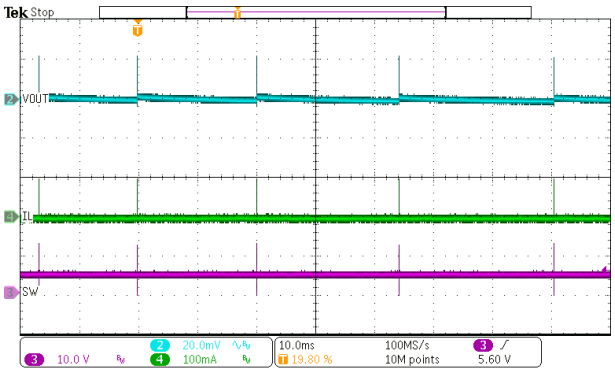


Figure 15. Steady State Waveforms, I_{OUT} = 0A

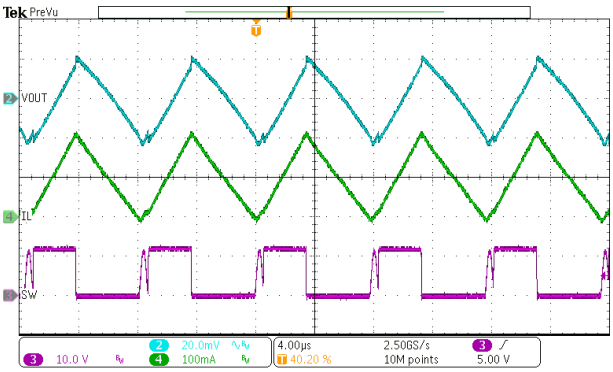


Figure 16. Steady State Waveforms, I_{OUT} = 0.1A

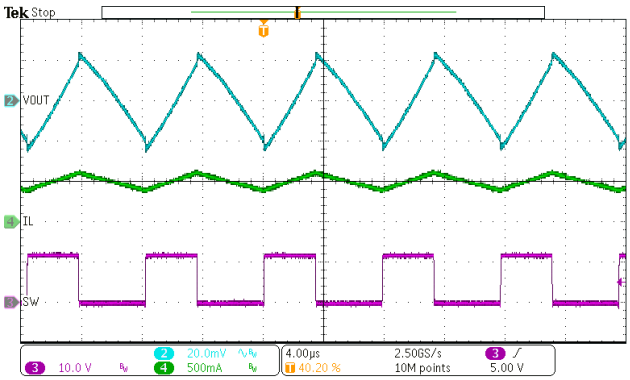


Figure 17. Steady State Waveforms, I_{OUT} = 0.5A

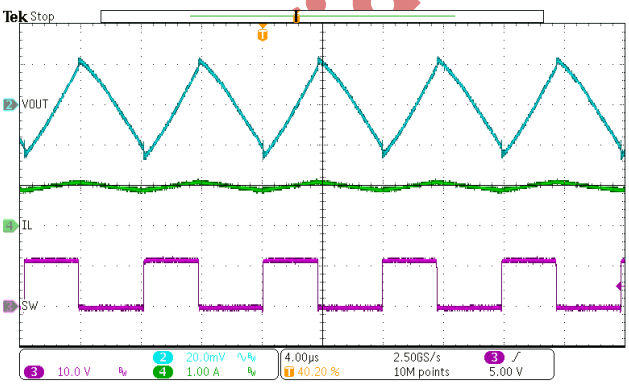


Figure 18. Steady State Waveforms, I_{OUT} = 1A

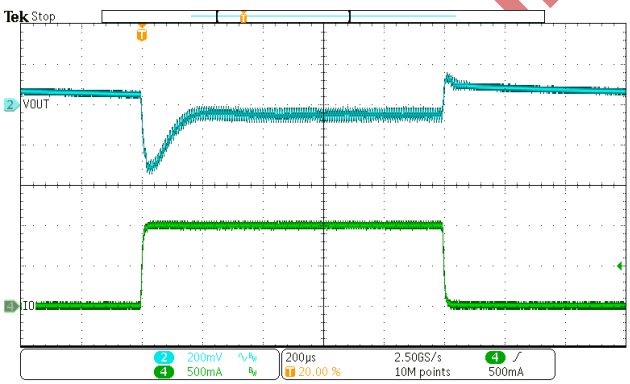


Figure 19. Transient Response from 0 to 1A with slew rate of 0.25 A/µs

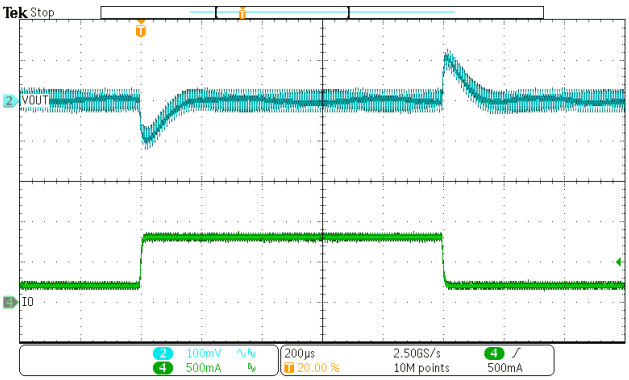


Figure 20. Transient Response from 0.2 to 0.8A with slew rate of 0.25 A/µs

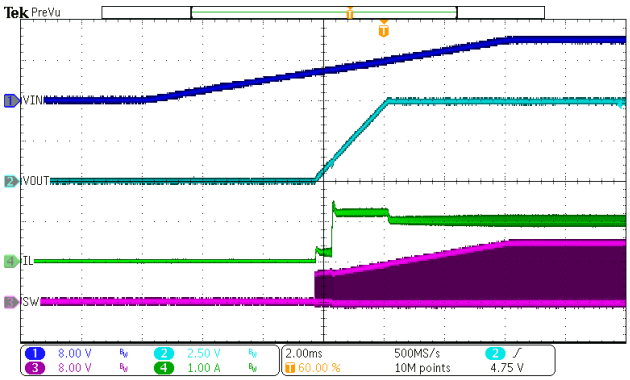


Figure 21. Start-up Relative to VIN

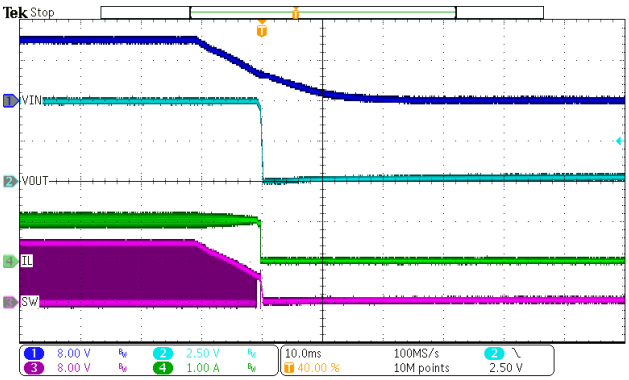


Figure 22. Shutdown Relative to VIN

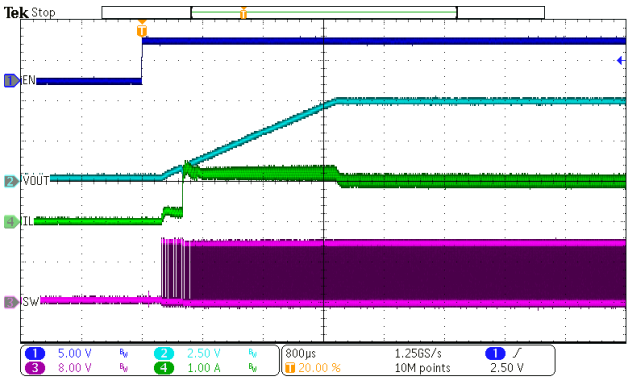


Figure 23. Enable Relative to EN

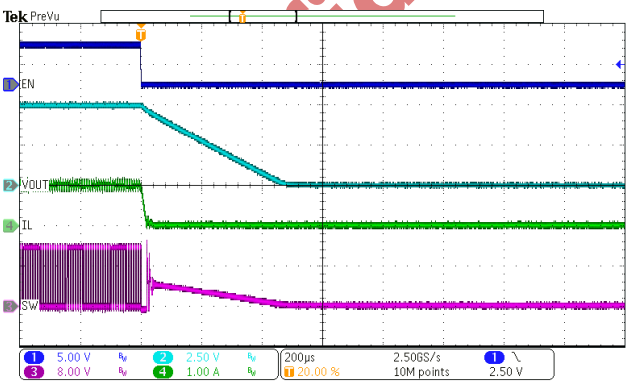


Figure 24. Disable Relative to EN

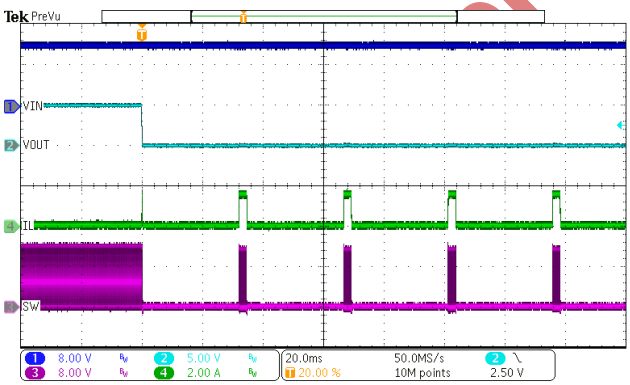


Figure 25. Output Short Protection

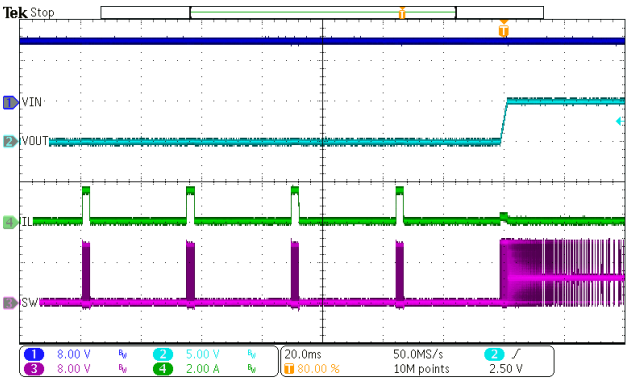


Figure 26. Output Short Recovery

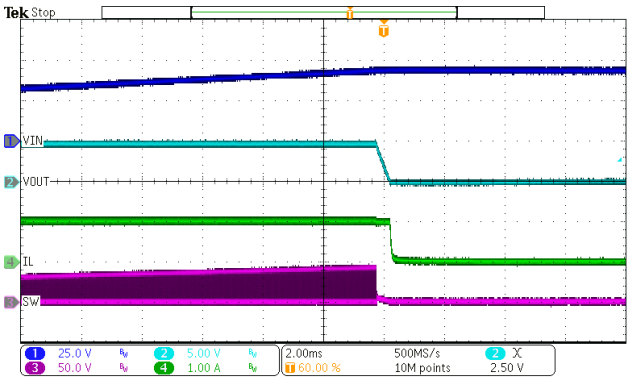


Figure 27. Input OVP

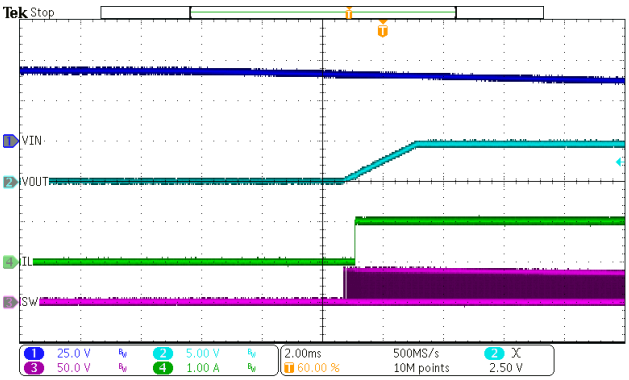


Figure 28. Input OVP Recovery

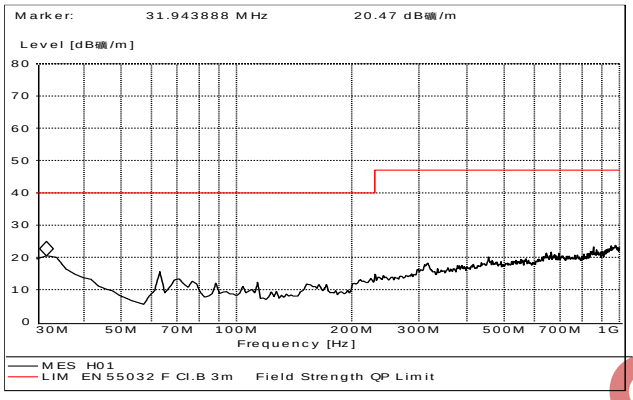


Figure 29. Radiant Emission, EN55032 class B 3m, Horizontal, I_{OUT} = 1A

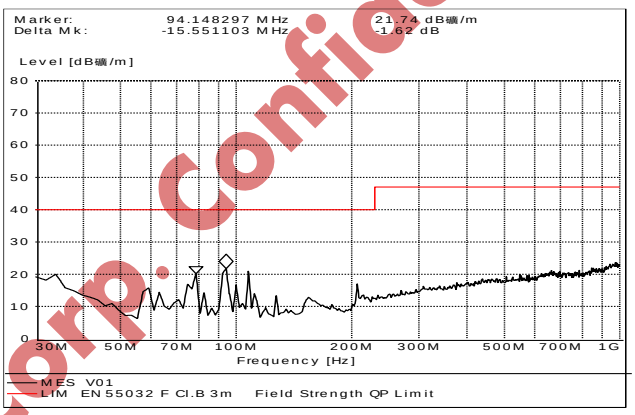


Figure 30. Radiant Emission, EN55032 class B 3m, Vertical, I_{OUT} = 1A

11 Typical Application Circuit

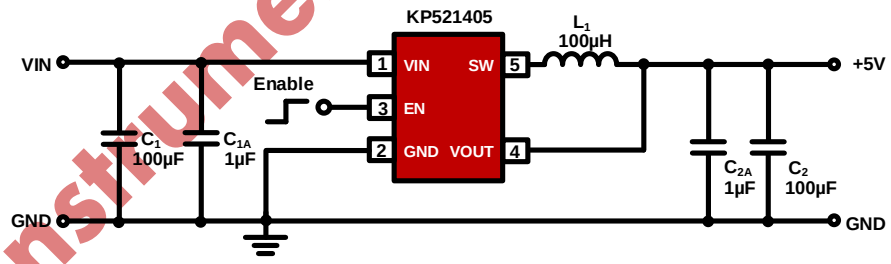


Figure 31. V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1A

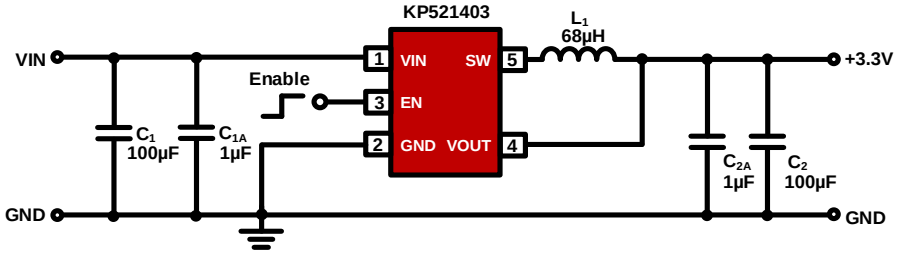
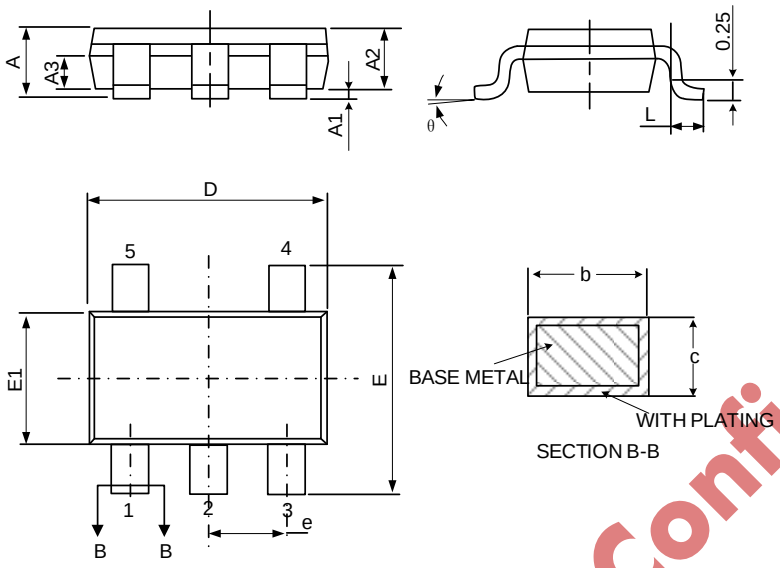


Figure 32. V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A

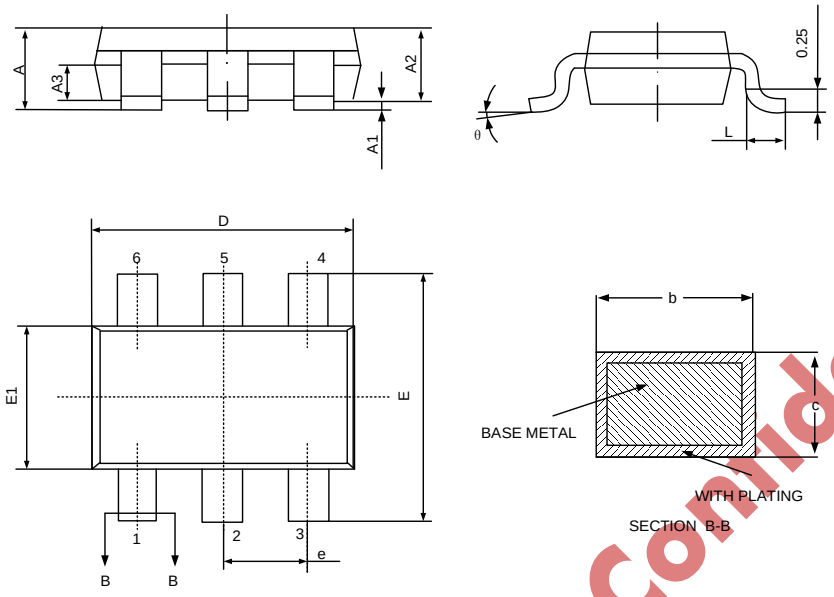
12 Package Dimension

TSOT23-5



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	-	0.950	-	0.037
A1	0.000	0.150	0.000	0.006
A2	0.750	0.850	0.030	0.033
A3	0.350	0.450	0.014	0.018
b	0.300	0.500	0.012	0.020
c	0.077	0.200	0.003	0.008
D	2.700	3.100	0.106	0.122
E	2.600	3.000	0.102	0.118
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
L	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

TSOT23-6



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	-	0.950	-	0.037
A1	0.000	0.150	0.000	0.006
A2	0.750	0.850	0.030	0.033
A3	0.350	0.450	0.014	0.018
b	0.300	0.500	0.012	0.020
c	0.077	0.200	0.003	0.008
D	2.700	3.100	0.106	0.122
E	2.600	3.000	0.102	0.118
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
L	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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