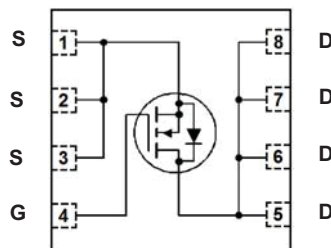


N-Channel MOSFET

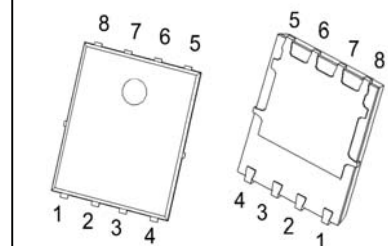
AON6512 (KON6512)

■ Features

- $V_{DS} (V) = 30 V$
- $I_{D(MAX)} (at V_{GS} = 10 V) = 150 A$
- $R_{DS(ON)} (at V_{GS} = 10 V) < 1.7 m\Omega$
- $R_{DS(ON)} (at V_{GS} = 4.5 V) < 2.4 m\Omega$
- Low Gate Charge
- High Current Capability



DFN5x6-8(PDFNWB5x6-8L)

■ Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^G	I_D	$T_C = 25^\circ C$	A
		$T_C = 100^\circ C$	
Pulsed Drain Current ^C	I_{DM}	340	
Continuous Drain Current	I_{DSM}	$T_A = 25^\circ C$	
		$T_A = 75^\circ C$	
Avalanche Current ^C	I_{AS}	70	
Avalanche Energy $L = 0.05 mH$ ^C	E_{AS}	123	mJ
V_{DS} Spike	V_{SPIKE}	36	V
Power Dissipation ^B	P_D	$T_C = 25^\circ C$	W
		$T_C = 100^\circ C$	
Power Dissipation ^A	P_{DSM}	$T_A = 25^\circ C$	
		$T_A = 70^\circ C$	
Thermal Resistance.Junction- to-Ambient ^A	R_{thJA}	$t \leq 10s$	$^\circ C/W$
Thermal Resistance.Junction- to-Ambient ^{A,D}		Steady-State	
Thermal Resistance.Junction- to-Case	R_{thJC}	Steady-State	
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature Range	T_{stg}	-55 to 150	

Notes:

- A. The value of R_{thJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$. The Power dissipation P_{DSM} is based on R_{thJA} and the maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Single pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ C$.
- D. The R_{thJA} is the sum of the thermal impedance from junction to case R_{thJC} and case to ambient.
- G. The maximum current rating is package limited.

N-Channel MOSFET

AON6512 (KON6512)

■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DS}	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\text{V}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$			1	μA
		$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 55^\circ\text{C}$			5	
Gate to Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$			± 100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$			1.7	m Ω
		$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$, $T_J = 125^\circ\text{C}$			2.3	
		$V_{GS} = 4.5\text{V}$, $I_D = 20\text{A}$			2.4	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{V}$, $I_D = 20\text{A}$		85		S
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 15\text{V}$, $f = 1\text{MHz}$		3430		pF
Output Capacitance	C_{oss}			1327		
Reverse Transfer Capacitance	C_{rss}			175		
Gate Resistance	R_g	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$, $f = 1\text{MHz}$	0.3		1.1	Ω
Total Gate Charge	$Q_g(10\text{V})$	$V_{GS} = 10\text{V}$, $V_{DS} = 15\text{V}$, $I_D = 20\text{A}$		53	64	nC
Total Gate Charge	$Q_g(4.5\text{V})$			25	30	
Gate Source Charge	Q_{gs}			7.8		
Gate Drain Charge	Q_{gd}			10.3		
Turn-On DelayTime	$t_{d(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 15\text{V}$, $R_L = 0.75\ \Omega$, $R_{GEN} = 3\ \Omega$		7.5		ns
Turn-On Rise Time	t_r			5.0		
Turn-Off DelayTime	$t_{d(off)}$			33.8		
Turn-Off Fall Time	t_f			9.8		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{A}$, $di/dt = 500\text{A}/\mu\text{s}$		22		nC
Body Diode Reverse Recovery Charge	Q_{rr}			58		
Maximum Body-Diode Continuous Current	I_S				85	A
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_S = 1\text{A}$			1	V

Notes:

E. The static characteristics in Figures 1 to 6 are obtained using <300s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 150^\circ\text{C}$. The SOA curve provides a single pulse rating.H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.

N-Channel MOSFET

AON6512 (KON6512)

■ Typical Characteristics

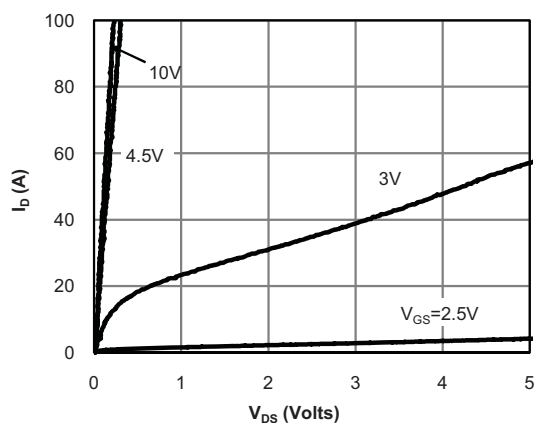


Fig 1: On-Region Characteristics (Note E)

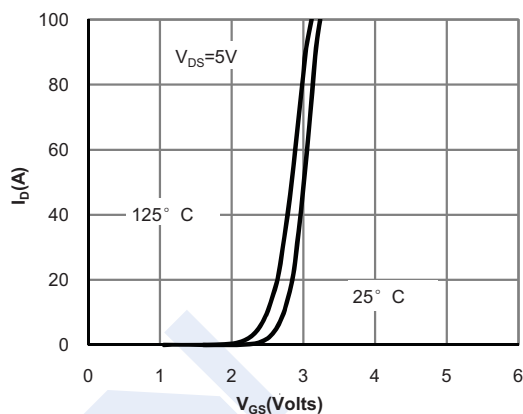


Figure 2: Transfer Characteristics (Note E)

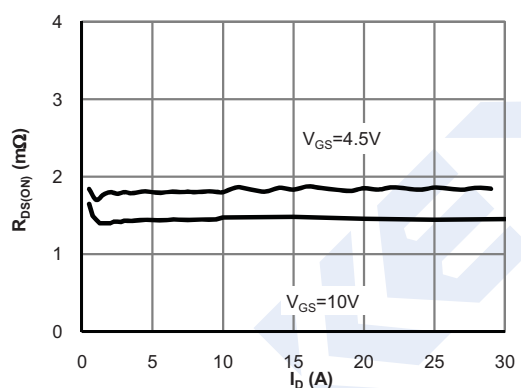


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

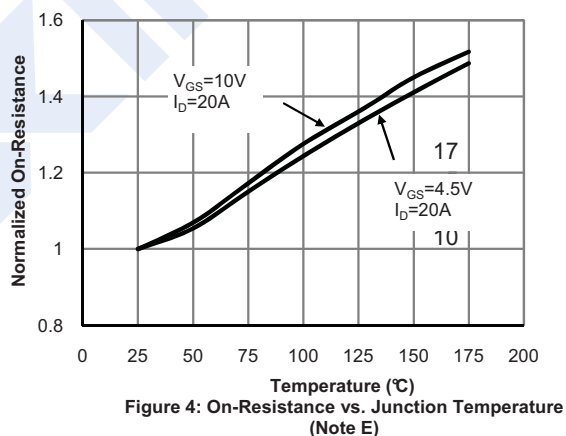


Figure 4: On-Resistance vs. Junction Temperature (Note E)

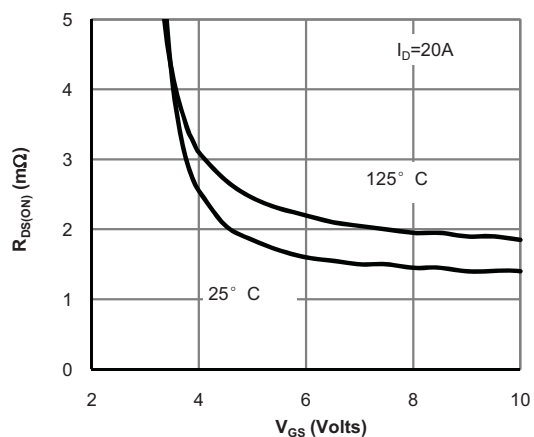


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

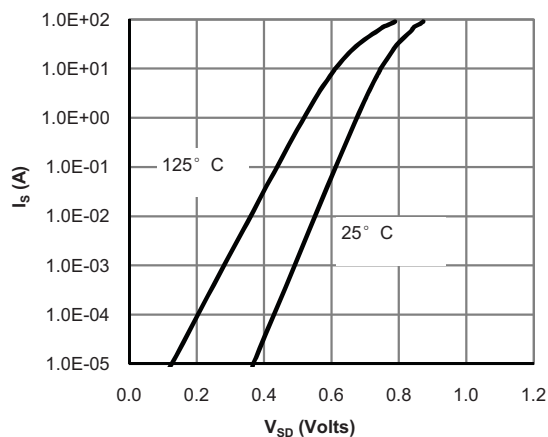
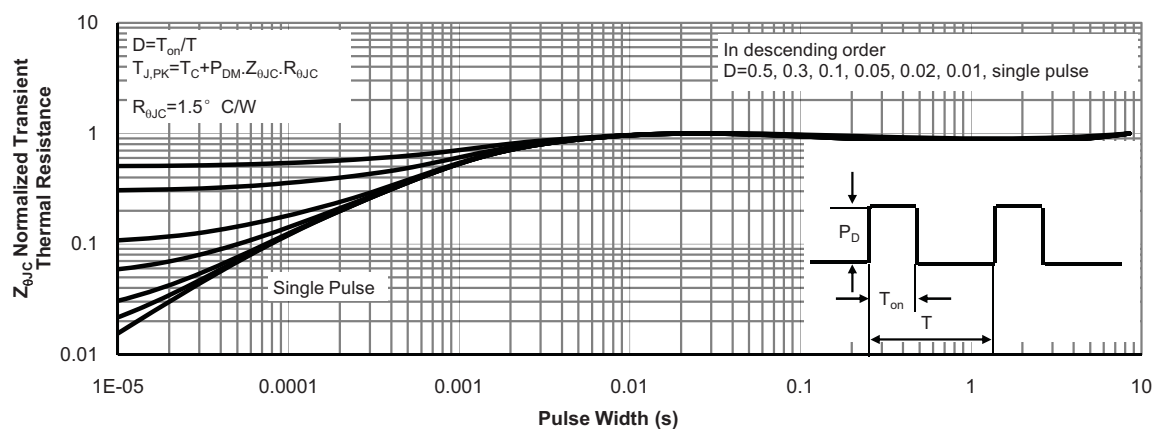
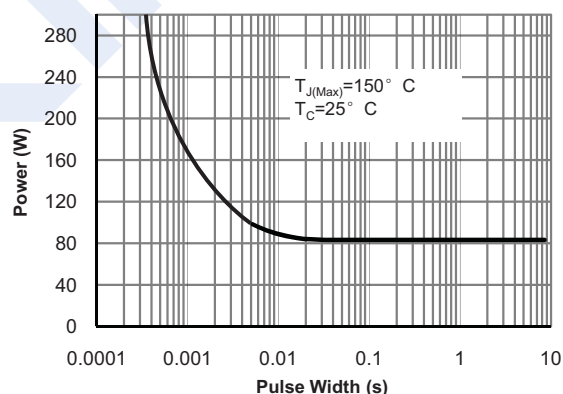
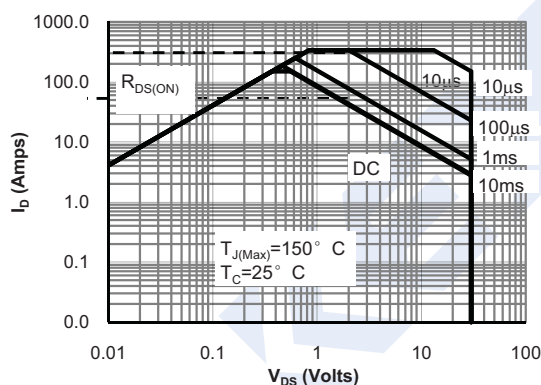
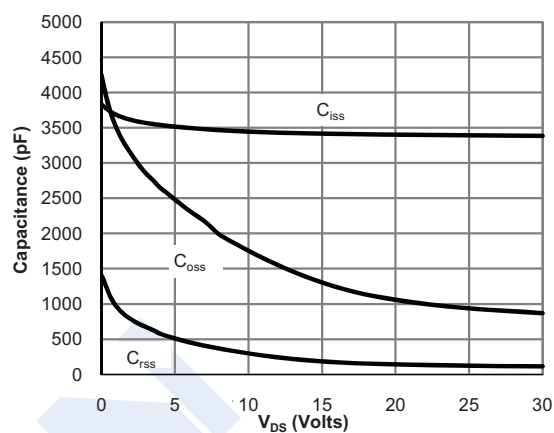
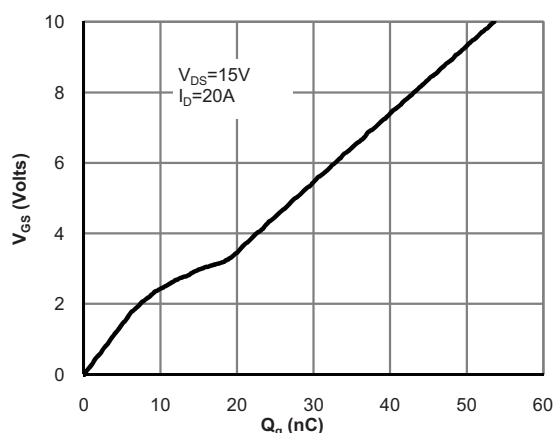


Figure 6: Body-Diode Characteristics (Note E)

N-Channel MOSFET

AON6512 (KON6512)

■ Typical Characteristics



N-Channel MOSFET

AON6512 (KON6512)

■ Typical Characteristics

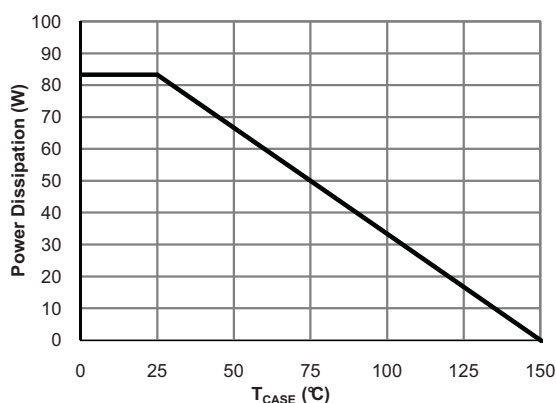


Figure 12: Power De-rating (Note F)

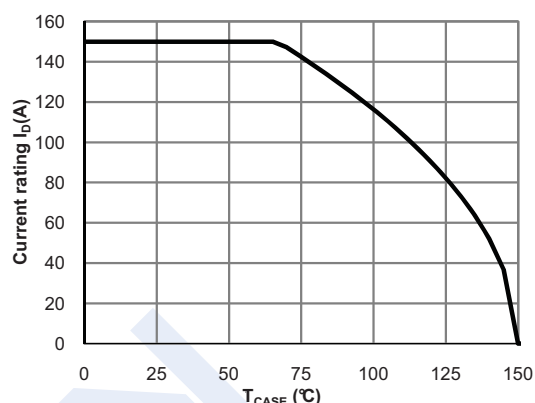


Figure 13: Current De-rating (Note F)

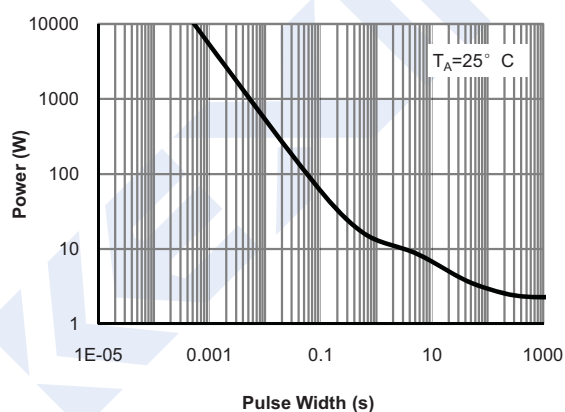


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

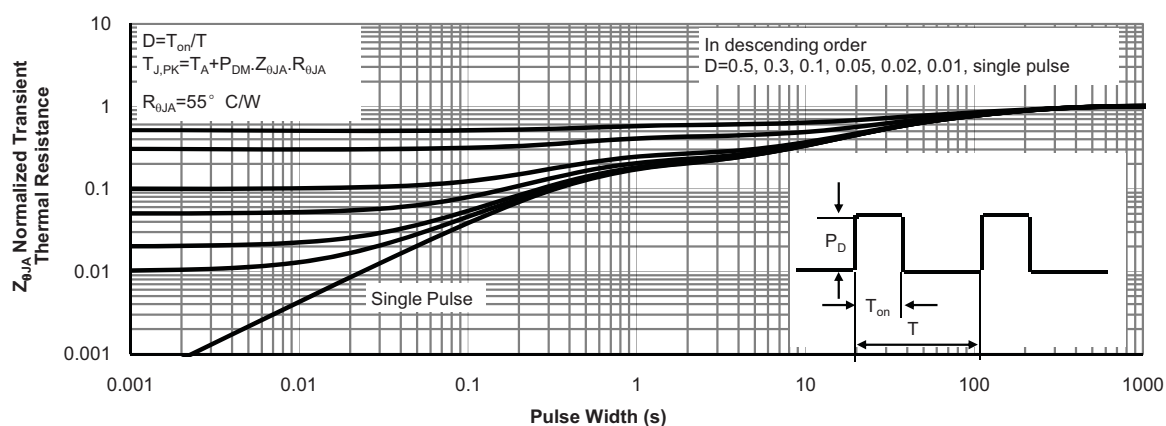


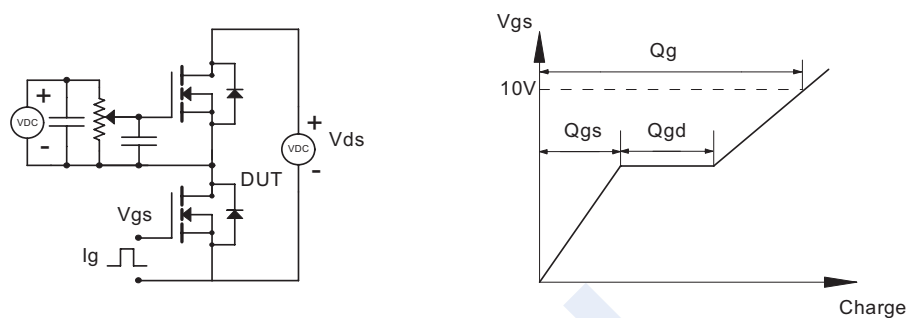
Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

N-Channel MOSFET

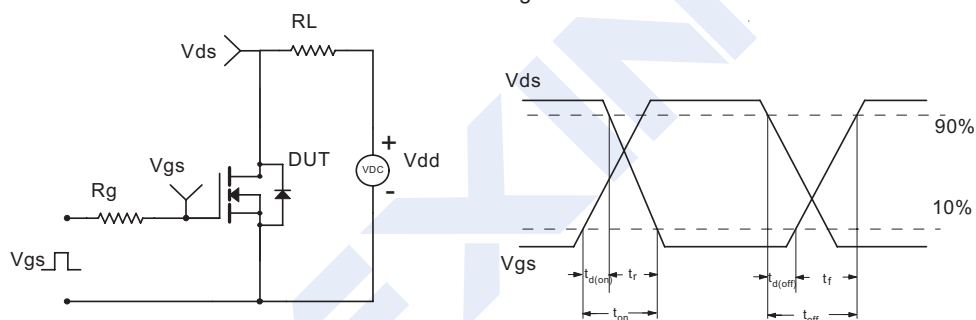
AON6512 (KON6512)

■ Typical Characteristics

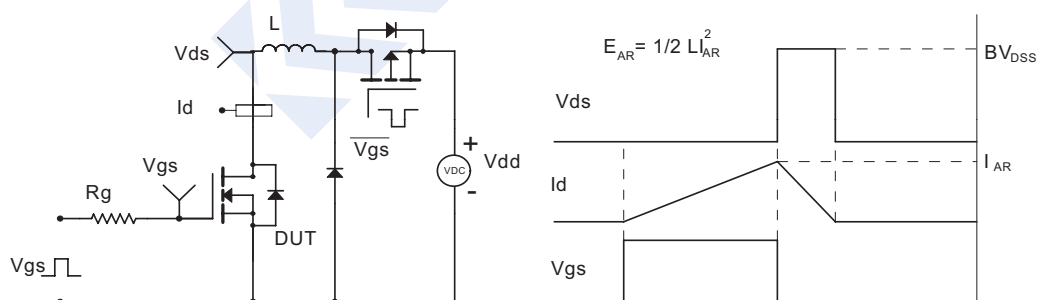
Gate Charge Test Circuit & Waveform



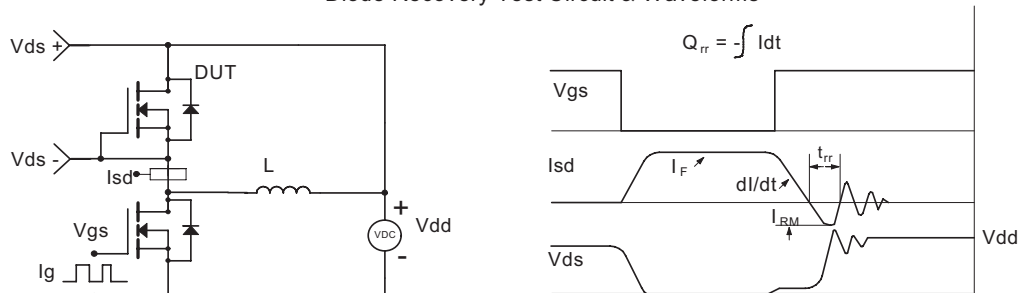
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



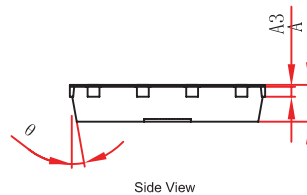
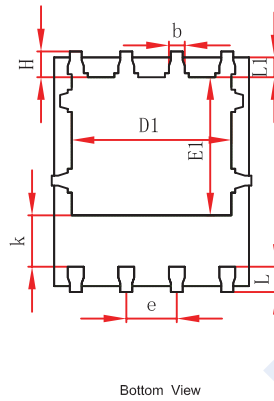
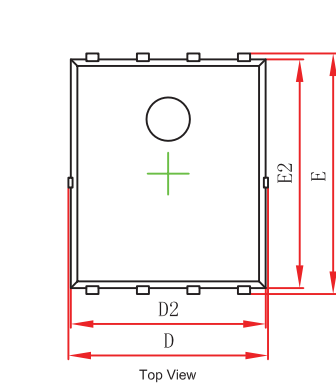
Diode Recovery Test Circuit & Waveforms



N-Channel MOSFET

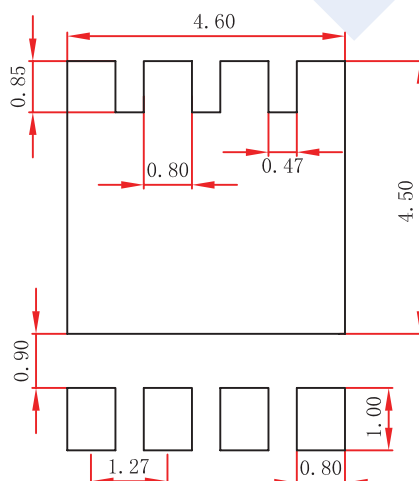
AON6512 (KON6512)

■ DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.