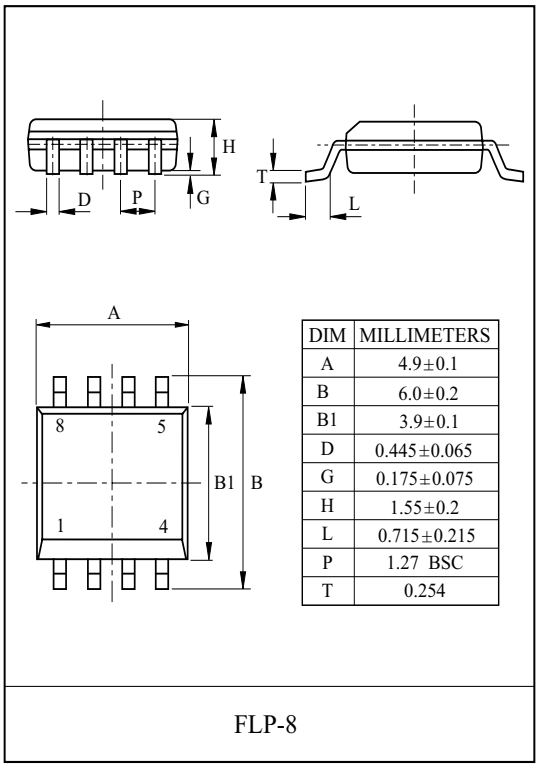
KMA5D8DP20Q

Dual P-CH Trench MOSFET

General Description

Battery Packs and Battery-powered portable equipment applications. It's mainly suitable for use as a load switch in battery powered applications and protection in battery packs.



DIM	MILLIMETERS
A	4.9±0.1
B	6.0±0.2
B1	3.9±0.1
D	0.445±0.065
G	0.175±0.075
H	1.55±0.2
L	0.715±0.215
P	1.27 BSC
T	0.254

FLP-8

FEATURES

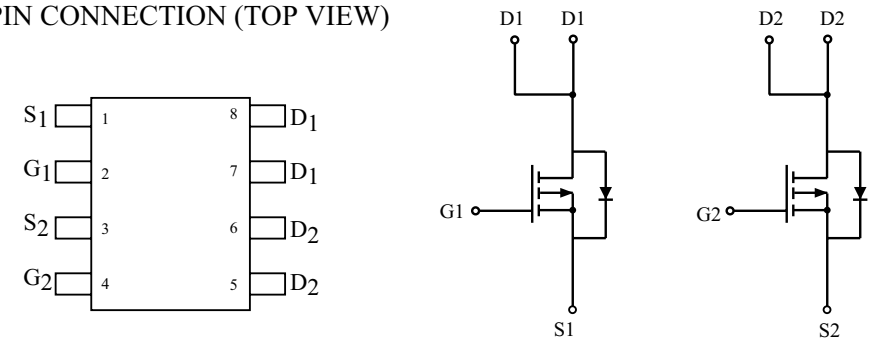
- V_{DSS}=-20V, I_D=-5.8A.
- Drain-Source ON Resistance.
  : $R_{DS(ON)}$=36mΩ (Max.) @ V_{GS}=-4.5V.
  : $R_{DS(ON)}$=62mΩ (Max.) @ V_{GS}=-2.5V.

MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current	DC	I_D *	-5.8	A
	Pulsed (Note2)	I_{DP}	-24	
Drain Power Dissipation	Ta=25℃	P_D *	2.0	W
	Ta=100℃		0.8	
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55~150	℃
Thermal Resistance, Junction to Ambient		R_{thJA} *	62.5	℃/W

* : Surface Mounted on 1"×1" Board, t≤10sec.

PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25℃)

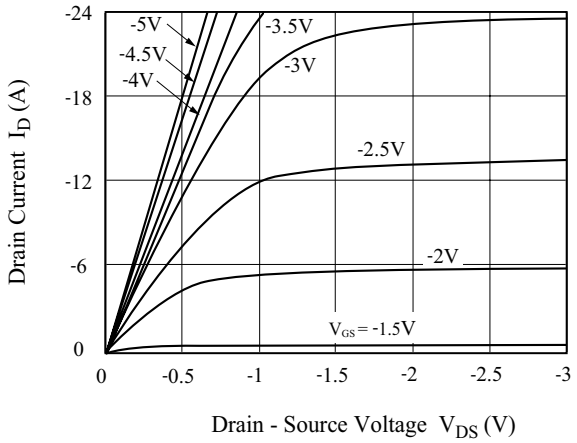
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250㎂, V_{GS}=0V,	-20	-	-	V
Drain Cut-off Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V,	-	-	-1	㎂
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=-250㎂	-0.6	-	-	V
Gate Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-5.8A (Note 2)	-	29	36	mΩ
		V_{GS}=-2.5V, I_D=-4.4A (Note 2)	-	49	62	
Dynamic (Note 3)						
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-5.8A	-	14	-	nC
Gate-Source Charge	Q_{gs}	V_{GS}=-4.5V	-	2.3	-	
Gate-Drain Charge	Q_{gd}	(Fig.1)	-	5.5	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=-10V,	-	10	-	ns
Turn-on Rise time	t_r	R_L=1.69Ω, R_G=6Ω	-	37	-	
Turn-off Delay time	$t_{d(off)}$	(Fig.2)	-	36	-	
Turn-off Fall time	t_f		-	52	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	V_{GS} < V_{th} (Note 1)	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	I_S=-5.8A, V_{GS}=0V (Note 2)	-	-	-1.5	V

Note 1) Based on thermal dissipation from junction to ambient while mounted on a 1" ×1" PCB Board.

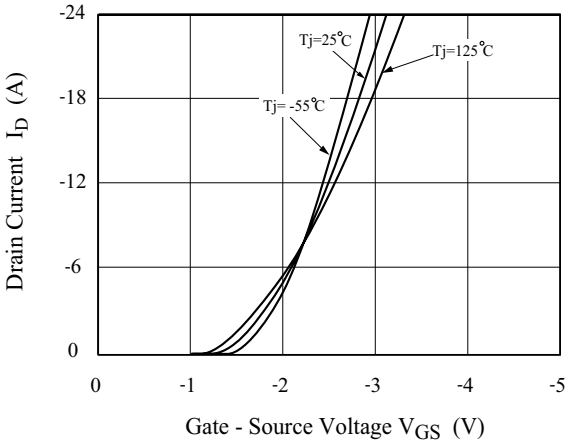
Note 2) Pulse test : Pulse width ≤300㎲.

Note 3) Guaranteed by design, not subject to production testing.

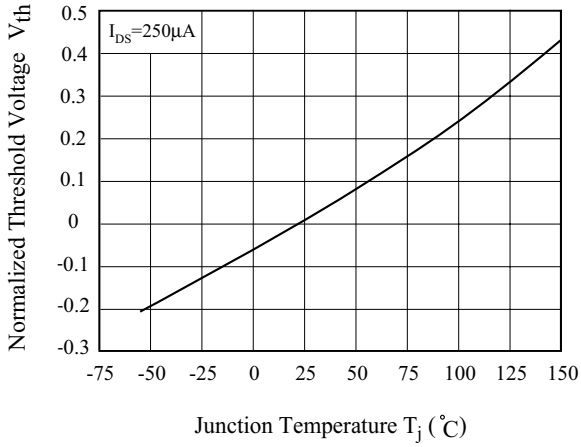
I_D - V_{DS}



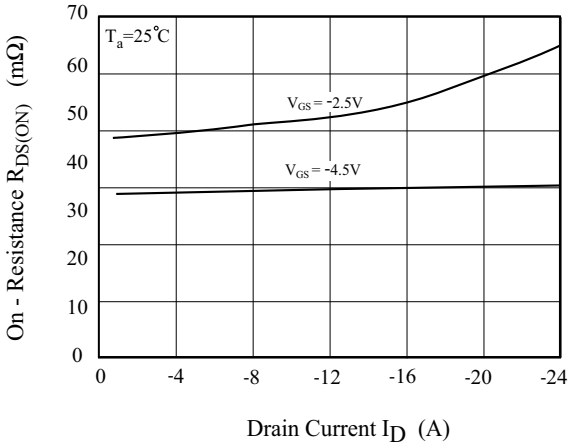
I_D - V_{GS}



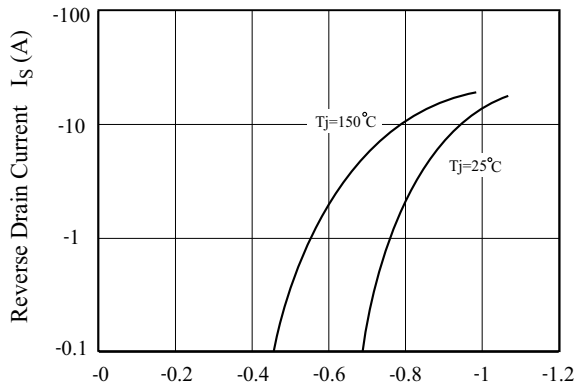
V_{th} - T_j



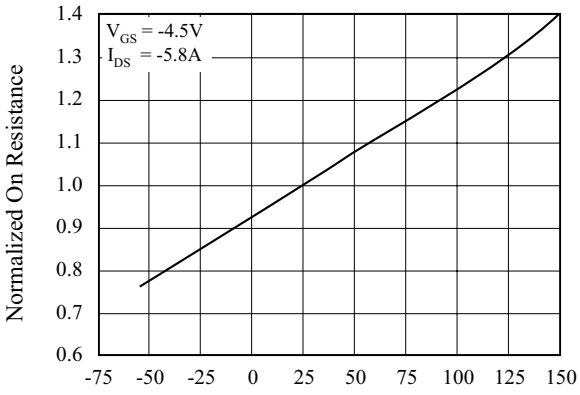
$R_{DS(ON)}$ - I_D



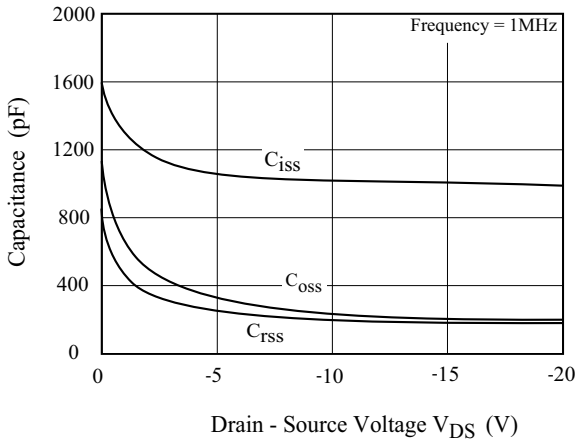
I_S - V_{SD}



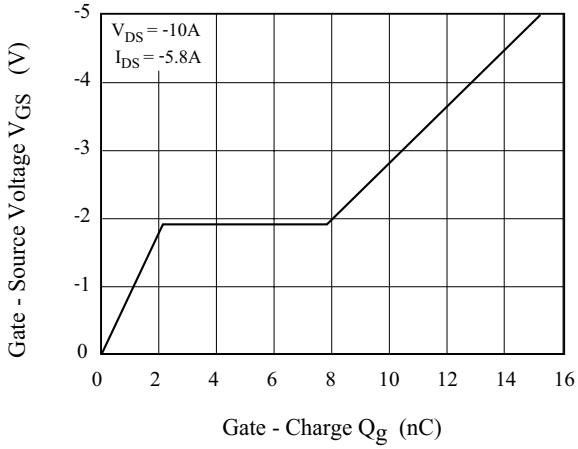
$R_{DS(ON)}$ - T_j



C - V_{DS}



Q_g - V_{GS}



R_{th}

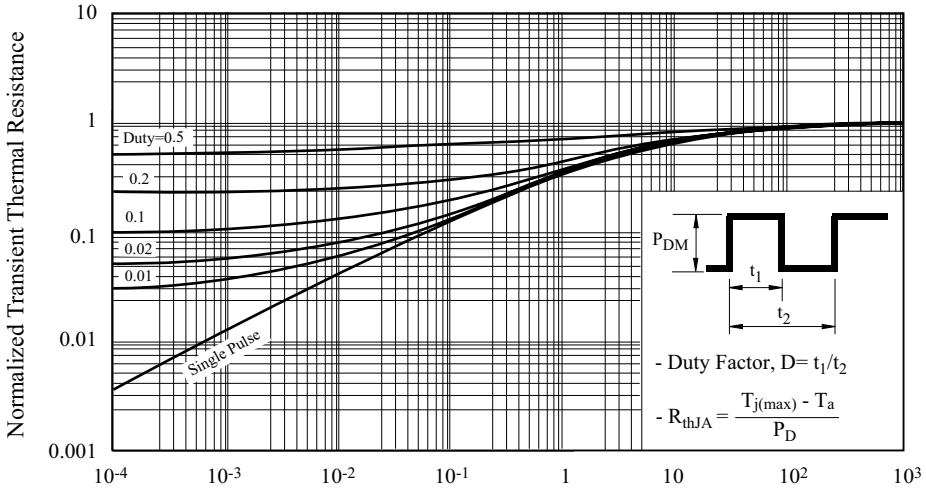


Fig. 1 Gate Charge

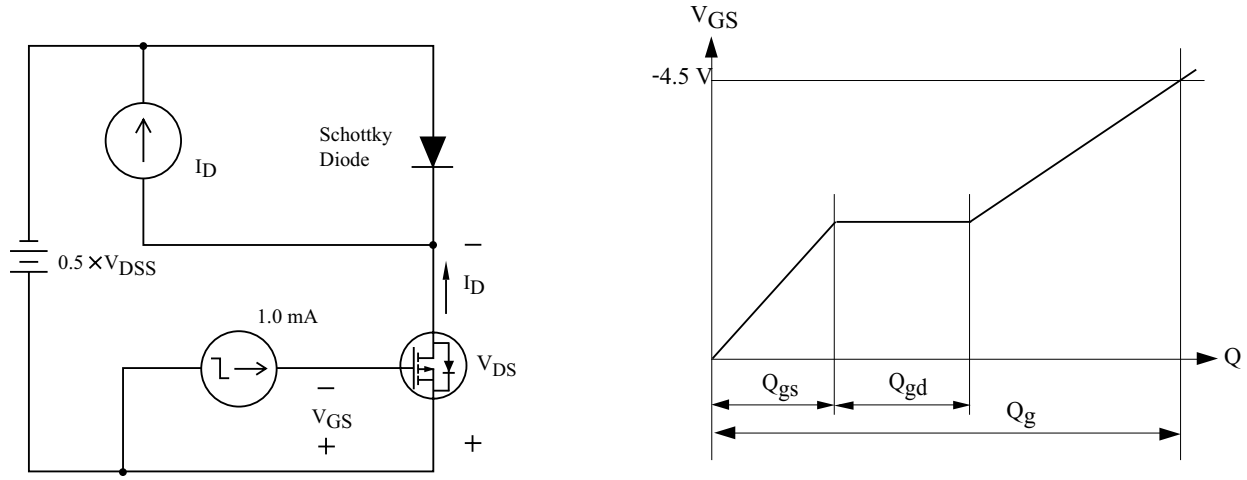


Fig. 2 Resistive Load Switching