SAMSUNG SEMICONDUCTOR, INC.

KM6816

2,048 × 8 BIT CMOS STATIC RAM

GENERAL DESCRIPTION

The KM6816 is a 2048 word by 8 bit static random access memory fabricated with Samsung's high performance CMOS silicon-gate technology.

The KM6816 design has been optimized for high performance applications, such as microcomputer systems, where fast access time and ease of use are required.

The KM6816 has an output enable pin for precise control of the data outputs. It also has a chip enable pin for the minimum current power down mode. It is particularly well suited for battery backup novolatile memory applications.

The KM6816 is fully static and may be maintained in any state indefinitely. All inputs and outputs are TTL compatible. It operates on a single +5 volt supply. It is available in a standard 24-pin DIP with the Jedec Standard pinout and is also compatible with 2K×8 EPROM and ROM pinouts.

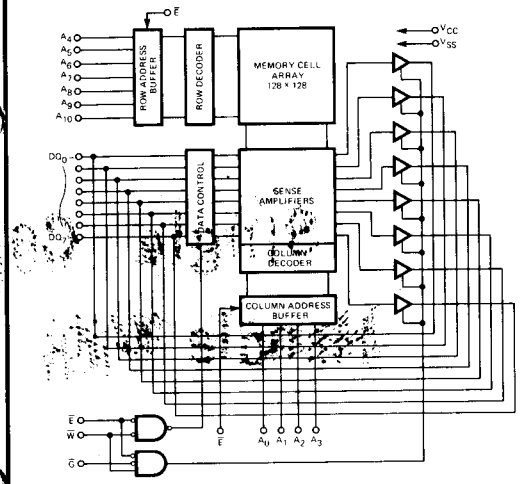
FEATURES

- Industry standard 24 pin DIP.
- Single +5V±10% power supply
- Low standby power: 55μW (max)
- Performance range

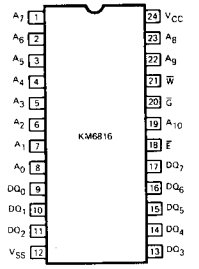
TYPE	t_{AA}	t_{OE}	t_{RC}	UNIT
KM6816-15	150	75	150	ns
KM6816-20	200	100	200	ns

- No clock or Timing Strobe Required
- Standard 16K EPROM/ROM Compatible
- Directly TTL compatible
- Equal access and cycle time
- Three-State data output

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



A_0-A_{10}	Address Input
DQ_0-DQ_7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS (See Note)

RATING	SYMBOL	VALUE	UNITS
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.3 to V_{CC} +0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.3 to +7.0	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{OPR}	0	25	+70	°C
Input High Voltage, all Inputs	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC CHARACTERISTICS (T_A =0°C to 70°C, V_{CC} =5V±10%, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING POWER SUPPLY CURRENT	I_{CC1}	$\overline{E}$ =V_{IL}, $I_{I/O}$ =O mA ($\overline{G}$ =V_{IH})		15	30	mA
AVERAGE OPERATING CURRENT	I_{CC2}	Min Cycle Duty =100%		25	40	mA
STANDBY POWER SUPPLY CURRENT	I_{SB}	$\overline{E}$ =V_{CC} other pins OV to V_{CC}			10	µA
Input Leakage Current	I_{IL}	V_{IN} =OV to V_{CC}			1.0	µA
Output Leakage Current	I_{OL}	$\overline{E}$ =V_{IH}, $V_{I/O}$ =OV to V_{CC}			1.0	µA
Output High Voltage	V_{OH}	I_{OH} = −1.0 mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} =2.1 mA	—	—	0.4	V

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ PIN	REF. CYCLE
H	X	X	NOT SELECTED	HIGH Z	STANDBY
L	L	H	READ	Q	READ CYCLE
L	L	L	WRITE	D	WRITE CYCLE (1)
L	H	L	WRITE	D	WRITE CYCLE (2)

CAPACITANCE (T_A =25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}	V_I =OV	—	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ =OV	—	—	8	pF

NOTES: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=5V±10% unless otherwise specified.)

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Time	10 ns
Input/Output Timing Level	1.5V
Output Load	100pF+1TTL

READ CYCLE

PARAMETER	SYMBOL		KM6816-15		KM6816-20		UNIT
	ALTERNATE	*STANDARD	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	TAVAV	150		200		ns
Address Access Time	t_{AA}	TAVQV		150		200	ns
Chip Enable Access Time	t_{ACS}	TELQV		150		200	ns
Output Low Z from $\overline{E}$	t_{CLZ}	TELQX	15		20		ns
Output Enable to Output Valid	t_{OE}	TGLQV		75		100	ns
Output Low Z from $\overline{E}$	t_{OLZ}	TGLQX	15		20		ns
Output High Z from $\overline{G}$	t_{OHZ}	TGHQZ	0	50	0	60	ns
Output High Z from $\overline{E}$	t_{CHZ}	TEHQZ	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	TAVQX	15		20		ns

WRITE CYCLE

PARAMETER	SYMBOL		KM6816-15		KM6816-20		UNIT
	ALTERNATE	*STANDARD	MIN	MAX	MIN	MAX	
White Cycle Time	t_{WC}	TAVAV	150		200		ns
Chip Enable Low to $\overline{W}$ High	t_{CW}	TELWH	110		135		ns
Address Valid to End of Write	t_{AW}	TAVWH	110		135		ns
Address Set Up Time	t_{AS}	TAVWL	0		5		ns
Write Pulse Width	t_{WP}	TWLWH	110		140		ns
Write Recovery Time	t_{WR}	TWHAX	20		35		ns
Write to Output in High Z	t_{WHZ}	TWLQZ		40		60	ns
Data Set-Up Time	t_{DW}	TDVWH	70		80		ns
Data Hold from Write	t_{DH}	TWHDX	10		10		ns
Write High to Output Valid	t_{OW}	TWHQV	15		20		ns
Output High Z from $\overline{G}$	t_{OHZ}	TGHQZ		40		60	ns

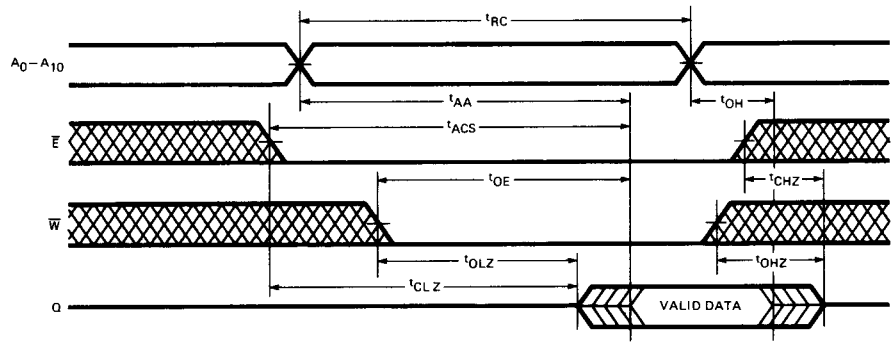
See notes on following page

* Those symbols described in **IEEE Std, 662-1980: IEEE Standard Terminology for Semiconductor memory.**

NOTES:
1. A write operation occurs during the time (tWP) when both $\overline{E}$ and $\overline{W}$ are low.
2. t_{WR} is measured from the earlier of $\overline{E}$ and $\overline{W}$ going high at the end of the Write Cycle.
3. During this period the DQ pins are in the output low-Z state. Input signals of opposite phase to the output must not be applied during this time because buss contention can occur.
4. If the $\overline{E}$ high to low transition occurs simultaneously with or after the $\overline{W}$ high to low transition, the output will remain in the high impedance state.
5. If $\overline{E}$ is low during this period, the DQ pins are in the output low-Z state. Input signals of opposite phase to the output must not be applied during this time because buss contention can occur.

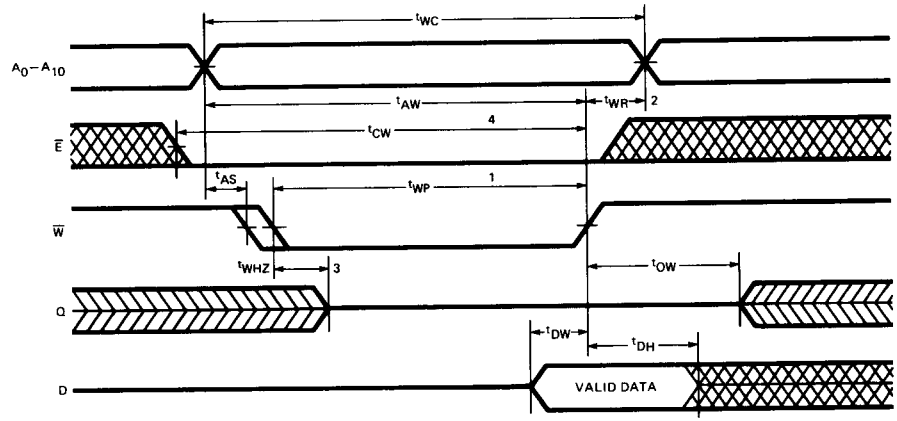
TIMING DIAGRAMS

READ CYCLE
($\overline{W}=V_{IH}$)

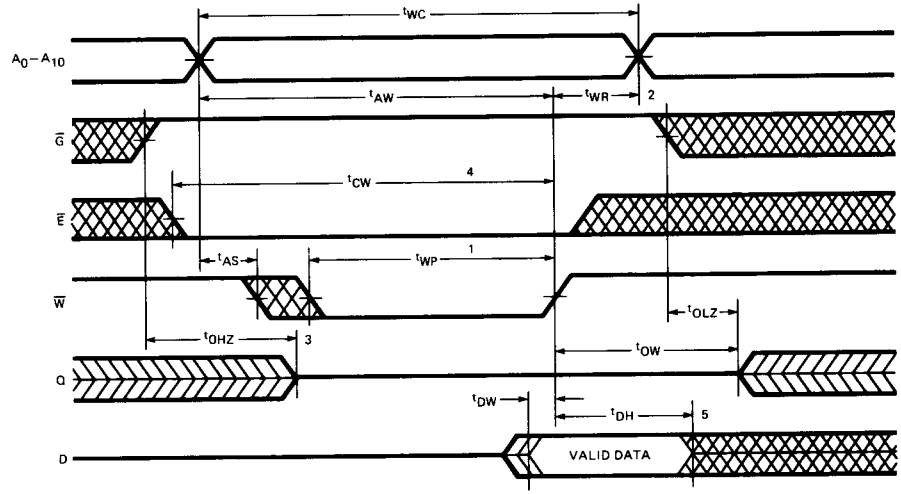


TIMING DIAGRAMS (Continued)

WRITE CYCLE (1)
($\overline{G}$ = V_{IL})

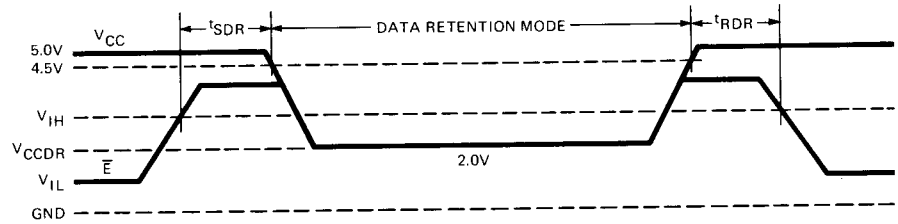


WRITE CYCLE (2)



LOW VOLTAGE DATA HOLD CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DR}	V_{IN}=OV to V_{CC}, $\overline{CS}$=V_{CC}	2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=2.0V V_{IN}=OV to V_{CC}, $\overline{CS}$=V_{CC}			10	μA
Data Retention Set-Up Time	t_{SDR}		0			ns
Data Retention Hold Time	t_{RDR}		t_{RC}			ns



NOTES

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7