256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.

This 256Kx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C256B/BL (5V, 512 Ref.)
  - KM416V256B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	325	495
-7	290	440
-8	270	415

- Refresh cycles

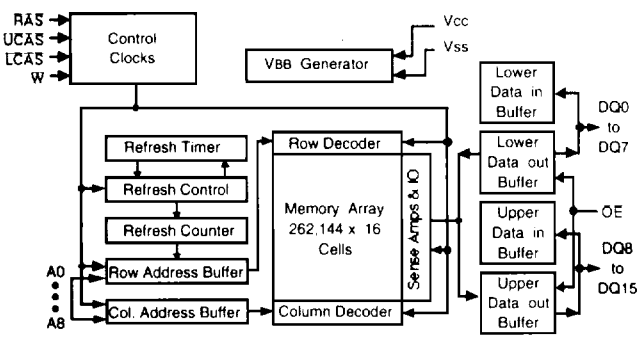
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C256B	5V	512	8ms	128ms
V256B	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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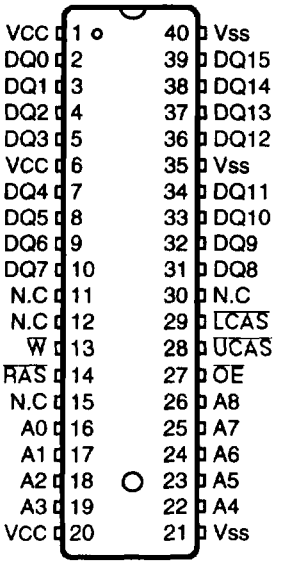
SAMSUNG ELECTRONICS

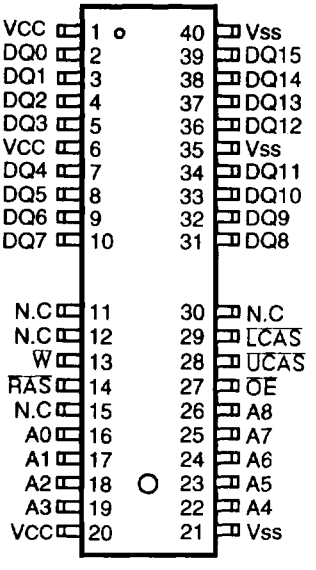
PIN CONFIGURATION (Top Views)

• KM416C/V256BJ



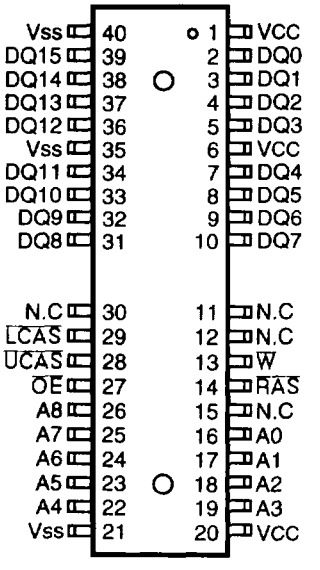
(SOJ)

• KM416C/V256BT



(TSOP(II)-Forward Type)

• KM416C/V256BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V256B	KM416C256B	
I_{CC1}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	75	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	75	mA
I_{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	55	mA
		-8	50	50	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	75	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$= 0.2V

Din = Don't care, T_{RC}= 125µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	10		10		15		15		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	10		10		15		15		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

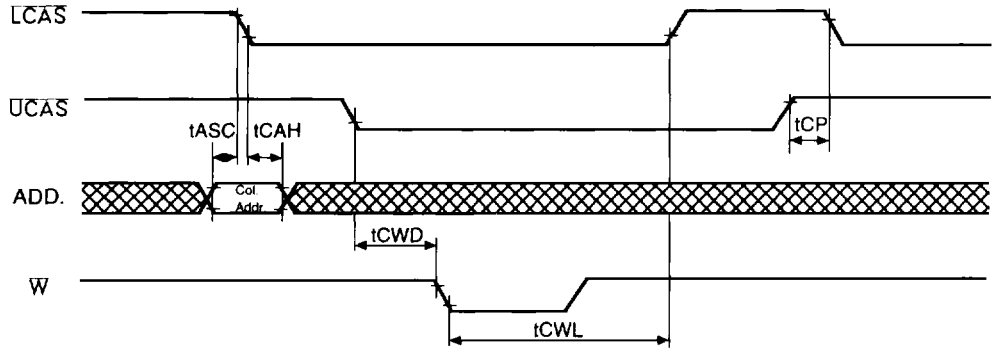
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

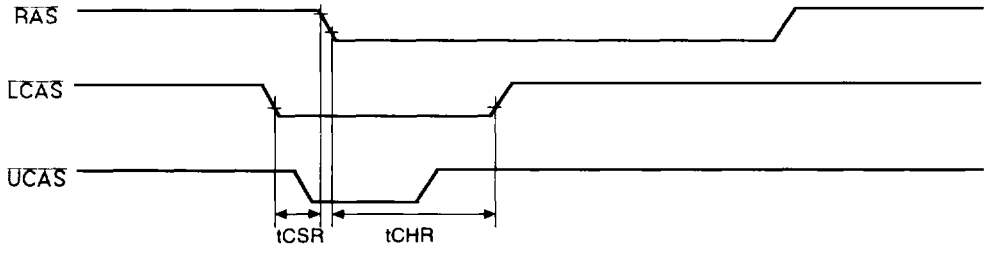
KM416C/V256B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
12. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
13. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).