32M-Bit (4Mx8 /2Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
  4,194,304 x 8(byte mode)
  2,097,152 x 16(word mode)
- Fast access time
  Random Access Time
  3.3V Operation : 80ns(max.)
  3.0V Operation : 100ns(max.)
  2.5V Operation : 120ns(max.)
- Supply voltage
  KM23V32000B(E)TY : 2.7V ~ 3.6V
  KM23S32000B(E)TY : 2.3V ~ 2.7V
- Current consumption
  Operating : 30mA(max.)
  Standby : 30㎂(max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
  -. KM23V(S)32000B(E)TY : 48-TSOP1-1218

GENERAL DESCRIPTION

The KM23V32000B(E)TY and KM23S32000B(E)TY are fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 x 8 bit(byte mode) or as 2,097,152 x 16 bit(word mode) depending on BHE voltage level.(See mode selection table)

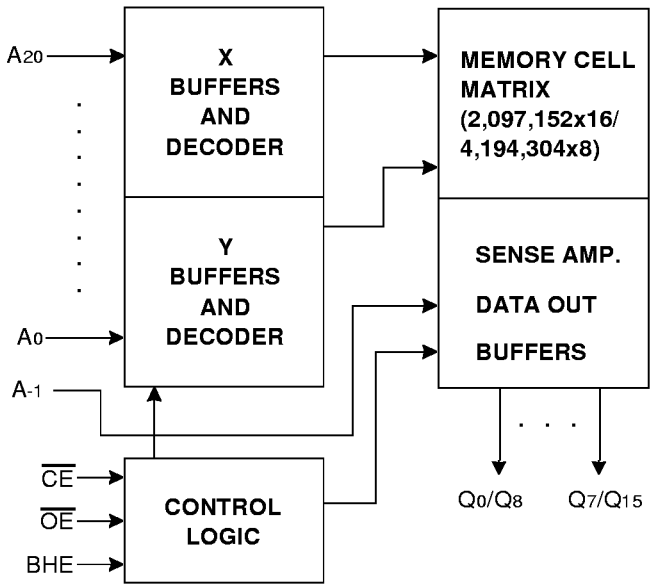
This device operates with low power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V32000B(E)TY and KM23S32000B(E)TY are packaged in a 48-TSOP1.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_{20}	Address Inputs
Q_0 - Q_{14}	Data Outputs
Q_{15} /A_{-1}	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
V_{SS}	Ground
N.C	No Connection

Preliminary

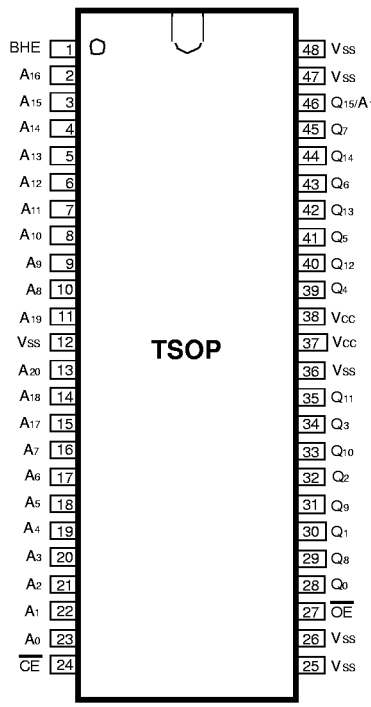
KM23V32000B(E)TY/KM23S32000B(E)TY CMOS MASK ROM

32M-Bit (4Mx8 /2Mx16) CMOS MASK ROM

PRODUCT INFORMATION

Product	Operating Temp Range	Vcc Range	Speed (ns)
KM23V32000BTY	0¡ ~ 70¡	3.3V/3.0V	80/100
KM23S32000BTY		2.5V	120
KM23V32000BETY	-20¡ ~ 85¡	3.3V/3.0V	80/100
KM23S32000BETY		2.5V	120

PIN CONFIGURATION



KM23V32000B(E)TY
KM23S32000B(E)TY

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	Remark
Voltage on Any Pin Relative to VSS	VIN	-0.3 to +4.5	V	-
Temperature Under Bias	TBIAS	-55 to +150	¡	-
Storage Temperature	TStg	-55 to +150	¡	-
Operating Temperature	Ta	0 to +70	¡	KM23V32000BTY KM23S32000BTY
		-20 to +85	¡	KM23V32000BETY KM23S32000BETY

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7/3.0	3.0/3.3	3.3/3.6	V
		2.3	2.5	2.7	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol		Test Conditions		Min	Max	Unit
Operating Current	I_{CC}		$\overline{CE}$=$\overline{OE}$=V_{IL} all outputs open	V_{CC}=3.3V¡ 0.3V	-	30	mA
				V_{CC}=3.0V¡ 0.3V	-	25	mA
				V_{CC}=2.5V¡ 0.2V	-	20	mA
Standby Current(TTL)	I_{SB1}	KM23V32000B(E)TY	$\overline{CE}$=V_{IH}, all outputs open		-	500	㎂
		KM23S32000B(E)TY			-	100	㎂
Standby Current(CMOS)	I_{SB2}	KM23V32000B(E)TY	$\overline{CE}$=V_{CC}, all outputs open		-	30	㎂
		KM23S32000B(E)TY			-	5	㎂
Input Leakage Current	I_{LI}		V_{IN}=0 to V_{CC}		-	10	㎂
Output Leakage Current	I_{LO}		V_{OUT}=0 to V_{CC}		-	10	㎂
Input High Voltage, All Inputs	V_{IH}				2.0	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}	KM23V32000B(E)TY			-0.3	0.6	V
		KM23S32000B(E)TY			-0.3	0.4	V
Output High Voltage Level	V_{OH}	KM23V32000B(E)TY	I_{OH} = -400㎂		2.4	-	V
		KM23S32000B(E)TY	I_{OH} = -400㎂		2.0	-	V
Output Low Voltage Level	V_{OL}		I_{OL} = 2.1mA		-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q_0~Q_{15} : Dout	Active
		L	Input	Operating	Q_0~Q_7 : Dout Q_8~Q_{14} : Hi-Z	Active

CAPACITANCE (T_A =25¡ , f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS (Vcc = 3.3V/3.0V¡ 0.3V, Vcc = 2.5V¡ 0.2V, unless otherwise noted.)

TEST CONDITIONS

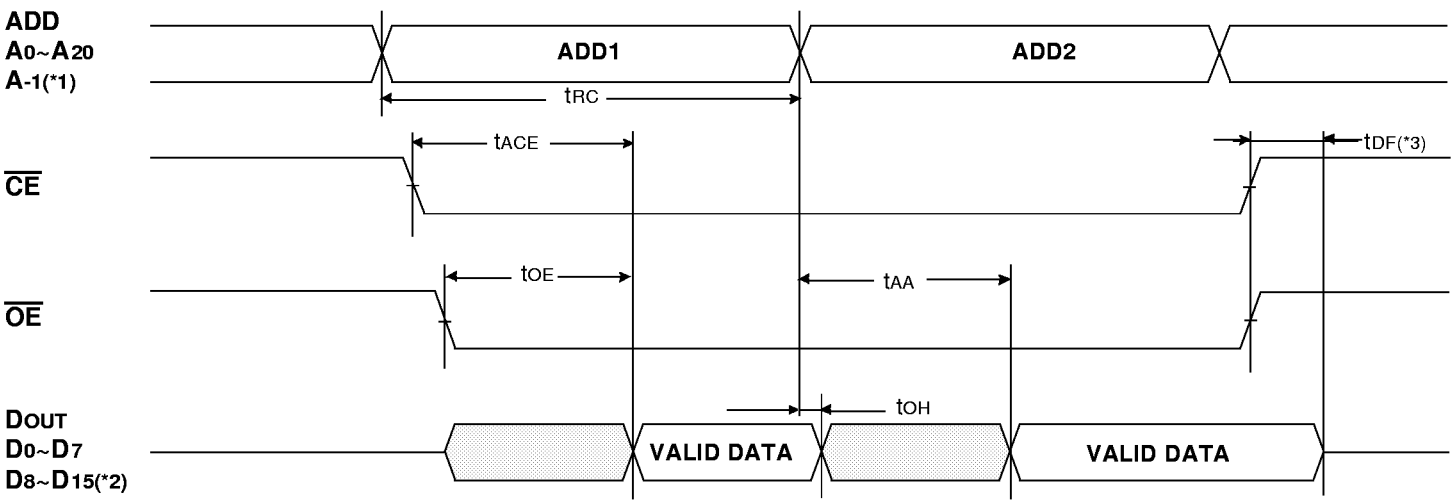
Item	Value
Input Pulse Levels	0.45V to 2.4V(at Vcc=3.3V/3.0V)
	0.4V to 2.2V (at Vcc=2.5V)
Input Rise and Fall Times	10ns
Input and Output timing Levels	1.5V (at Vcc=3.3V/3.0V)
	1.1V (at Vcc=2.5V)
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Item	Symbol	Vcc = 3.3V¡ 0.3V		Vcc = 3.0V¡ 0.3V		Vcc = 2.5V¡ 0.2V		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	80		100		120		ns
Chip Enable Access Time	tACE		80		100		120	ns
Address Access Time	tAA		80		100		120	ns
Output Enable Access Time	tOE		30		50		60	ns
Output or Chip Disable to Output High-Z	tDF		20		20		20	ns
Output Hold from Address Change	tOH	0		0		0		ns

TIMING DIAGRAM

READ



NOTES : *1. Byte Mode only. A-1 is Least Significant Bit Address.(BHE = VIL)
*2. Word Mode only.(BHE = VIH)
*3. tDF is defined as the time at which the outputs achieve the open circuit condition and is not referenced to VOH or VOL level.