

KLM - 064MA - 16B

This module designed for light emitting display device. Organize with 16 × 32 matrix combination with 512 of each Red, Green LED Chips, for indoor use.

FEATURES

- Active display size : 64mm × 128mm
- Dot size : $\phi 3$
- Dot pitch : 4mm
- Display color : RED, GREEN, AMBER(Mixed color)
- Duty rate : 1/16
- Dot matrix : 512(16 × 32)
- Weight : 150g(Typ.)
- With a simple serial - inter face.

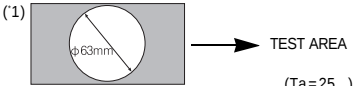
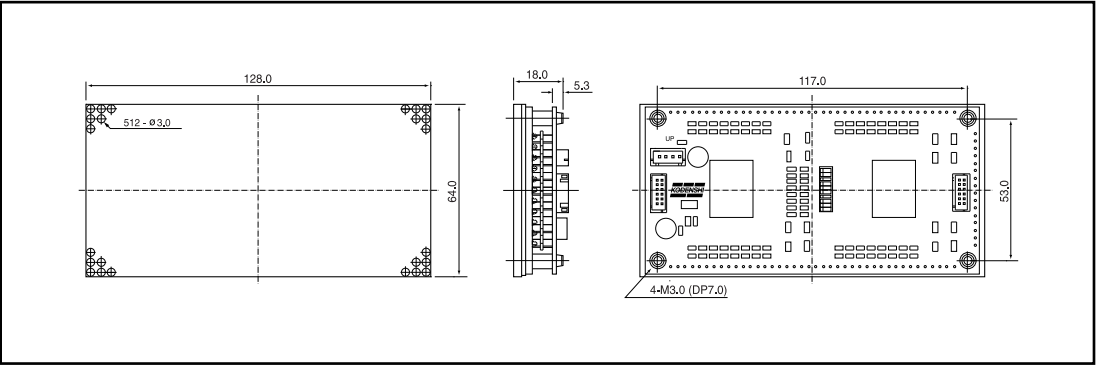
MAXIMUM RATINGS

(Ta=25)

ITEM	SYMBOL	RATING	UNIT	COND.
Power dissipation	P_D	25	W	
Supply voltage(DRIVE)	V_{DD}	6	V	
Supply voltage(LED)	V_{LED}	6	V	
Logic input power	V_{in}	- 0.5 ~ V_{DD}	V	
Junction Temp.	T_j	115		
Operating Temp.	T_{opr}	- 20 ~ + 60		
Storage Temp.	T_{stg}	- 20 ~ + 65		

DIMENSIONS

(Unit : mm)



OPTICAL CHARACTERISTICS

(Ta=25)

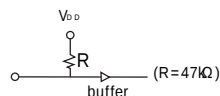
ITEM		SYMBOL	CONDITON	MIN.	TYP.	MAX.	UNIT.
Bright - ness(16× 16)	GREEN	IV_g	$V_{DD} = 5V$	-	120	-	cd/m^2
	RED	IV_r		-	100	-	
	AMBER	IV_o		-	180	-	
Dot - Balance	GREEN	IVR_g	$V_{LED} = 5V$	-	-	2	-
	RED	IVR_r		-	-	2	
	AMBER	IVR_o		-	-	2	
Emission Wavelength	GREEN	λ_p		-	565	-	nm
	RED	λ_p		-	630	-	
Spectrum half - band	GREEN	λ_g		-	25	-	nm
	RED	λ_r		-	40	-	

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*2. $V_{DD}=5V$, $V_{LED}=5V$

*PULL UP



CLASSIFICATION		NAME	STANDARD	LENGH	COMPANY	REMARK
POWER CONN.		WAFER	B 4B - XH - A	-	KST	JST C/N
INPUT SIGNAL CONN.		WAFER	B 12B - PHDSS	-	KST	JST C/N
OUTPUT SIGNAL CONN.		WAFER	B 12B - PHDSS	-	KST	JST C/N
ASS Y	POWER	HARNESS	XHP - 4P - 000(Ring type)	Option	KST	JST C/N
		HARNESS	XHP - 4P - 000(Solder type)	Option	KST	JST C/N
	SIGNAL	HARNESS	HPDR - 12VS - 000	Option	KST	JST C/N

The timing diagram illustrates the operation of the 74VHC163 4-bit binary counter. It shows the following signals and their timing relationships:

- Clock:** A periodic square wave signal.
- R-Data:** A signal that is active-low (indicated by a bubble) and is used to load a new value into the counter.
- G-Data:** A signal that is active-low (indicated by a bubble) and is used to clear the counter.
- Latch:** A signal that is active-low (indicated by a bubble) and is used to latch the current value of the counter.
- Out Enable:** A signal that is active-low (indicated by a bubble) and is used to enable the output of the counter.
- Address (A₀-A₃):** A 4-bit binary address signal.

Key timing parameters are labeled on the diagram:

- t_{SU} : Setup time for R-Data and G-Data before the clock edge.
- t_{HD} : Hold time for R-Data and G-Data after the clock edge.
- t_{LATCH} : Latch time for the Latch signal.
- t_{OE} : Out Enable delay from the Latch signal to the Out Enable signal.
- t_{LOC} : Load output delay from the R-Data signal to the Out Enable signal.
- $t_{SET(A)}$: Set delay from the R-Data signal to the output.
- $t_{CLR(A)}$: Clear delay from the G-Data signal to the output.
- $t_{0(A)}$: Output delay from the clock edge to the output.
- $t_{0(L-E)}$: Load enable delay from the Latch signal to the output.

NO	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
1	CLOCK FREQUENCY	f_{cl}	-	-	40	MHz
2	CLOCK CYCLE	$1/f_{cl}$	25	-	-	ns
3	CLOCK - LATCH TIME	$t_{dl}(C-L)$	25	-	-	ns
4	LATCH PULSE WIDTH	t_{wst}	25	-	-	ns
5	ENABLE - LATCH TIME	$t_{dl}(E-L)$	0	-	-	ns
6	DATA SETUP TIME	t_{sd}	6	-	-	ns
7	DATA HOLD TIME	t_{hd}	6	-	-	ns
8	ADDRESS - ENABLE TIME	$t_{dl}(A-E)$	25	-	-	ns
9	LATCH - ADDRESS TIME	$t_{dl}(L-A)$	0	-	-	ns
10	LATCH - ENABLE TIME	$t_{dl}(L-E)$	0	-	-	ns
11	ENABLE CYCLE	t_{oc}	-	-	1	ms