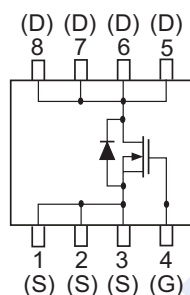


N-Channel MOSFET

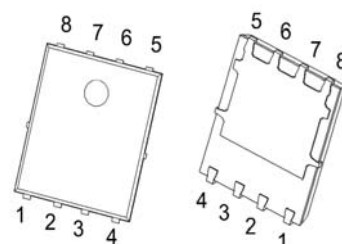
SI7738DP (KI7738DP)

■ Features

- $V_{DS} (V) = 150V$
- $I_D = 30 A$
- $R_{DS(ON)} \leq 38m\Omega$ ($V_{GS} = 10V$)



DFN5x6-8(PDFNWB5x6-8L)

■ Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ C$)	$T_C = 25^\circ C$	I_D	30 ^a	A
	$T_C = 70^\circ C$		26	
	$T_A = 25^\circ C$		7.7 ^{b,c}	
	$T_A = 70^\circ C$		6.2 ^{b,c}	
Pulsed Drain Current		I_{DM}	60	
Continuous Source-Drain Diode Current	$T_C = 25^\circ C$	I_S	30 ^a	A
	$T_A = 25^\circ C$		4.5 ^{b,c}	
Single Pulse Avalanche Current	$L = 0.1mH$	I_{AS}	30	mJ
Single Pulse Avalanche Energy		E_{AS}	45	
Maximum Power Dissipation	$T_C = 25^\circ C$	P_D	96	W
	$T_C = 70^\circ C$		62	
	$T_A = 25^\circ C$		5.4 ^{b,c}	
	$T_A = 70^\circ C$		3.5 ^{b,c}	
Thermal Resistance.Junction- to-Ambient ^{b,f}	$t \leq 10s$	R_{thJA}	23	$^\circ C/W$
Thermal Resistance.Junction- to-Case (Drain)	Steady state	R_{thJC}	1.3	
Soldering Recommendations (Peak Temperature) ^{d,e}			260	$^\circ C$
Junction Temperature		T_J	150	
Storage Temperature Range		T_{stg}	-55 to 150	

Notes: a.Package limited. b.Surface Mounted on 1" x 1" FR4 board. c. $t = 10 s$.

d.The DFN5X6-8 is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed to ensure adequate bottom side solder interconnection.

e.Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f.Maximum under Steady State conditions is 65 $^\circ C/W$.

N-Channel MOSFET

SI7738DP (KI7738DP)

■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D=250\mu\text{A}$		200		$\text{mV}/^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-10		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=150\text{V}$, $V_{GS}=0\text{V}$			1	μA
		$V_{DS}=150\text{V}$, $V_{GS}=0\text{V}$, $T_C=55^\circ\text{C}$			10	
Gate-Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2		4	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{V}$, $V_{GS}=10\text{V}$	30			A
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=7.7\text{A}$			38	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}$, $I_D=7.7\text{A}$		22		S
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=75\text{V}$, $f=1\text{MHz}$		2100		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			45		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=75\text{V}$, $R_L=12\Omega$, $I_D=6.2\text{A}$, $V_{GEN}=10\text{V}$, $R_g=1\Omega$		15	25	ns
Turn-On Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Turn-Off Fall Time	t_f			10	15	
Total Gate Charge	Q_g	$V_{DS}=75\text{V}$, $I_D=7.7\text{A}$, $V_{GS}=10\text{V}$		35	53	nC
Gate Source Charge	Q_{gs}			8		
Gate Drain Charge	Q_{gd}			9		
Body Diode Reverse Recovery Time	t_{rr}	$I_F=6.2\text{A}$, $di/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$		75	115	ns
Body Diode Reverse Recovery Charge	Q_{rr}			245	370	nC
Body Diode Reverse Recovery Fall Time	t_a			58		ns
Body Diode Reverse Recovery Rise Time	t_b			17		
Maximum Body-Diode Continuous Current	I_S	$T_C=25^\circ\text{C}$			30	A
Maximum Body-Diode Current (Pulsed)	I_{SM}				30	
Diode Forward Voltage	V_{SD}	$I_{SD}=6.2\text{A}$, $V_{GS}=0\text{V}$			1.2	V

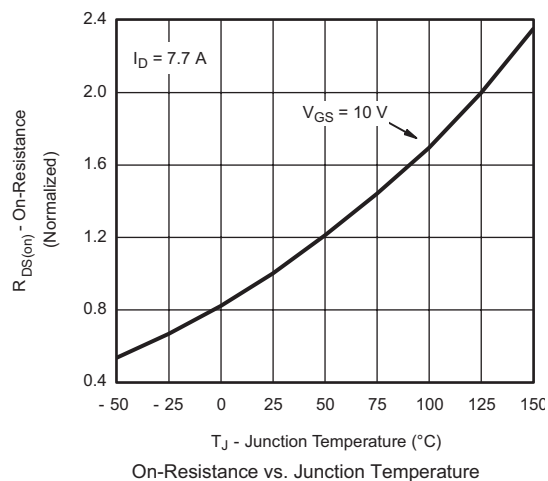
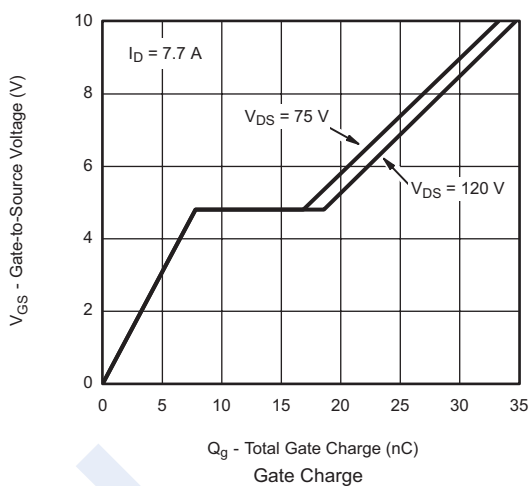
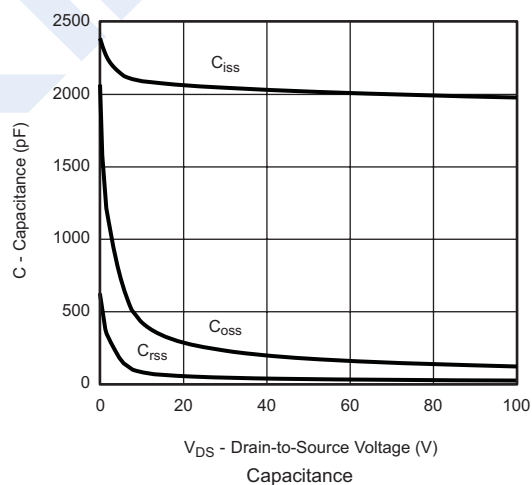
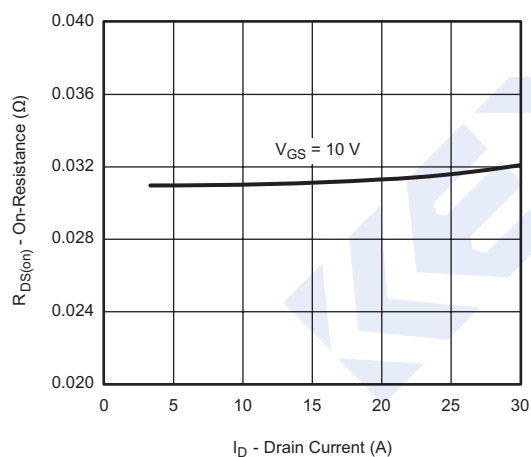
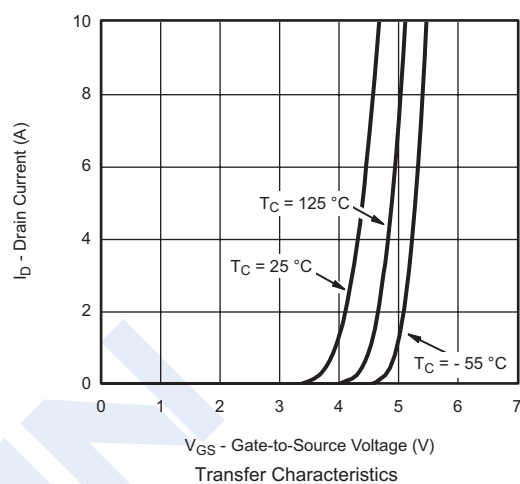
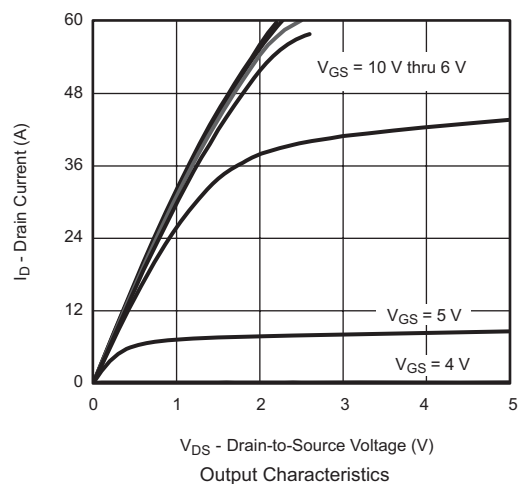
Notes: a. Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

N-Channel MOSFET

SI7738DP (KI7738DP)

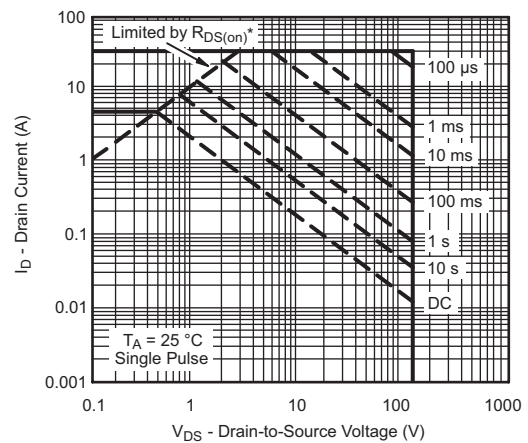
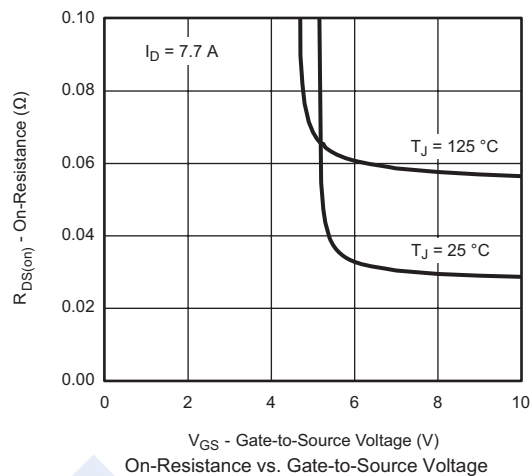
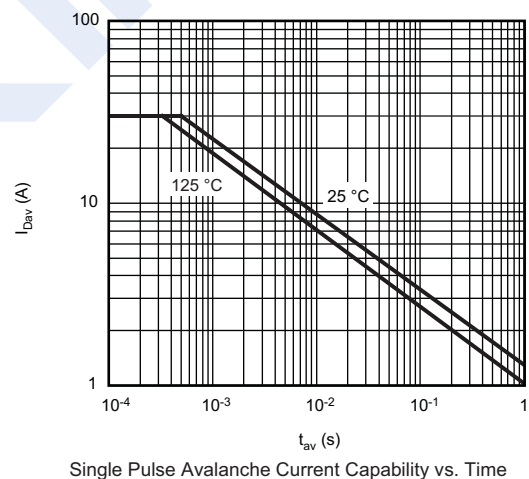
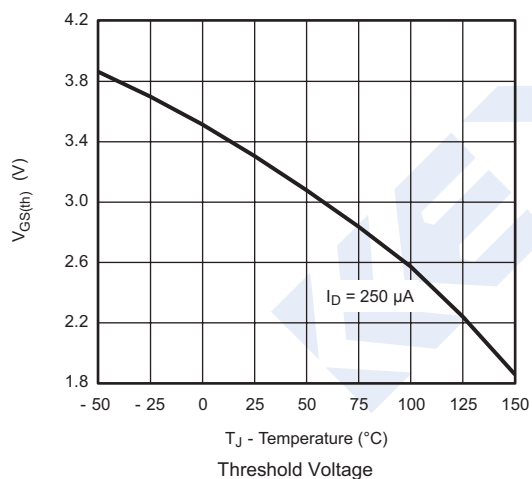
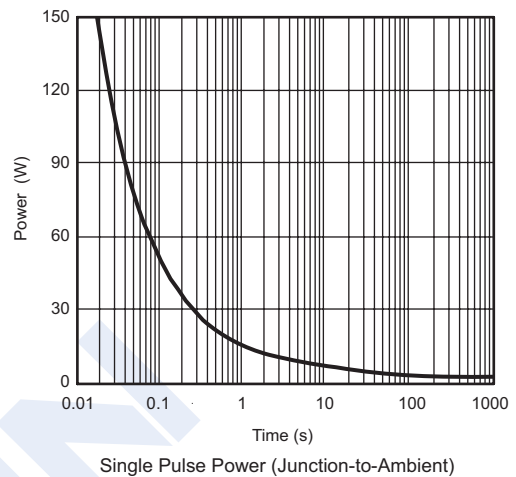
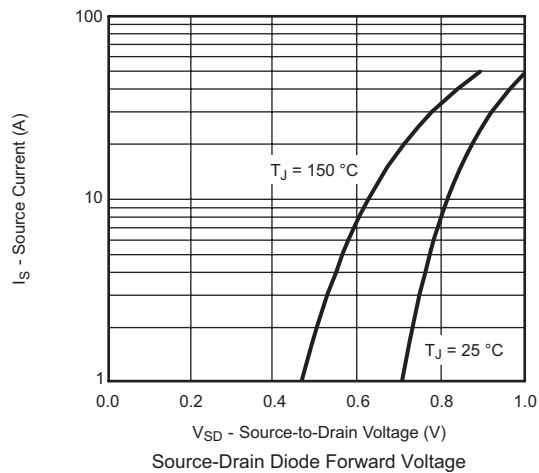
■ Typical Characteristics 25°C unless otherwise noted



N-Channel MOSFET

SI7738DP (KI7738DP)

■ Typical Characteristics 25°C unless otherwise noted

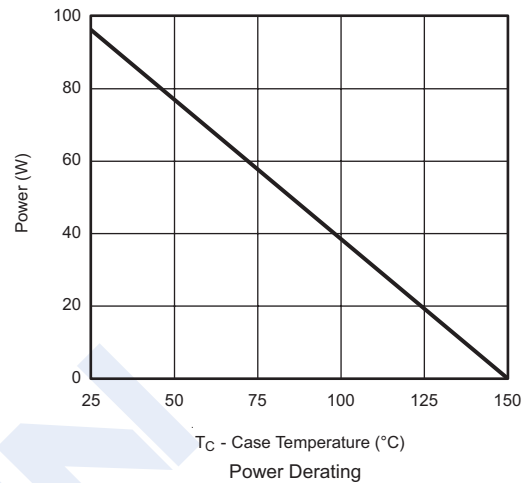
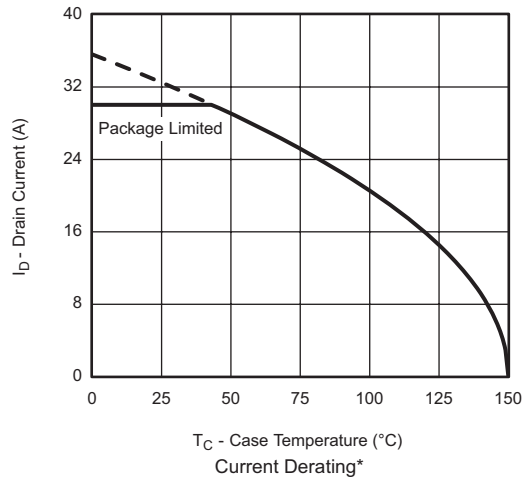


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

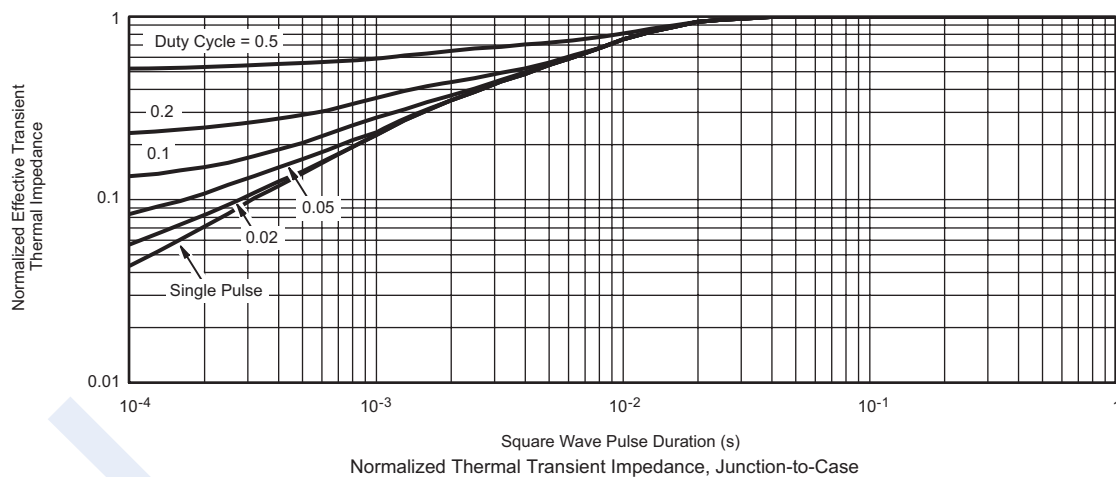
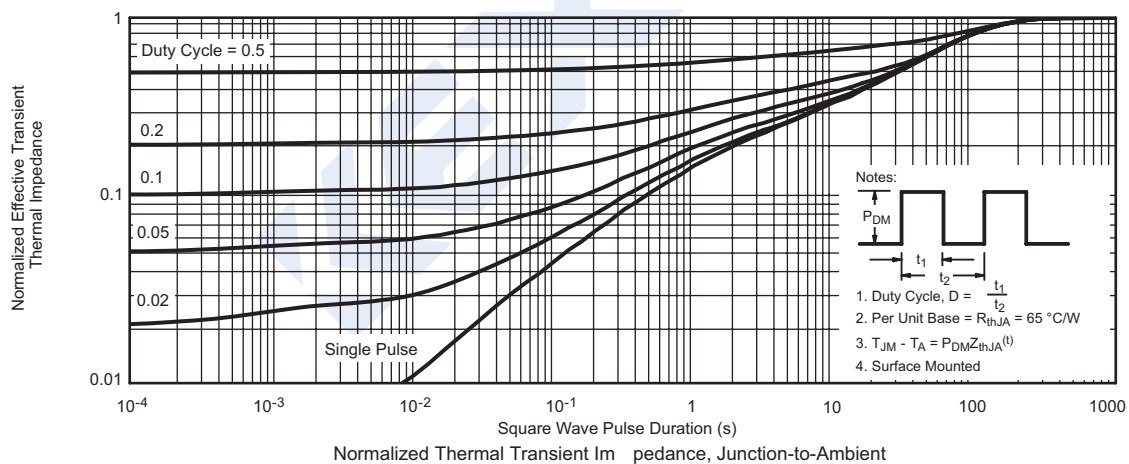
N-Channel MOSFET

SI7738DP (KI7738DP)

■ Typical Characteristics 25°C unless otherwise noted



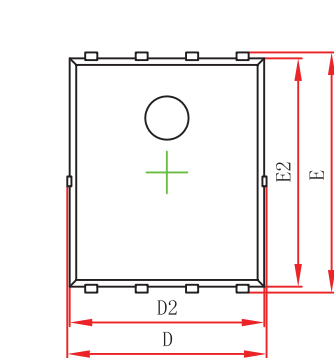
* The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



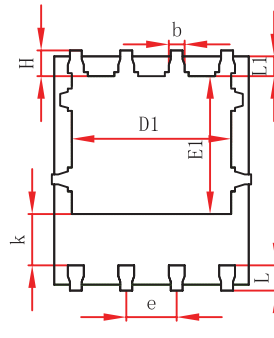
N-Channel MOSFET

SI7738DP (KI7738DP)

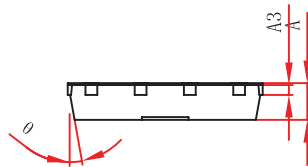
■ DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Top View
[顶视图]



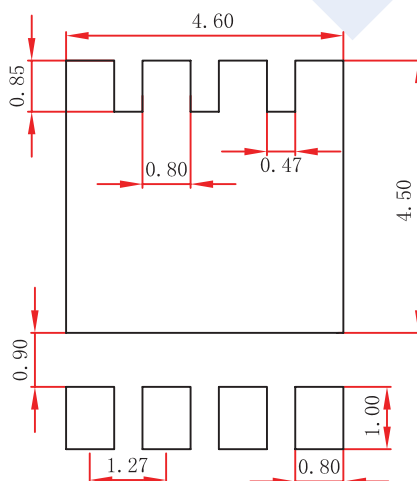
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.