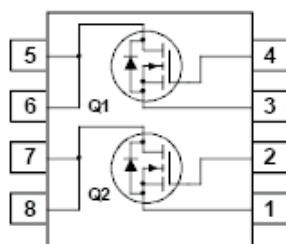
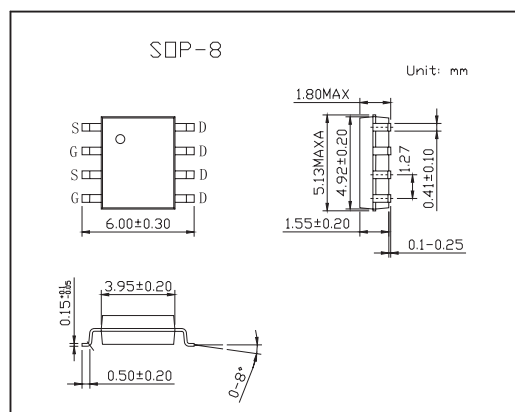


100V Dual N-Channel PowerTrench MOSFET

KDS3912

■ Features

- 3 A, 100 V. $R_{DS(ON)} = 125\text{m}\Omega$ @ $V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 135\text{m}\Omega$ @ $V_{GS} = 6\text{ V}$
- Low gate charge (14 nC typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DS}	100	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous (Note 1a)	I_D	3	A
Drain Current Pulsed		20	A
Power Dissipation for Dual Operation	P_D	1.6	W
Power Dissipation for Single Operation (Note 1a)	P_D	1	W
Power Dissipation for Single Operation (Note 1b)		0.9	
Power Dissipation for Single Operation (Note 1c)		0.9	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	$^\circ\text{C/W}$

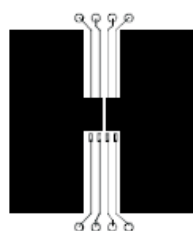
KDS3912

■ Electrical Characteristics Ta = 25°C

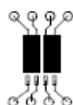
Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Single Pulse Drain-Source Avalanche Energy	W _{DSS}	Single Pulse, V _{DD} =50V, I _D =3A(Not 2)			90	mJ
Maximum Drain-Source Avalanche Current	I _{AR}	(Not 2)			3.0	A
Drain-Source Breakdown Voltage	B _V DSS	V _{GS} = 0 V, I _D = 250 μA	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		108		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			10	μA
Gate-Body Leakage, Forward	I _{GSSF}	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I _{GSSR}	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	2.5	4	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		-6		mV/°C
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 3 A		92	125	mΩ
		V _{GS} = 6 V, I _D = 2.8 A		98	135	
		V _{GS} = 10 V, I _D = 3 A, T _J = 125°C		175	250	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 10V	10			A
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 3A		11		S
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1.0 MHz		632		pF
Output Capacitance	C _{oss}			40		pF
Reverse Transfer Capacitance	C _{rss}			20		pF
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		8.5	17	ns
Turn-On Rise Time	t _r			2	4	ns
Turn-Off Delay Time	t _{d(off)}			23	37	ns
Turn-Off Fall Time	t _f			4.5	9	ns
Total Gate Charge	Q _g	V _{DS} = 50 V, I _D = 3 A, V _{GS} = 10 V (Note 2)		14	20	nC
Gate-Source Charge	Q _{gs}			2.4		nC
Gate-Drain Charge	Q _{gd}			3.8		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				1.3	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.3 A (Not 2)		0.76	1.2	V
Diode Reverse Recovery Time	t _{rr}	I _F = 3A		30		nS
Diode Reverse Recovery Charge	Q _{rr}	diF/dt = 100 A/μs (Not 2)		106		nC

Notes:

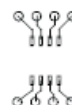
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%