SPECIFICATION
FOR
LCD Module
KD035HVTMA026-TP

MODULE:	KD035HVTMA026-TP
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2016.01.06

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2016.01.06	V1.0	ALL	FIRST ISSUE

Contents

General Description

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5TFT-LCD contains 320x480 pixels, and can display up to 65K/262K colors.

*** Features**

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

Interface: 8/9/16/18BIT 8080 MCU interface

3SPI/4SPI+16/18BIT RGB interface

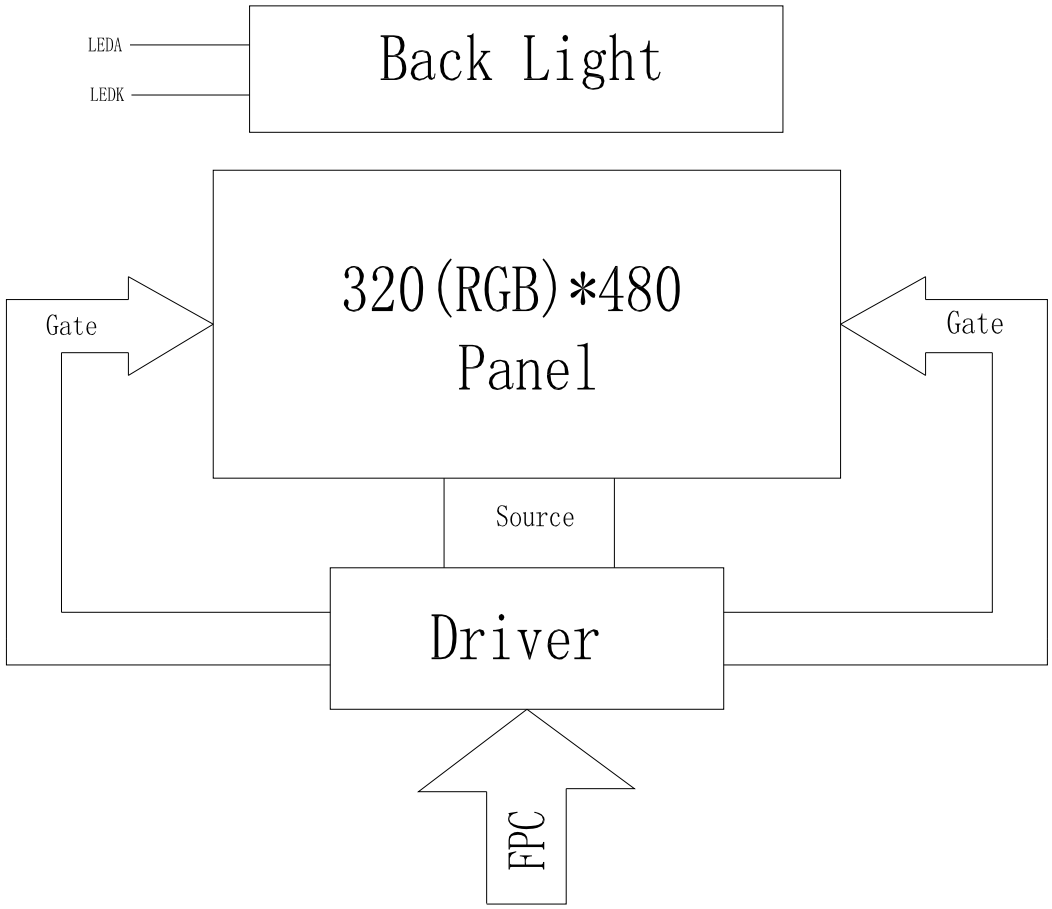
3/4-wire serial interface

eral Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44（V） (3.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	6:00	o'clock	-
Controller IC	ILI9488	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

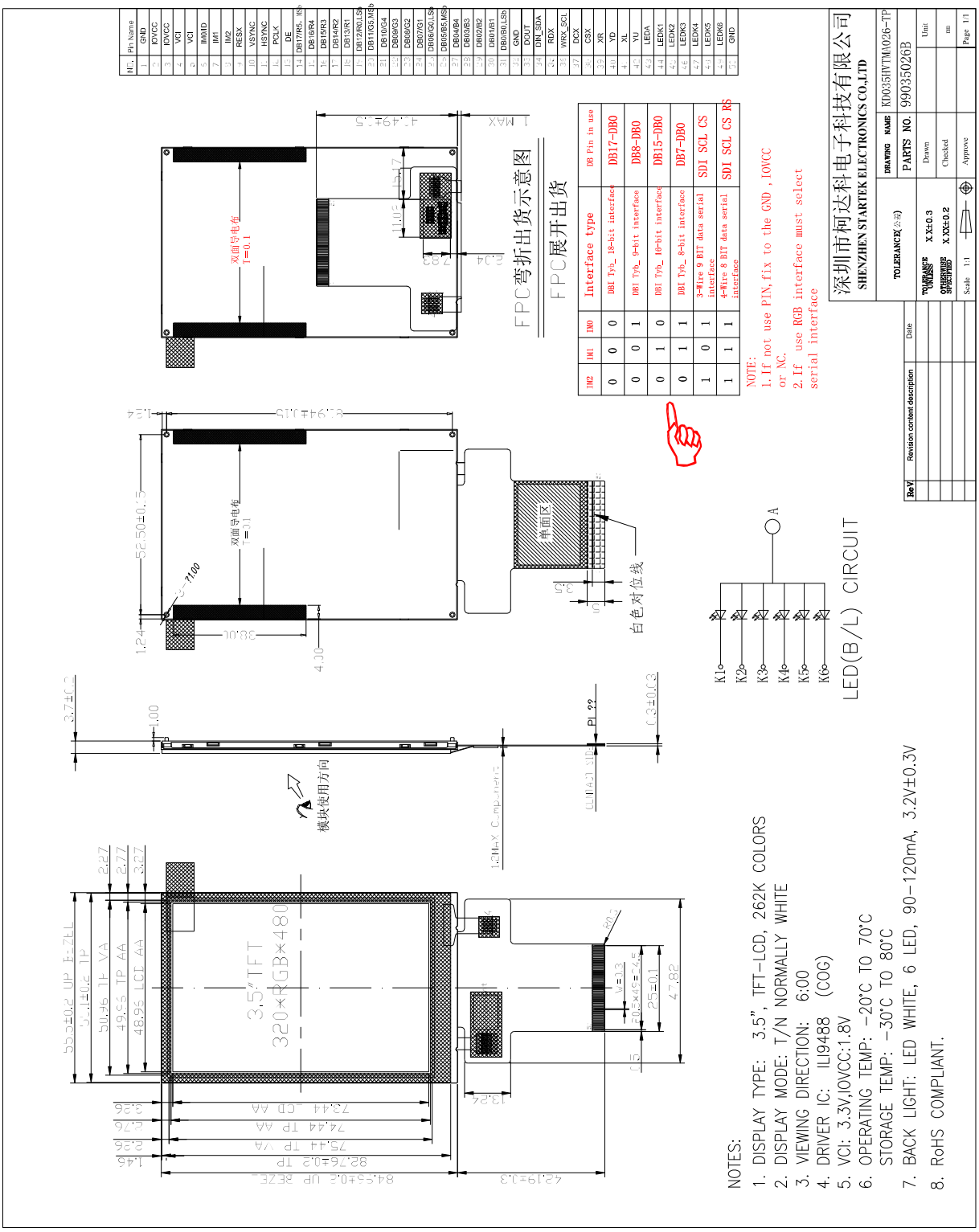
*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		55.50		mm	-
	Vertical(V)		84.96		mm	-
	Depth(D)		3.7		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	IOVCC	Supply voltage(1.8-3.3V)	P
3	IOVCC	Supply voltage(1.8-3.3V)	P
4	VCI	Supply voltage(3.3V).	P
5	VCI	Supply voltage(3.3V).	P
6	IM0/ID	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
7	IM1		I
8	IM2		I
9	RESX	This signal will reset the device and must be applied to properly initialize the chip.	I
10	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
11	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use	I
12	PCLK	Dot clock signal for RGB interface operation Fix this pin at VCI or GND when not in use.	I
13	DE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
14-31	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I
32	GND	Ground.	I
33	DOUT	Serial data output pin in serial bus system interface. If not used, please open this pin.	O
34	DIN_SDA	Serial input signal.The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND.	I
35	RDX	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
36	WRX_SCL	DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the serial	I

		interface	
37	DCX	Display data/ command selection pin	I
38	CSX	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.	I
39	XR(NC)	Touch panel Right Glass Terminal	A/D
40	YD(NC)	Touch panel Bottom Film Terminal	A/D
41	XL(NC)	Touch panel LIFT Glass Terminal	A/D
42	YU(NC)	Touch panel Top Film Terminal	A/D
43	LEDA	Anode pin of backlight	P
44	LEDK1	Cathode pin OF backlight	P
45	LEDK2	Cathode pin OF backlight	P
46	LEDK3	Cathode pin OF backlight	P
47	LEDK4	Cathode pin OF backlight	P
48	LEDK5	Cathode pin OF backlight	P
49	LEDK6	Cathode pin OF backlight	P
50	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

C. Optical specifications

Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time (By Quick)	Tr+Tf	θ= 0°	-	20	40	ms	Note 5
Contrast ratio	CR	θ= 0°	-	500	-		Note 2,6
Viewing angle	Top	CR≧10	-	60	-	deg.	Note 2,6,7
	Bottom	CR≧10	-	60	-		
	Left	CR≧10	-	70	-		
	Right	CR≧10	-	70	-		
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	Wx	θ= 0°	0.292	0.307	0.322		Note 3
	Wy		0.312	0.327	0.342		
	Rx		0.609	0.624	0.639		
	Ry		0.316	0.331	0.346		
	Gx		0.281	0.296	0.311		
	Gy		0.562	0.577	0.592		
	Bx		0.128	0.143	0.158		
	By		0.094	0.109	0.124		
NTSC			57%	60%	-		Note 3
Cross talk	Ct		-	-	2%		Note 9
Transmittance	Trans		-	5.50%	-		Note 4

Note 1: Ambient temperature = 25°C.

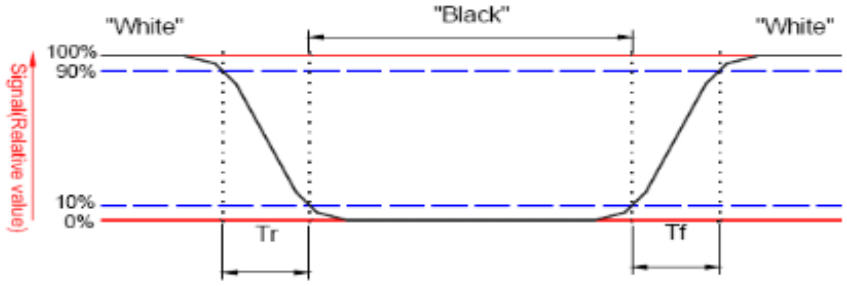
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer. The tolerance of Transmittance is ±10%.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

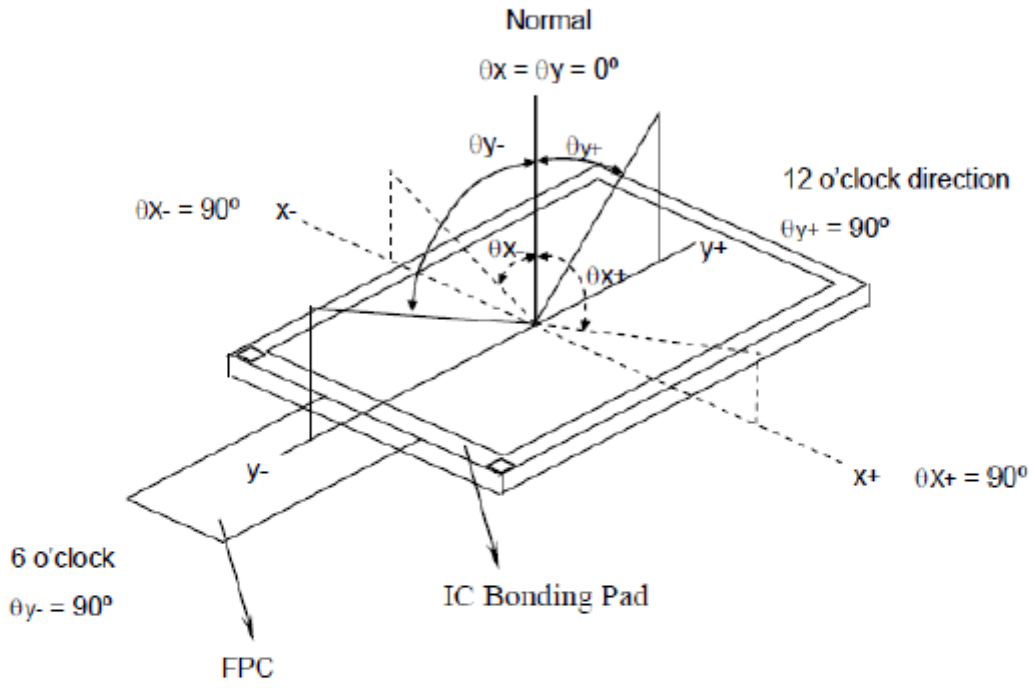


Note 6: Definition of contrast ratio:

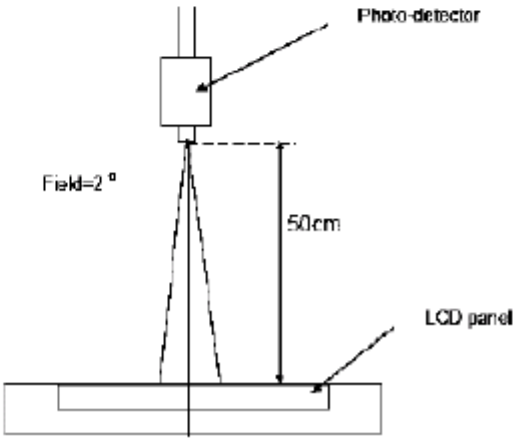
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

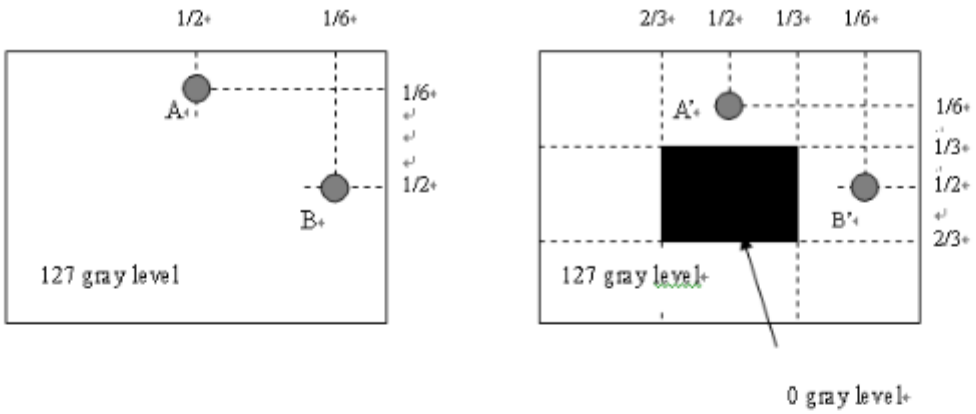
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note 9:



| LA-LA' | / LA x 100%= 2% max., LA and LA' are brightness at location A and A'

| LB-LB' | / LB x 100%= 2% max., LB and LB' are brightness at location B and B'

5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	**V**
Digital interface supple Voltage	VDDIO	-0.3	4.6	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

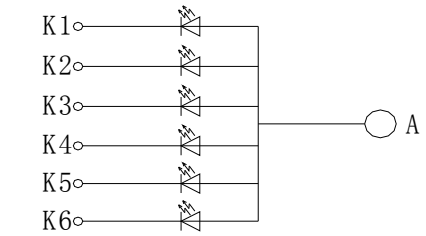
5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.4	3..3	4.2	V	
Digital interface supple Voltage	VDDIO	1.65	3.3	4.2	V	
Normal mode Current consumption	IDD	--	10	--	mA	
Level input voltage	V_{IH}	0.7V_{DDIO}		VDDIO	V	
	V_{IL}	GND		0.3V_{DDIO}	V	
Level output voltage	V_{OH}	0.8VDDIO		VDDIO	V	
	V_{OL}	GND		0.2VDDIO	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	90	120	--	mA	
Forward Voltage	V_F	2.9	3.2	3.4	V	
LCM Luminance	L_V	250	--	--	cd/m2	IF=120mA
Uniformity	AVg	80	--	--	%	



LED(B/L) CIRCUIT

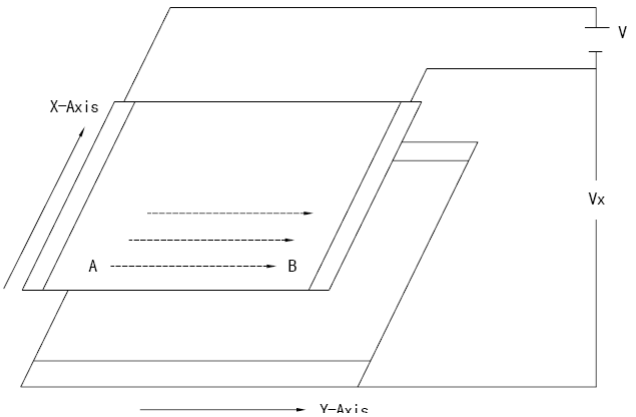
6. TP Feature

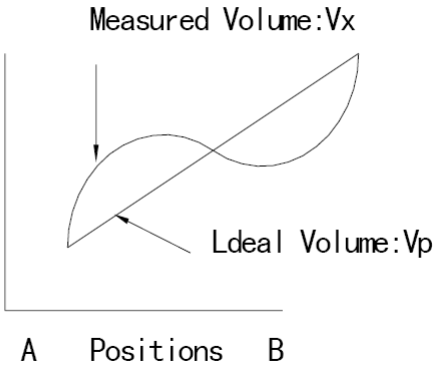
6.1 Conditions of use and storage

Item	Value(condition)	Note
Temperature range upon operation	Humidity: 20％~90％ non dew, condensation -20℃~70℃	In a simple substance
Temperature range upon storage	Humidity: 20％~90％ non dew, condensation -30℃~80℃	In a simple substance

6.2 Electrical property

Item	Value	Note
Maximum voltage	DC5V	
Resistance between terminals	X direction[Film side]:200-600Ω	
	Y direction [Glass side]:300-900Ω	
Insulation resistance	DC 25V 20MΩor above	Connect X + ～X- and Y+ ～Y-, apply 25VDC Between X and Y for perform measurements
Chattering	10 msec or below	
Rating	Voltage is DC 5V	





6.3 Mechanical property

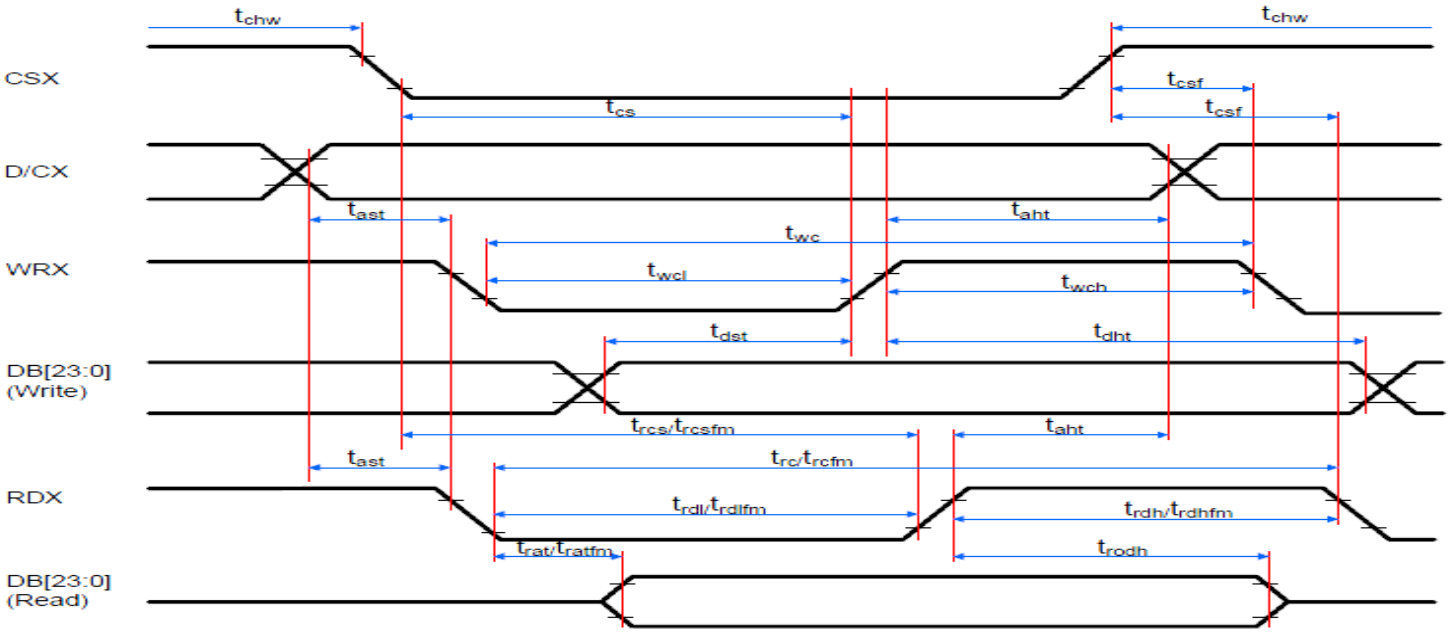
Item	Performance		Note
Input method	Used of an exclusive pen or finger		
Load upon operation	Exclusive pen	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: Stylus pen material : POM(ployacetal) . Tip : Diameter 3.0mm, SR 0.8 mm
	Finger	60-100g or below	Operations and measurement methods simulated for a finger must be carried out under the following tip conditions. Material :Silicon rubber (Hardness : 30°Hs) Tip : Diameter 12.0 mm, SR 12.5mm
Surface hardness	Pencil hardness : 3H or above		It complies with the way of test method JIS K5400.

6.4 Optical property

Item	Performance	Note
Total light transmittance	80% or above	JIS K7105
Haze	5% or below	JIS K7136
Film specification	Polished type with hard coated surface	

7. AC Characteristic

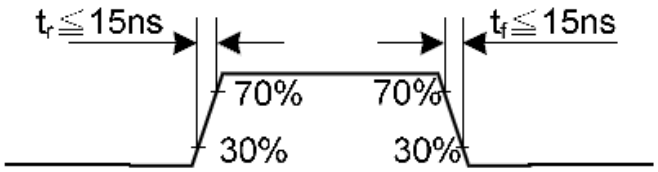
7.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- system)



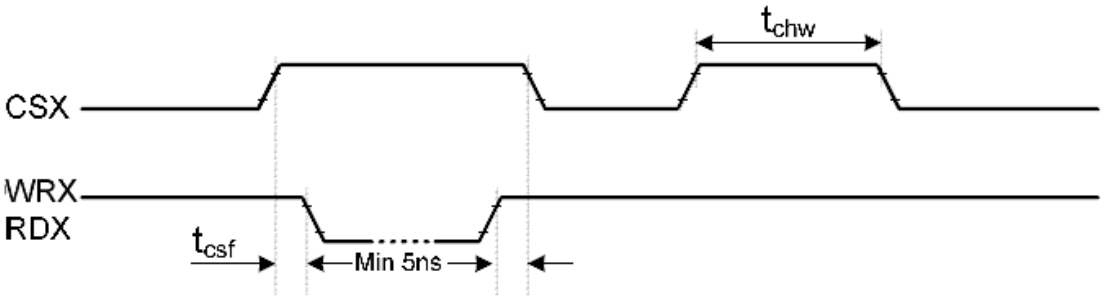
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

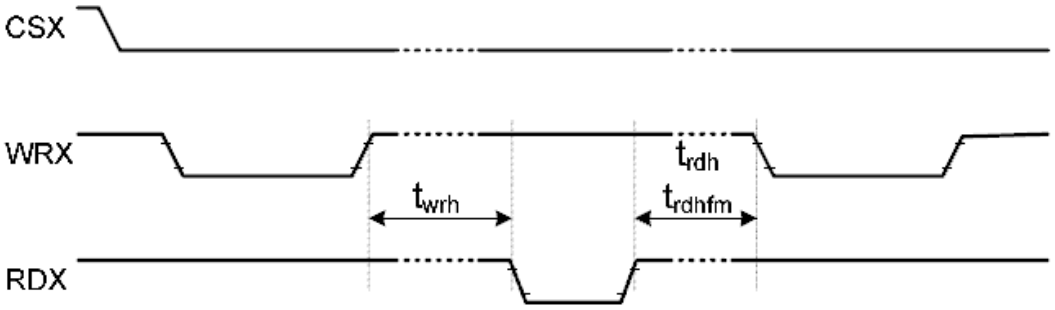
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



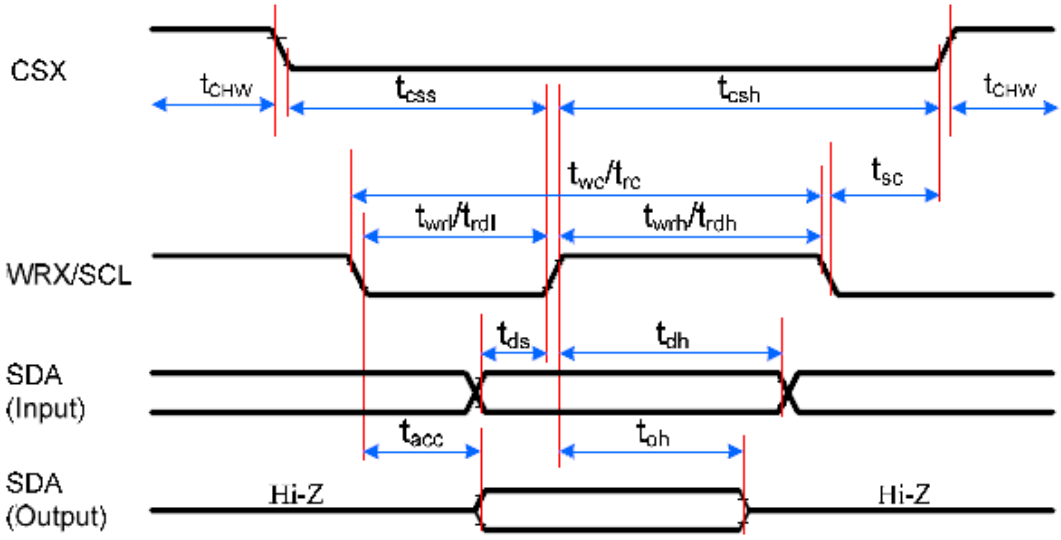
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

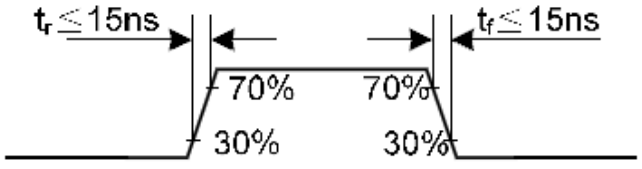


7.2 Display Serial Interface Timing Characteristics (3-line SPI system)

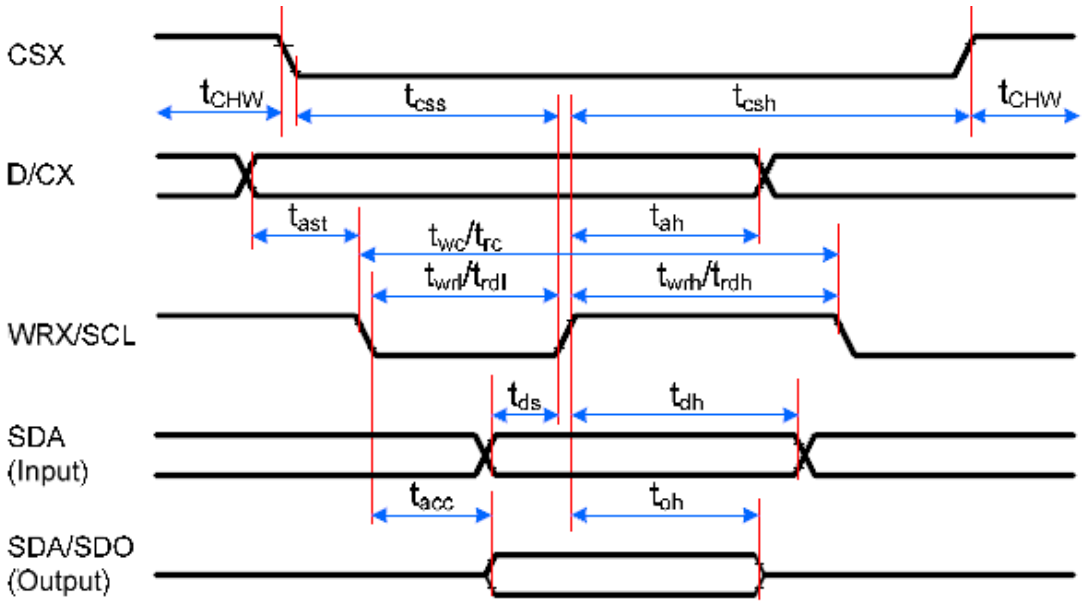


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



7.3 Display Serial Interface Timing Characteristics (4-line SPI system)

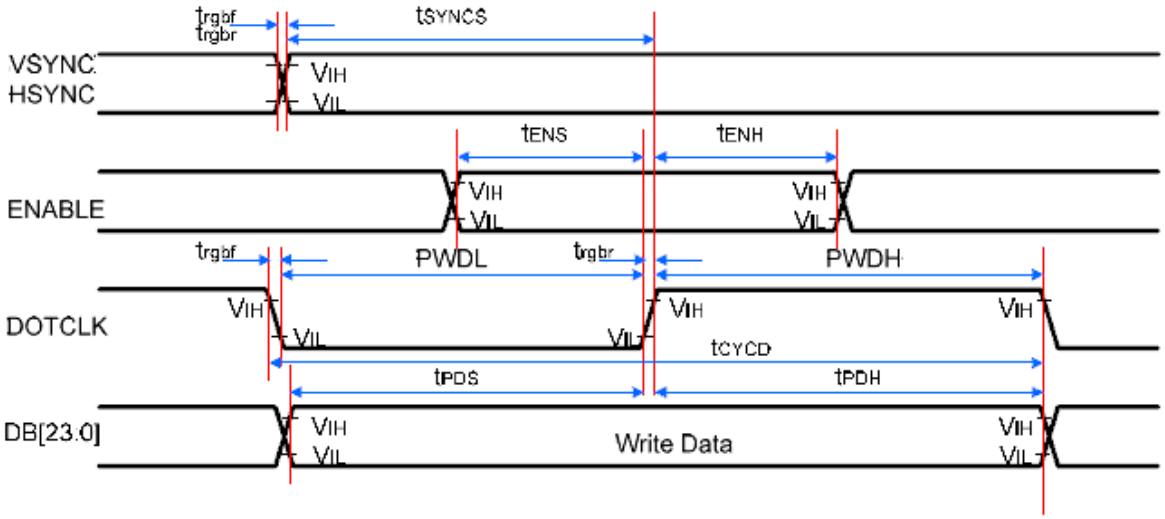


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

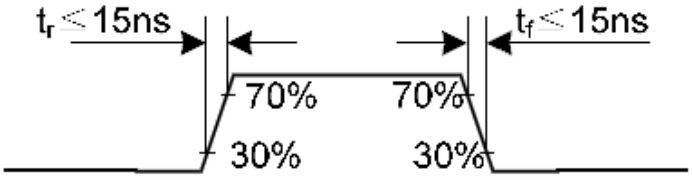
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

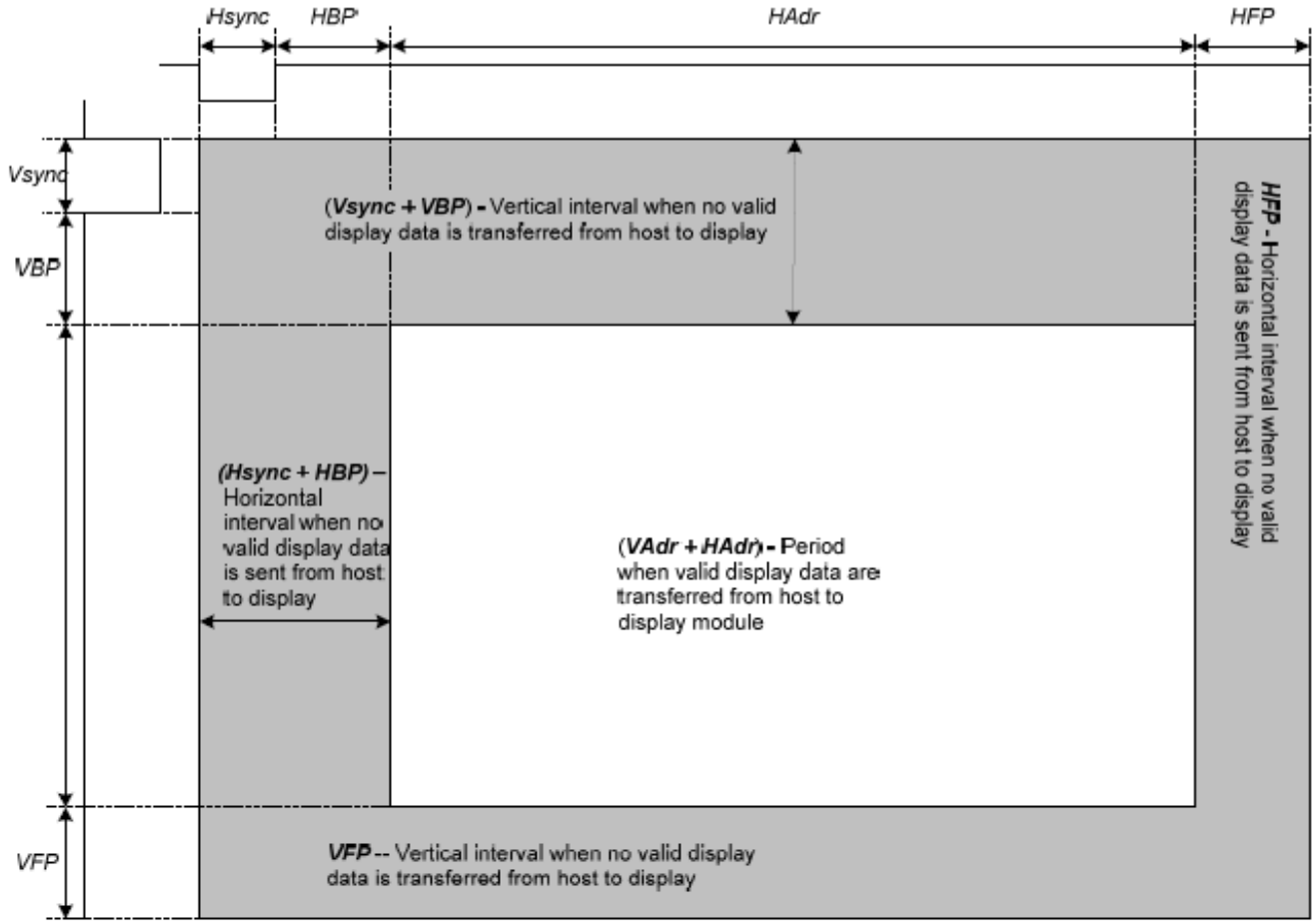
7.4 Parallel RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V





Parameters	Symbols	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3	-	PCLK
Horizontal Back Porch	HBP	3	3	-	PCLK
Horizontal Address	HAdr	-	320	-	PCLK
Horizontal Front Porch	HFP	3	3	-	PCLK
Vertical Synchronization	Vsync	2	2	-	Line
Vertical Back Porch	VBP	2	2	-	Line
Vertical Address	VAdr	-	480	-	Line
Vertical Front Porch	VFP	2	2	-	Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	-	KHz
PCLK Frequency(*)		10	12.5	15	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

7.5 Reset Timing Characteristics

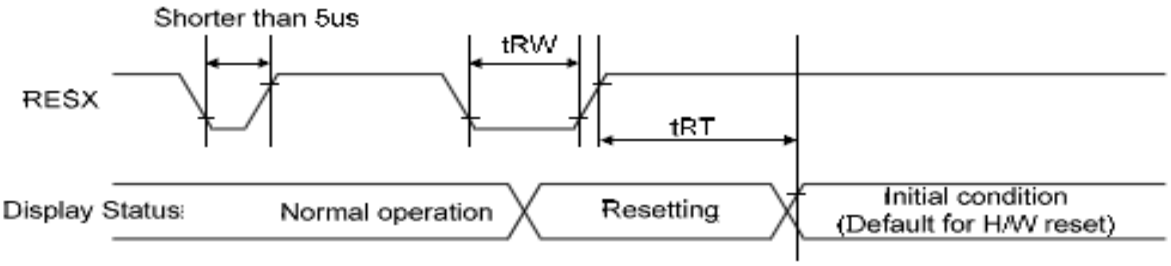


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

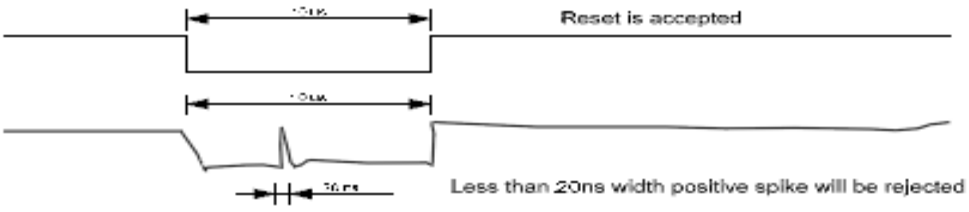


Figure 137: Positive Noise Pulse during Reset Low

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

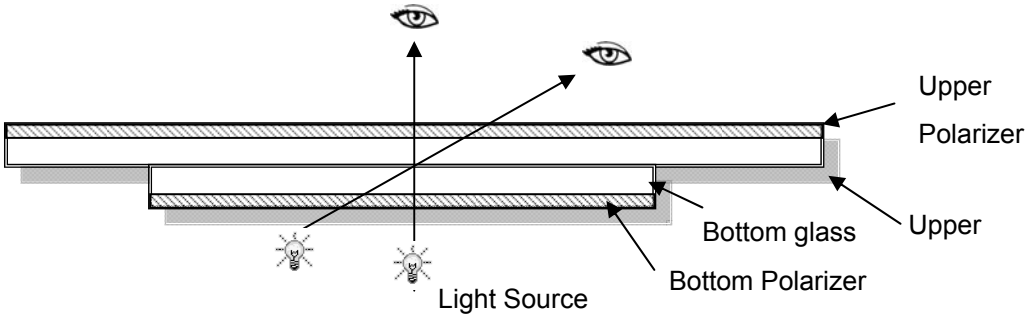
Temperature : 25±5℃

Humidity : 65%±10%RH

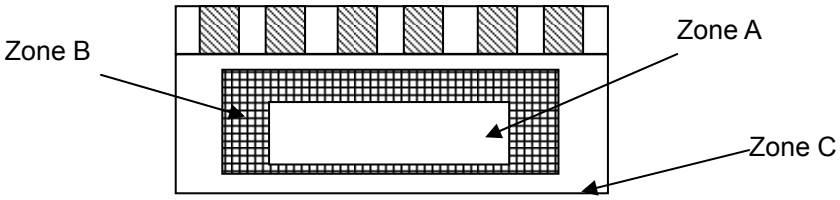
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

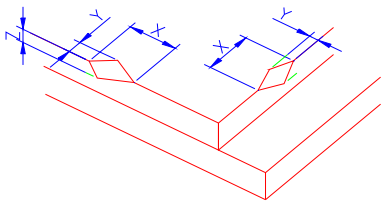
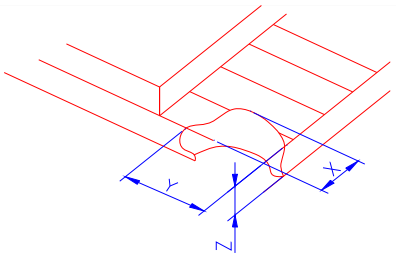
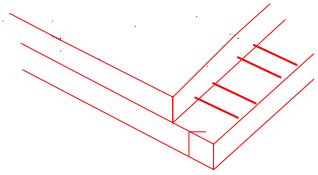
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

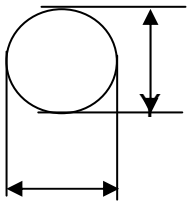
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken

NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0 Spot defect



X

Φ=(X+Y)/2

① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Zone / Size (mm)	Accep able Qty		
	A	B	C
Φ≤0.10	Ignore		Ignor
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ＞0.25	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.30	2		
Φ＞0.30	0		

③ Polarizer accidented spot

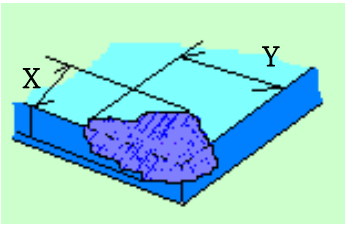
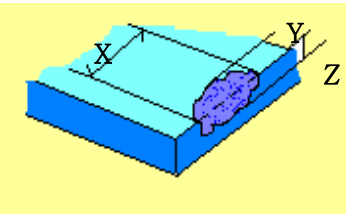
Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

Line defect (LCD/TP /Polarizer black/white line, scratch, stain)

Width(mm)	Length(mm	Acceptable Qty		
		A	B	C
Φ≤0.03	Igno e	Ignore		Ignore
0.03<W≤0.05	L≤3.0	N≤2		
0.05<W≤0.08	L≤2.0	N≤2		
0.08<W	Define as spot defect			

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td colspan="3">
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">3(distance≧10 m)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td colspan="3">According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
<tr><td rowspan="3">5.0</td><td rowspan="3">TP Related</td><td>TP bubble/ accidented spot</td><td colspan="2">
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2">3（distance≧</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td colspan="2">beyond the edge of backlight ≤0.15mm</td></tr>
<tr><td>Newton Ring</td><td>Newton Ring area>1/3 TP area NG

Newton Ring area≤1/3 TP area OK</td><td> 
</td></tr>
</table>

		TP corner broken X：length Y：width Z：height	X: X≤3.0mm; Y: Y≤3.0mm; Z: Z<LCD thicknes * Circuitry broken is not allowed.	
		TP edge broken X：length Y：width Z：height	X: X≤6.0mm; Y: Y≤2.0mm; Z: Z<LCD thicknes * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11.Packing

----TBD----------