KAF-18500

5270 (H) x 3516 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−18500 is a dual output, high performance color CCD (charge coupled device) image sensor with 5270 (H) x 3516 (V) photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains anti−blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.8 μm square pixels are selectively covered with red, green or blue pigmented filters for color separation. Microlenses are added for improved sensitivity.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD with Square Pixels
Total Number of Pixels	5422 (H) x 3610 (V) = 19.6 M
Number of Effective Pixels	5310 (H) x 3556 (V) = 18.8 M
Number of Active Pixels	5270 (H) x 3516 (V) = 18.5 M
Pixel Size	6.8 μm (H) x 6.8 μm (V)
Imager Size	43.1 mm (diagonal), 35 mm Optical format
Chip Size	37.8 mm (H) x 26.4 mm (V)
Aspect Ratio	3:2
Saturation Signal	42 ke^-
Charge to Voltage Conversion	25 $\mu V/e^-$
Quantum Efficiency (RGB)	30%, 45%, 40%
Read Noise (f = 24 MHz)	15.7 e^-
Dark Signal (T = 60°C)	50 pA/cm^2
Dark Current Doubling Temperature	5.3°C
Linear Dynamic Range (f = 24 MHz, T = 60°C)	68.1 dB
Charge Transfer Efficiency (HCTE/VCTE)	0.999995 0.999998
Blooming Protection (4 ms exposure time)	5600 X saturation exposure
Maximum Data Rate	24 MHz
Readout Mode	Dual Output Only
Package	PGA
Cover Glass	AR coated (S8612)

NOTE: Unless otherwise noted, all parameters above are specified at T = 20°C to 25°C.

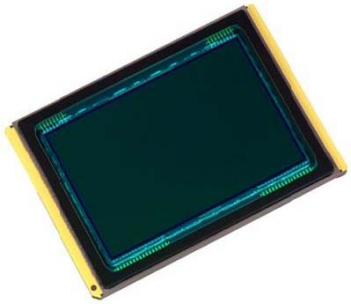

Figure 1. KAF−18500 CCD Image Sensor

Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- High Resolution, 35 mm Format
- Broad Dynamic Range
- Low Noise
- Large Image Area

Applications

- Digital Still Cameras

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAF−18500−NXA−JH−AA−08	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass, 0.8 mm glass	KAF−18500−NXA−08
KAF−18500−NXA−JH−AE−08	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass, 0.8 mm glass [Engineering Grade]	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

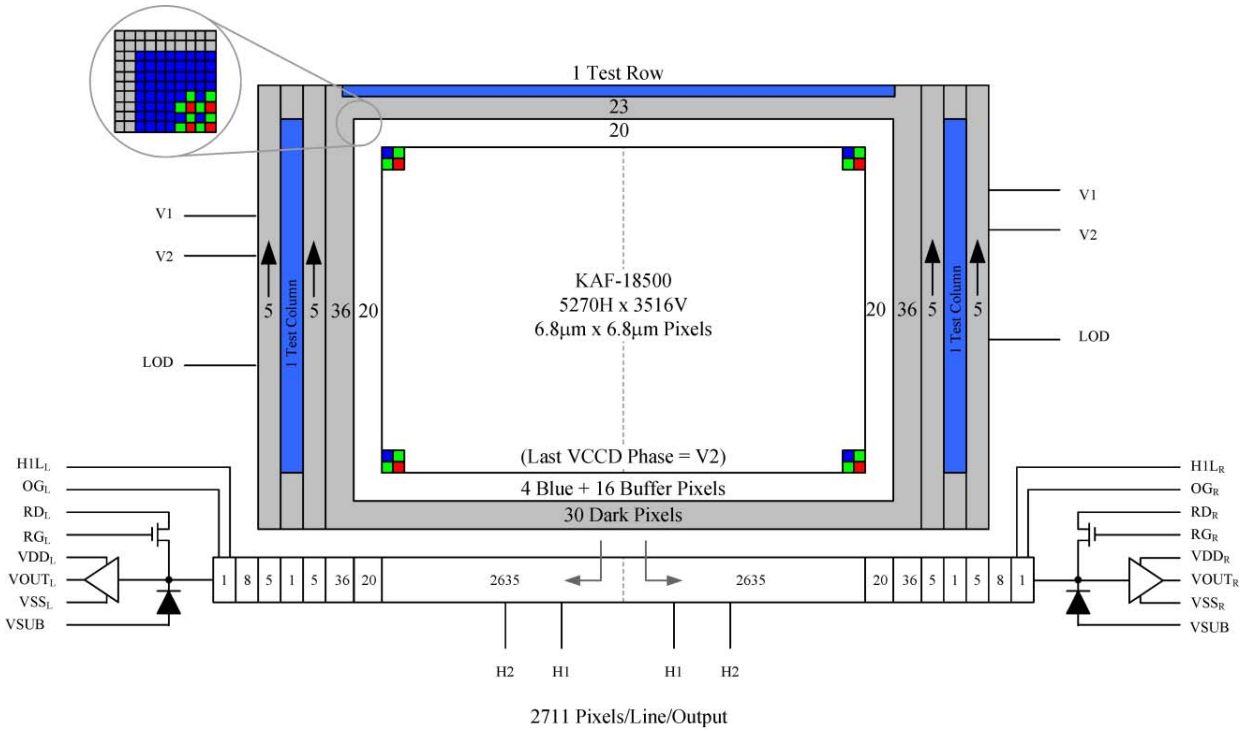


Figure 2. Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 36 leading dark pixels on every line. There are also 30 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dummy Pixels

Within each horizontal shift register there are 20 leading additional shift phases required before the dark reference pixels: (1 + 8 + 5 + 1 + 5) (See Figure 2). These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 20 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non−uniformities. For the leading 20 active column pixels, the first 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B).

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the device. These photon−induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non−linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each photogate (pixel) is transported to the output using a two−step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented with a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion output amplifier. On each falling edge of H1L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

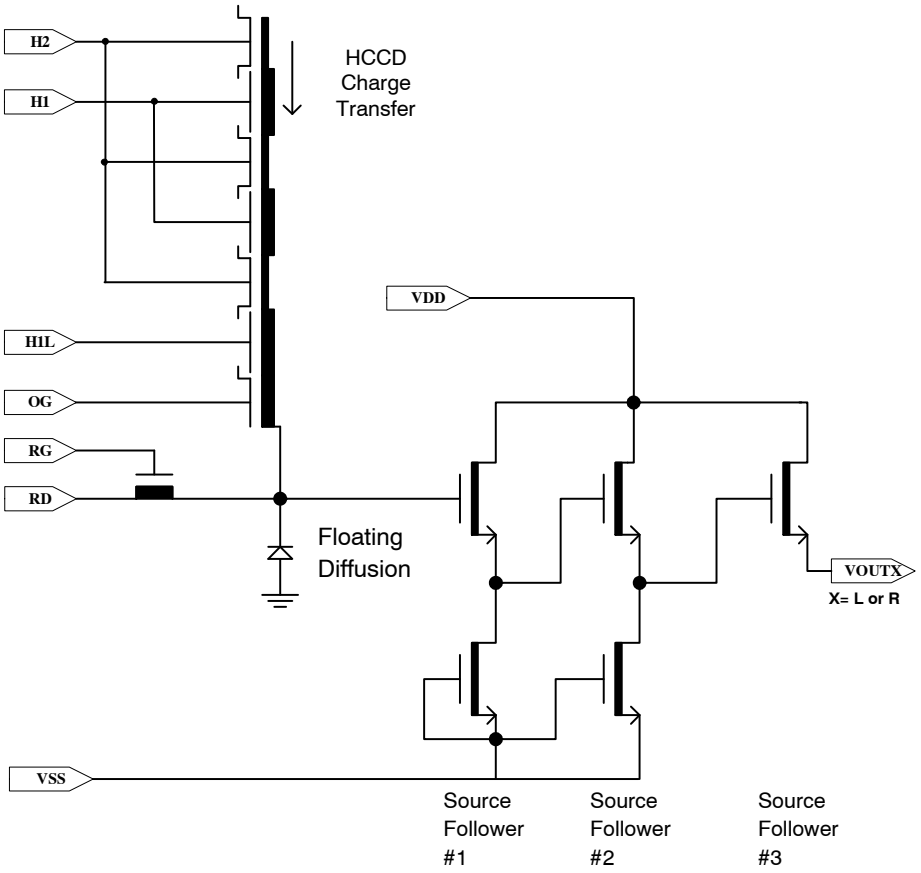
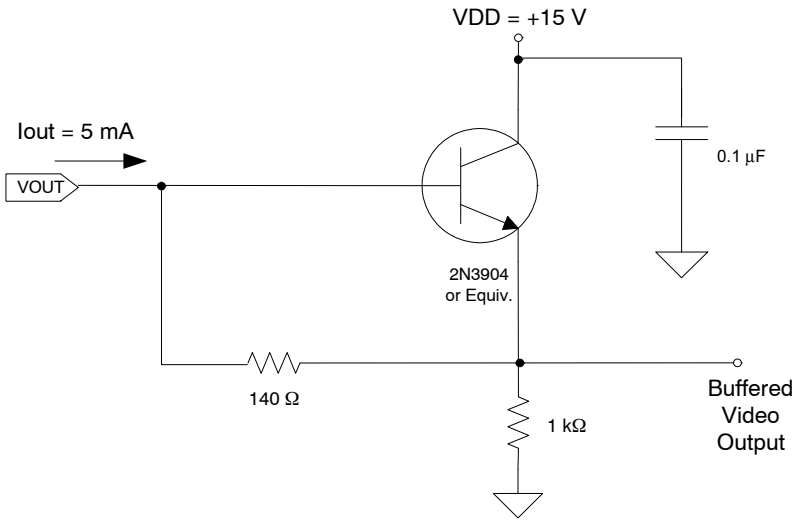


Figure 3. Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three−stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off−chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off−chip current source must be added to the VOUT pins of the device. See Figure 4.

Output Load

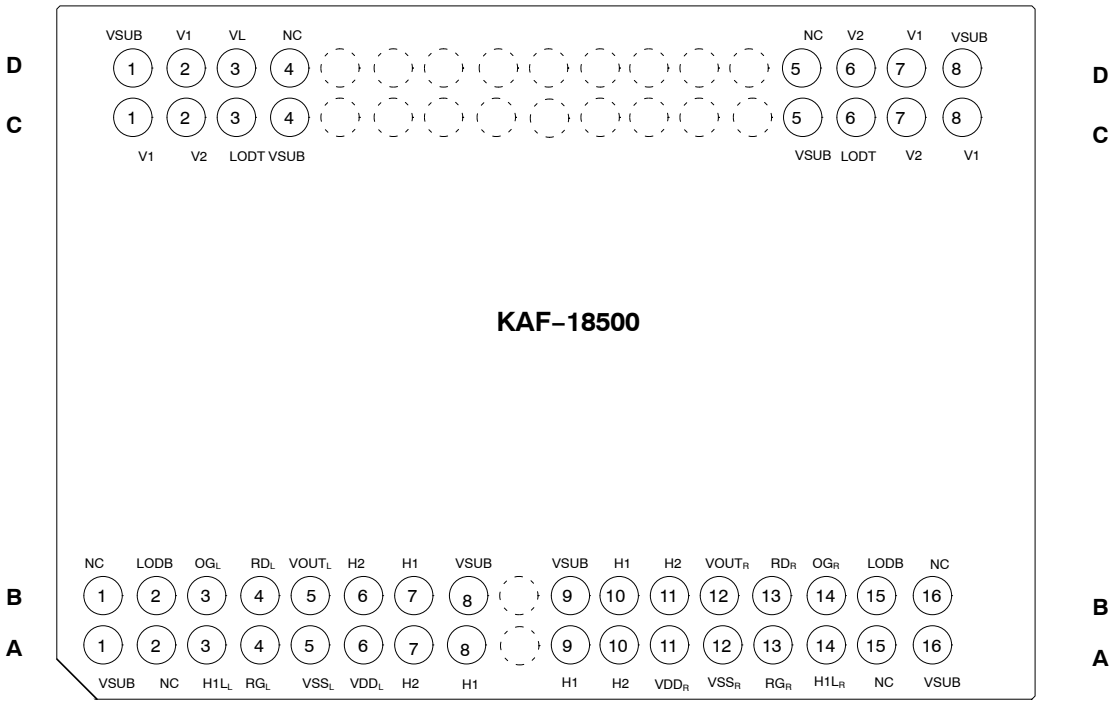


Note: Component values may be revised based on operating conditions and other design considerations.

Figure 4. Typical Output Structure Load Diagram

PHYSICAL DESCRIPTION

Pin Description and Device Orientation



Top View

Figure 5. Pinout Diagram − Top View

Table 3. PGA GRID ROW A

Pin	Name	Description
1	VSUB	Substrate
2	NC	Physical pin with no connection on die
3	$H1L_L$	Horizontal Phase 1, last phase, left side
4	RG_L	Reset Drain, left side
5	VSS_L	Output Amplifier Return, left side
6	VDD_L	Output Amplifier Supply, left side
7	H2	Horizontal Phase 2
8	H1	Horizontal Phase 1
9	H1	Horizontal Phase 1
10	H2	Horizontal Phase 2
11	VDD_R	Output Amplifier Supply, right side
12	VSS_R	Output Amplifier Return, right side
13	RG_R	Reset Gate, right side
14	$H1L_R$	Horizontal Phase 1, last phase, right side
15	NC	Physical pin with no connection on die
16	VSUB	Substrate

Table 4. PGA GRID ROW B

Pin	Name	Description
1	NC	Physical pin with no connection on die
2	LODB	Lateral Overflow Drain, bottom
3	OG_L	Output Gate, left side
4	RD_L	Reset Gate, left side
5	$VOUT_L$	Video Output, left side
6	H2	Horizontal Phase 2
7	H1	Horizontal Phase 1
8	VSUB	Substrate
9	VSUB	Substrate
10	H1	Horizontal Phase 1
11	H2	Horizontal Phase 2
12	$VOUT_R$	Video Output, right side
13	RD_R	Reset Drain, right side
14	OG_R	Output Gate, right side
15	LODB	Lateral Overflow Drain, bottom
16	NC	Physical pin with no connection on die

Table 5. PGA GRID ROW C

Pin	Name	Description
1	V1	Vertical Phase 1
2	V2	Vertical Phase 2
3	LODT	Lateral Overflow Drain, top
4	VSUB	Substrate
5	VSUB	Substrate
6	LODT	Lateral Overflow Drain, top
7	V2	Vertical Phase 2
8	V1	Vertical Phase 1

Table 6. PGA GRID ROW D

Pin	Name	Description
1	VSUB	Substrate
2	V1	Vertical Phase 1
3	V2	Vertical Phase 2
4	NC	Physical pin with no connection on die
5	NC	Physical pin with no connection on die
6	V2	Vertical Phase 2
7	V1	Vertical Phase 1
8	VSUB	Substrate

IMAGING PERFORMANCE

Table 7. TYPICAL OPERATIONAL CONDITIONS

Description	Condition	Notes
Frame time ($t_{readout}$ + t_{int})	Varies, see below	Includes overclock pixels
Readout time ($t_{readout}$)	527 ms	
Integration time (t_{int})	Varies per test: Bright Field 250 ms, Dark Field 1 sec, Saturation 250 ms, Low light 33 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 – 25°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{Vw} = 11 μs	

Table 8. SPECIFICATIONS

Description	Symbol	Min	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal	Vsat Ne^-_{sat} Q/V	900 (35000)	1086 42000 25.6		mV e^- $\mu V/e^-$	1, 19	die[17] design[18] design[18]
Peak Quantum Efficiency red green blue	Rr Rg Rb		30 45 40		%		design[18]
High Level Photoresponse Non−Linearity	Le_High		2	10	%	2	die[17]
Low Level Photoresponse Non−Linearity	Le_Low		2	10	%	2	die[17]
Photo Response Non−Uniformity each color plane	PRNU		4.5	25	%p−p	3	die[17]
Integration Dark Signal	Vdark, int		4	10	mV/s	4, 16	die[17]
Readout Dark Signal	Vdark, read		12	20	mV/s	15, 16	die[17]
Dark Signal Non−Uniformity	DSNU		0.5	4	mV p−p	5	die[17]
Dark Signal Doubling Temperature	ΔT		5.3		°C		design[18]
Read Noise	N_R		15.7		e^- rms		design[18]
Total Noise	N		18.9		e^- rms	6	design[18]
Linear Dynamic Range	DR		68.1		dB	7	design[18]
Red−Green Hue Shift Blue−Green Hue Shift	RGHueUnif BGHueUnif		1.8	12	%	8	die[17]
Horizontal Charge Transfer Efficiency	HCTE	0.999995	0.999995			9	die[17]
Vertical Charge Transfer Efficiency	VCTE	0.999999	0.999999				die[17]
Blooming Protection	Xab		5600		x Vsat	10	design[18]
DC Offset, output amplifier	Vodc	6.0	8	9.5	V	11	die[17]
Output Amplifier Bandwidth	f_{-3dB}		232		MHz	12	design[18]
Output Impedance, Amplifier	R_{OUT}	100	137	300	Ω		die[17]
Hclk Feedthru	V_{hft}		3.7	20	mV	13	die[17]
Reset Feedthru	V_{rft}		0.5		V	14	design[18]

1. Increasing output load currents to improve bandwidth will decrease the conversion factor (Q/V).
2. Worst case deviation (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 85% of Vsat min.
3. Difference between the maximum and minimum average signal levels of 148 x 148 blocks within the sensor on a per color basis as a % of average signal level.
4. T = 60°C. Average non−illuminated signal with respect to over−clocked vertical register signal.
5. T = 60°C. Absolute difference between the maximum and minimum average signal levels of 148 x 148 blocks within the sensor.
6. rms deviation of a multi−sampled pixel measured in the dark including amplifier and system noise sources.
7. 20log (0.95 * Vsat/VN). Specified at T = 60°C.
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (148 x 148 blocks) within the sensor.
9. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 24 MHz.
10. Xab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4 ms.
11. Video level offset with respect to ground.
12. Last stage only. Assumes 5 pF off−chip load.
13. Amount of artificial signal due to H1 coupling.
14. Amplitude of feedthrough pulse in VOUT due to RG coupling.
15. T = 60°C. Average non−illuminated signal collected due to the read out time.
16. Total dark signal = (Vdark,int x t_{int}) + (Vdark,read x $t_{readout}$).
17. A parameter that is measured on every sensor during production testing.
18. A parameter that is quantified during the design verification activity.
19. Specified at T = 60°C.

TYPICAL PERFORMANCE CURVES

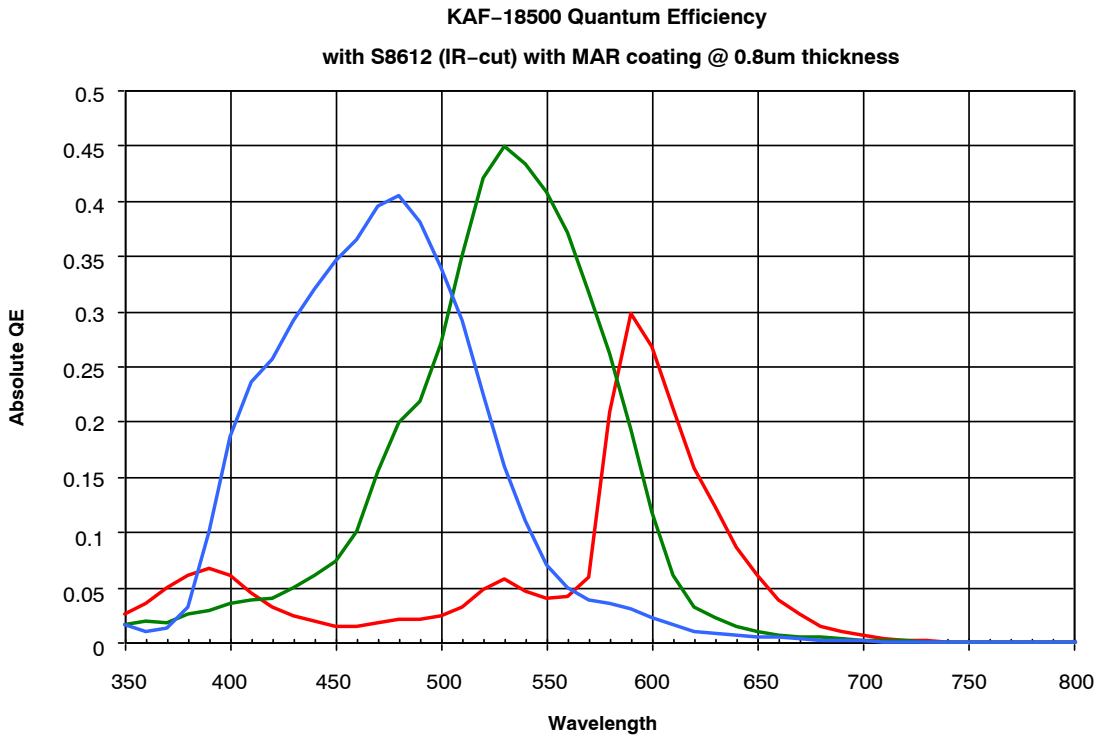


Figure 6. Typical Quantum Efficiency

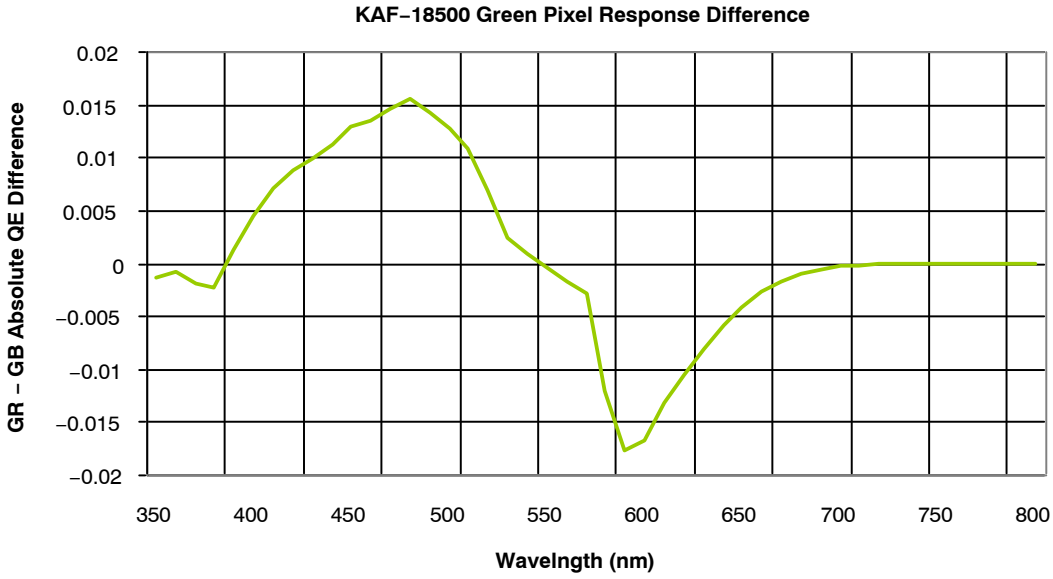


Figure 7. Typical GR−GB QE Difference

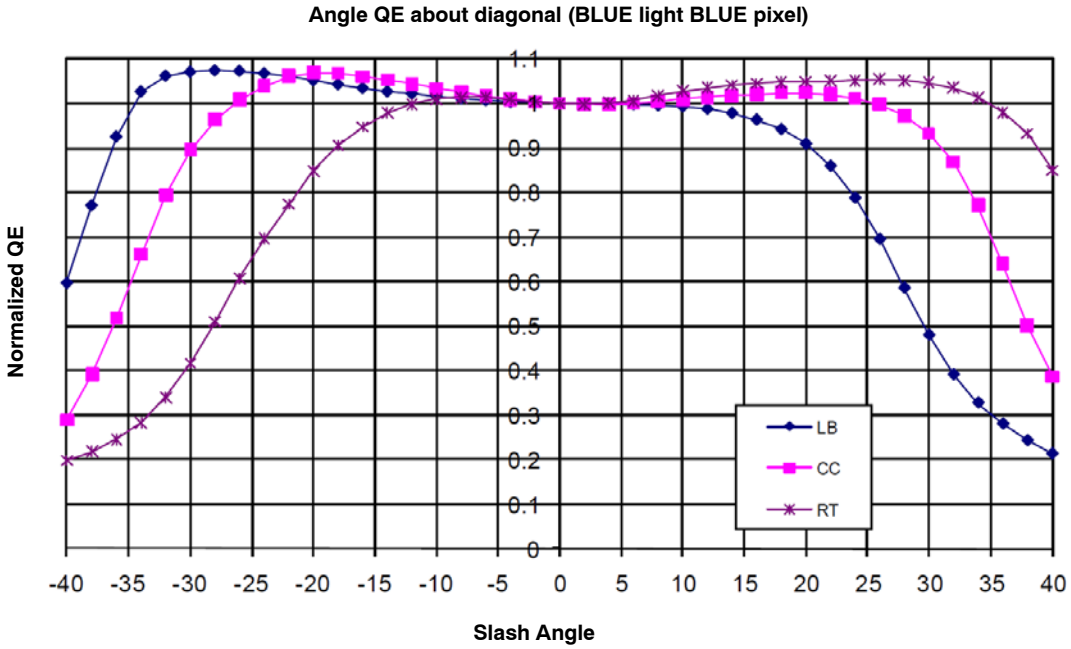


Figure 8. Typical Normalized Angle QE

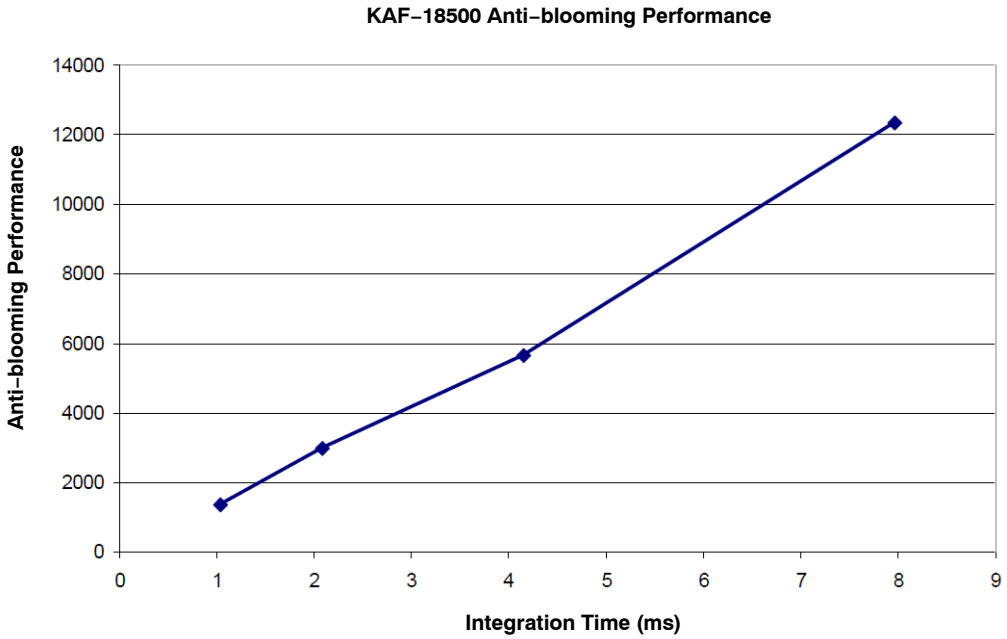


Figure 9. Typical Anti Blooming Performance

DEFECT DEFINITIONS

Operating Conditions

All defect tests performed at:

Table 9. OPERATING CONDITIONS

Description	Condition	Notes
Integration time (tint)	Varies per test: Bright Field 250 ms, Dark Field 1 sec, Saturation 250 ms, Low light 33 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 – 25°C	Room temperature

Table 10. SPECIFICATIONS

Classification	Points	Clusters, small and large	Clusters, large	Columns	Includes Dead Columns
Standard Grade	≤ 4400	≤ 50	≤ 5	≤ 15	yes

Point Defects

A pixel that deviates by more than 9 mV above neighboring pixels under non−illuminated conditions.

−or−

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions.

Cluster Defect

Small clusters: A grouping of adjacent point defects that can number in size from 2 to 10 pixels.

Large clusters: A grouping of more than 10 pixels but not larger than 20 adjacent point defects. A single large cluster is not to exceed 5 adjacent pixels within the same color plane.

Cluster Separation

Cluster defects are separated by no less than 4 good pixels in any direction.

Column Defect

A grouping of more than 10 point defects along a single column

−or−

A column that deviates by more than 0.9 mV above or below neighboring columns under non−illuminated conditions.

−or−

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions.

Column and cluster defects are separated by at least 4 good columns in the x direction. No multiple column defects (double or more) will be permitted.

Dead Columns

A column that deviates by more than 50% below neighboring columns under illuminated conditions.

Saturated Columns

A column that deviates by more than 100 mV above neighboring columns under non−illuminated conditions. No saturated columns are allowed.

OPERATION

Table 11. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	−0.5	+17.5	V	1, 2
Gate Pin Voltages	V_{gate1}	−13.5	+13.5	V	1, 3
Gate−Gate Voltages	V_{1-2}	−13.5	+13.5	V	4, 5
Output Bias Current	I_{out}		−30	mA	6
LOD Diode Voltage	V_{LODT}	−0.5	+13.0	V	7
Operating Temperature	T_{OP}	0	60	°C	8

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
5. Voltage difference between non−overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at the maximum values will reduce Mean Time to Failure (MTTF).
7. V1, H1, V2, H2, H1L, OG, and RD are tied to 0 V.
8. Noise performance will degrade at higher temperatures.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.

Power−up Sequence

The sequence chosen to perform an initial power−up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 12. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	VSS	0.5	0.7	1.0	V	I_{SS} = 3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB		0		V	0.01	
Output Gate	OG	−2.2	−2.0	−1.8	V	0.01	
Lateral Overflow Drain	LOD	9.8	10.0	10.2	V	0.01	
Video Output Current	I_{OUT}		−5	−10	mA		1

1. An output load sink must be applied to VOUT to activate output amplifier − see Figure 4.

AC Operating Conditions

Table 13. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	−9.2	−9.0	−8.8	V	245 nF	1, 2
V1 High Level	V1H	High	2.3	2.5	2.7	V	245 nF	1, 2
V2 Low Level	V2L	Low	−9.2	−9.0	−8.8	V	303 nF	1, 2
V2 High Level	V2H	High	2.3	2.5	2.7	V	303 nF	1, 2
H1, H2 (amplitude)	H1amp H2amp	Amplitude	6.5	6.75	7.0	V	See below	
H1 Low Level	H1Low	Low	−4.7	−4.5	−4.3	V	460 pF	1
H2 Low Level	H2Low	Low	−5.2	−5.0	−4.8	V	302 pF	1
H1L Low Level	H1Llow	Low	−6.7	−6.5	−6.3	V	15 pF	1
H1L High Level	H1Lhigh	High	1.3	1.5	1.7	V	15 pF	1
RG Low Level	RGL	Low	0.3	0.5	0.7	V	21 pF	1
RG High Level	RGH	High	7.8	8.0	8.2	V	21 pF	1

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).
2. Clock capacitance is the effective capacitance extrapolated from the rise and fall time measured while operating the sensor.

TIMING

Table 14. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			24	MHz	1, 2
V1, V2 Clock Frequency	f_V			45.5	kHz	1, 2
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5		10	%	3, 7
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	5		10	%	3
V1 − V2 Cross−over	V_{VCR}	1			V	
H1 − H2 Cross−over	V_{HCR}	−3.0	−1.5	0	V	
H1L Rise − H2 Fall Crossover	V_{H1LCR}	−2.0		1.0	V	9
H1, H2 Setup Time	t_{HS}	1	5		μs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
RG Rise, Fall Times	t_{RGr}, t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	11			μs	2, 6
Flush Clock Off Time	t_{off}	4			μs	2, 6
Pixel Period (1 Count)	t_e	42			ns	2
H1L − VOUT Delay	t_{HV}		5		ns	
RG − VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	505			ms	6, 8
Integration Time	t_{int}					5, 6
Line Time	t_{line}	140			μs	6
Fast Flush Time	t_{flush}	88			ms	

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10 nsec whichever is greater based on the frequency of the horizontal clocks.
8. $t_{readout} = t_{line} * 3610$ lines
9. The charge capacity near the output could be degraded if the voltage at the clock cross over point is outside this range.

Edge Alignment

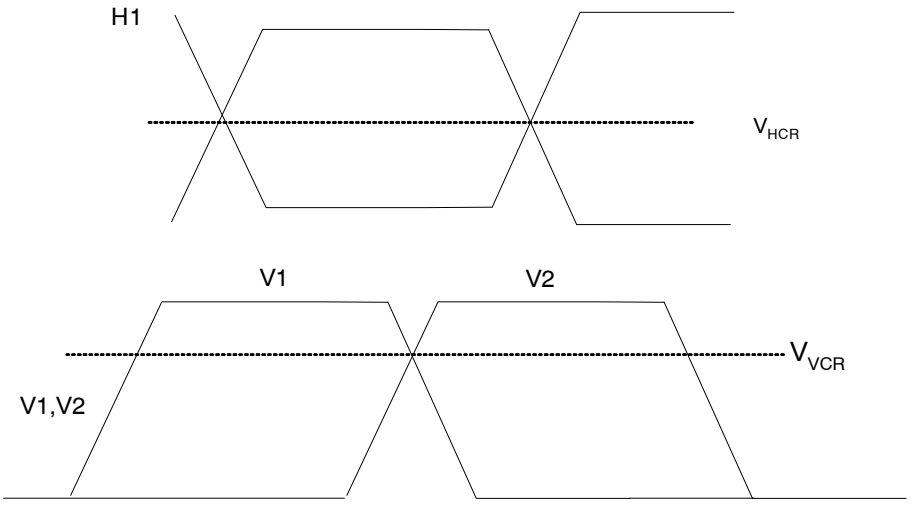


Figure 10. Timing Edge Alignment

Frame Timing

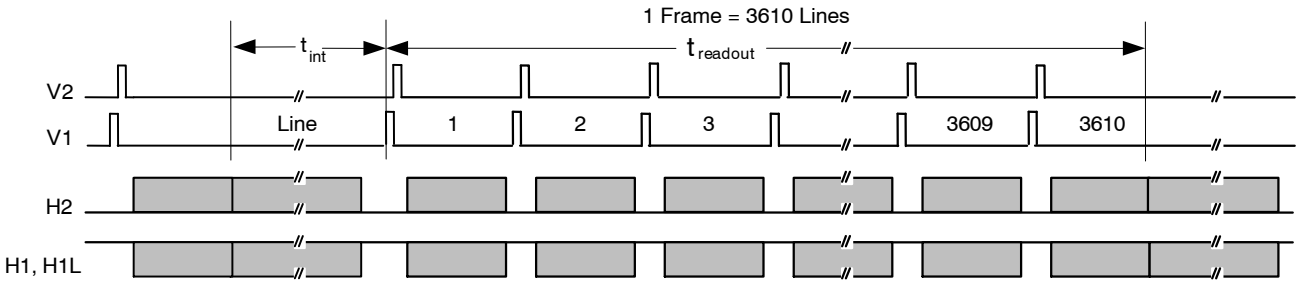


Figure 11. Frame Timing

Frame Timing Detail

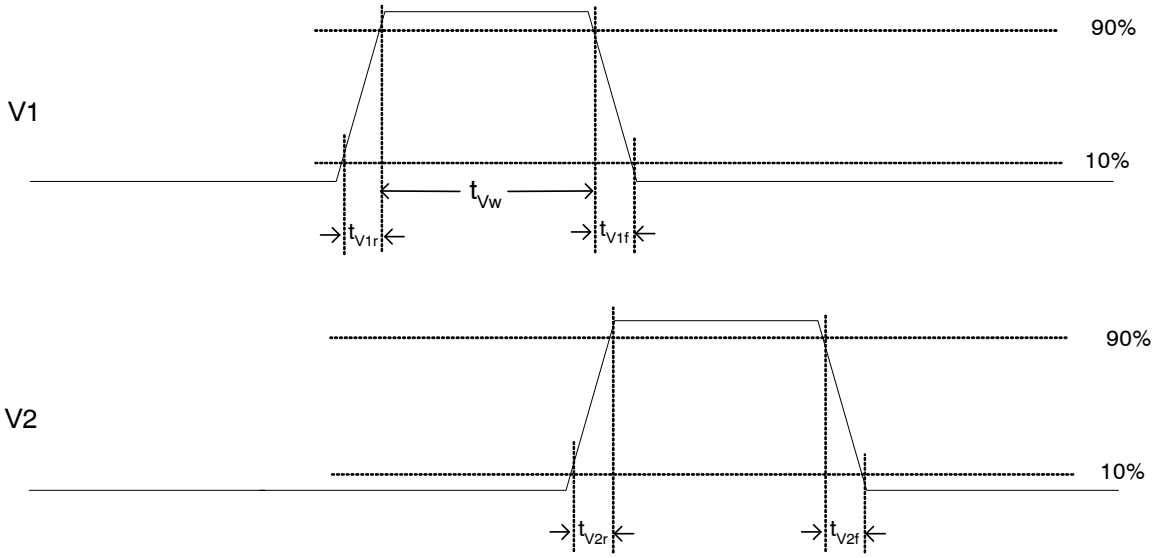


Figure 12. Frame Timing Detail

Line Timing (Each Output)

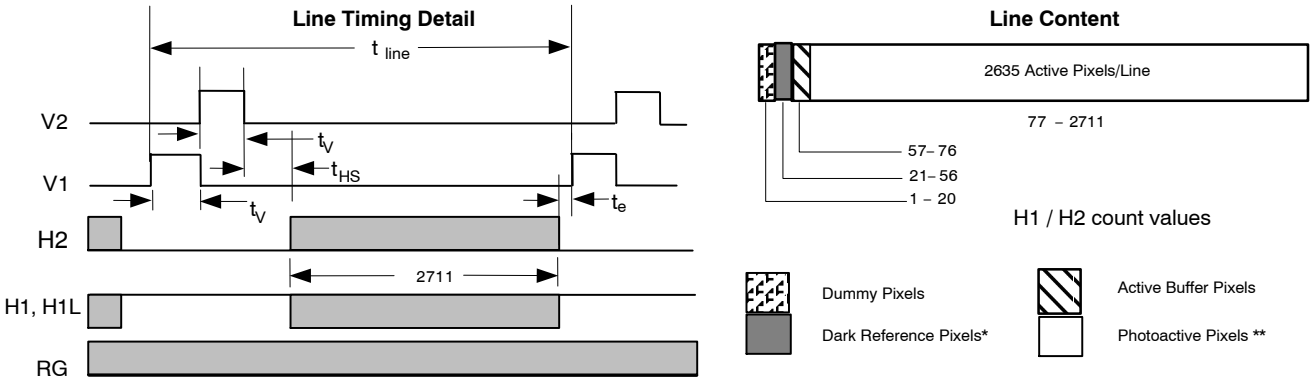


Figure 13. Line Timing

Pixel Timing

Pixel Timing Detail

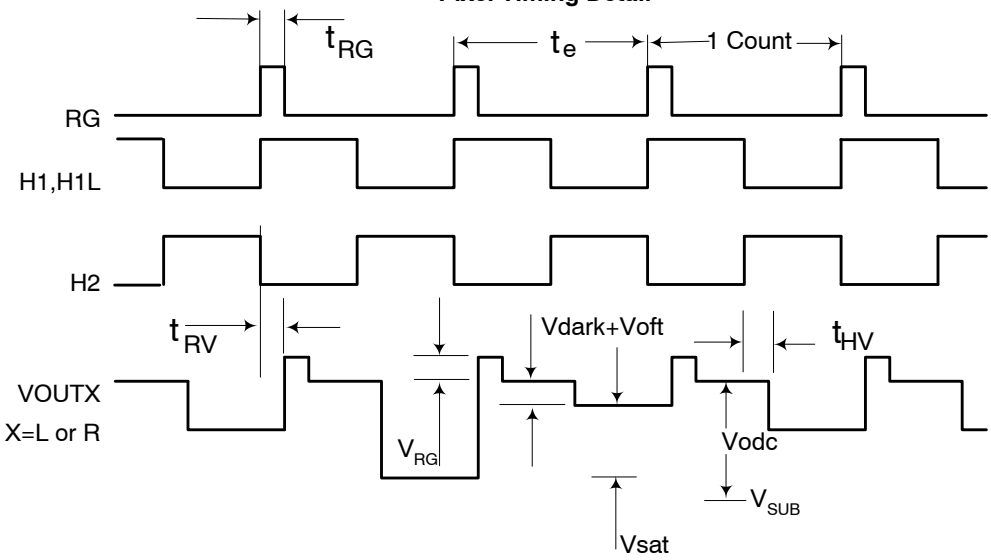


Figure 14. Pixel Timing

Pixel Timing Detail

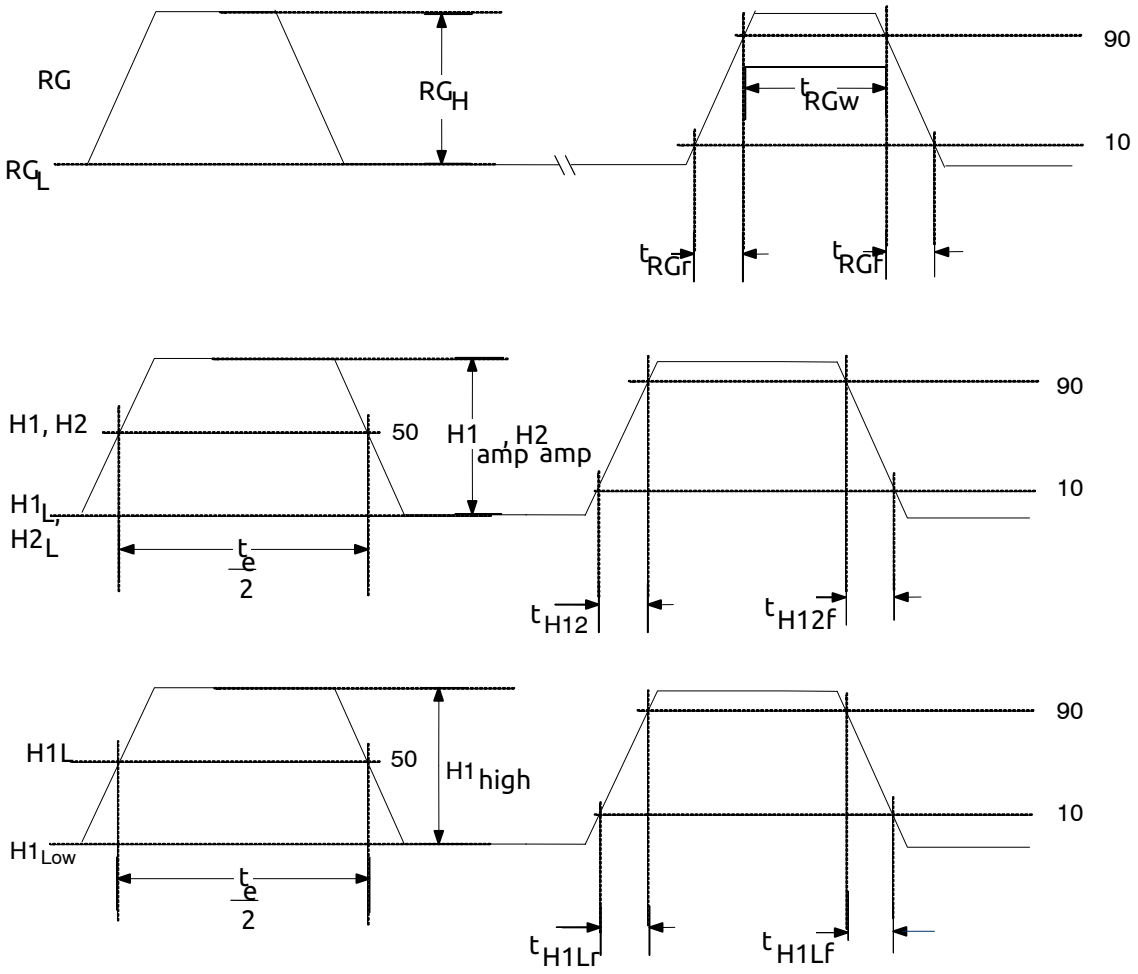


Figure 15. Pixel Timing Detail

MODE OF OPERATION

Power−up Flush Cycle

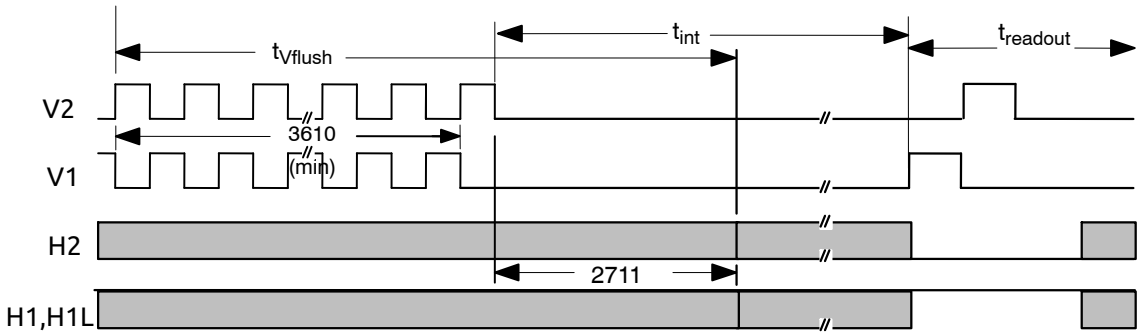


Figure 16. Power−up Flush Cycle

STORAGE AND HANDLING

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

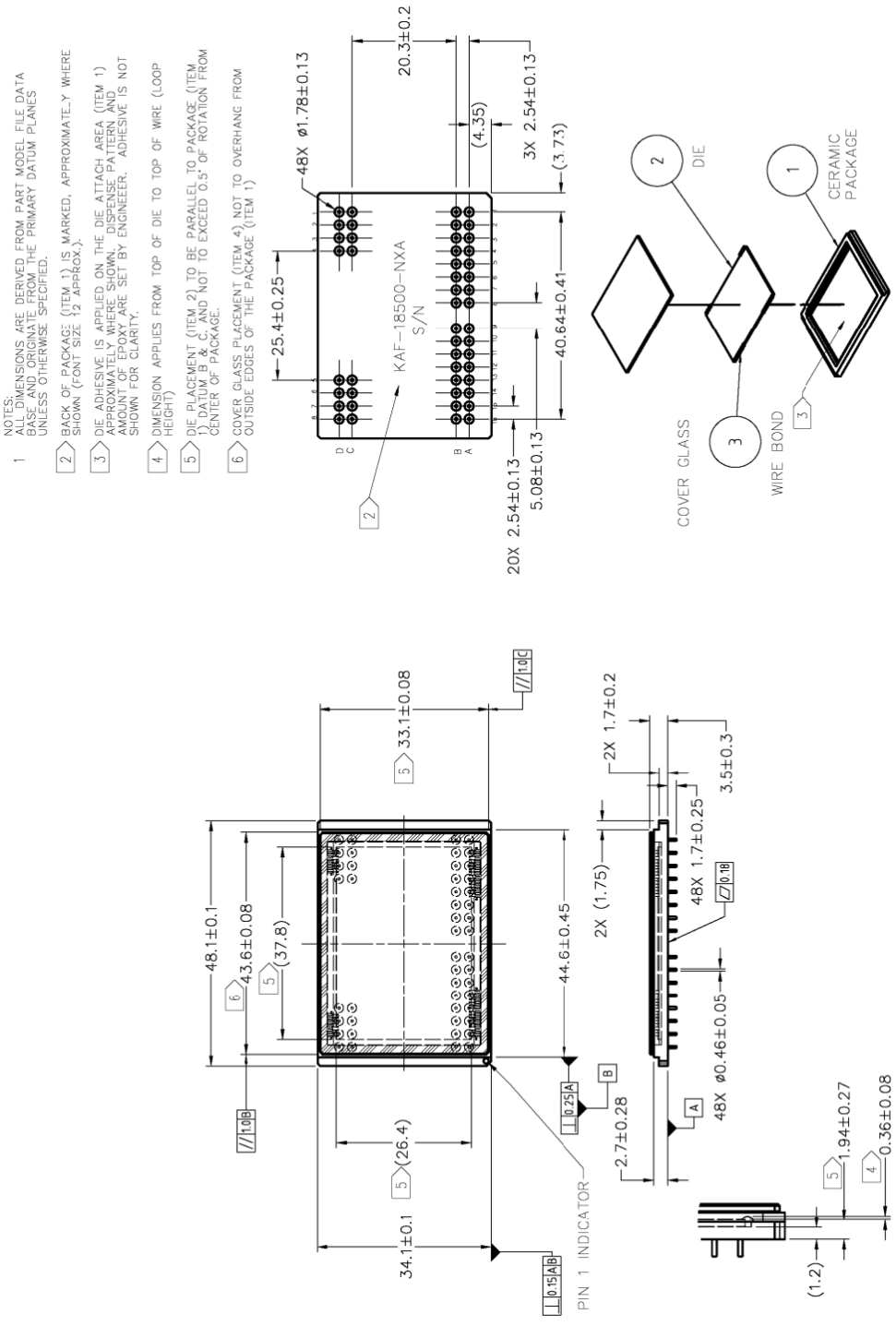


Figure 17. Completed Assembly Drawing

Cover Glass Specification

MAR Coated−IR Absorbing Cover Glass

1. Dust/Scratch/Digs/Defects: 20 micron max
2. Substrate material: Schott S8612 whose performance is as published and specifications controlled by Schott, North America. The cover glass supplied for this device is as shown in Figure 17. Data supplied in the graph below is a typical transmission of the AR coated material at 0.8 mm thickness.

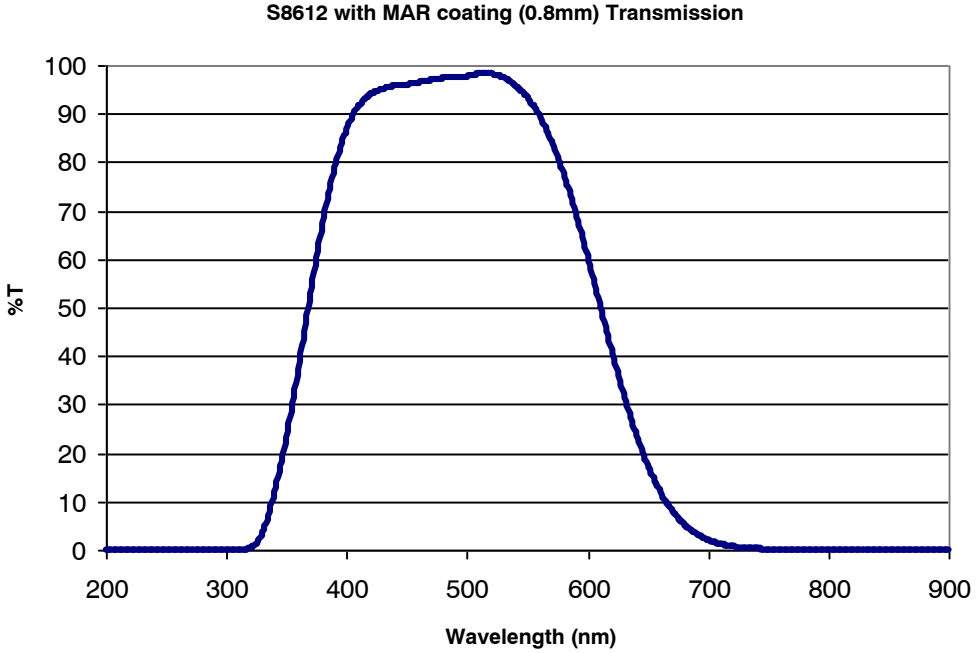


Figure 18. Cover Glass Substrate Transmission

3. Multilayer anti−reflective coating on two sides: Two−sided reflectance:

Table 15.

Wavelength	Transmission
420 − 450 nm	< 2%
450 − 630 nm	< 1%
630 − 680 nm	< 2%

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