K9GBGD8X0M
K9LCGD8X1M
K9HDGD8X5M
K9PFGD8X7M
K9PFGD8X5M

Document Title

Samsung Toggle Mode DDR NAND Specification

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	May 26, 2009	Advance
0.1	1. Restriction of Command latch cycle is noted. 2. Output driver strength impedence values for VccQ=1.8V is added.	Jun. 15, 2009	
0.1.5	1. K9LCGD8U1M-B, K9LCGD8S1M-B are added. 2. K9HDGD8U5M-B, K9HDGD8S5M-B are added. 3. K9PFGD8U7M-B, K9PFGD8S7M-B are added. 4. Ball pitch is changed from 1.4mm to 1.0mm.	Jul. 14, 2009	
0.2	1. Package type is changed from 100FBGA t o 180FBGA. 2. Output Driver Strength Values are changed. 3. Note 1 of 5.16 is amended. (Icc1 30mA -> 50mA)	Sep. 1, 2009	
0.3	1. Max. tR is changed from 400us to 80us. 2. Typ. tPROG is changed from 1.6ms to 2ms.	Sep. 24, 2009	
0.4	1. K9PFGD8U5M-B, K9PFGD8S5M-B are added. 2. Package dimension is amended. 3. Chip2 Status command(F2h) is added for K9PFGD8X5M. 4. Functional block diagram is modified. 5. A_{34} is added for K9PFGD8X5M. 6. Absolute maximum ratings are noted for each VccQ. 7. Stand-by current of TTL(I_{SB1}) is deleted. 8. Test conditions of Output High and Low Voltage Level are noted. 9. Min. valid blocks of all products are amended. 10. tR is noted for typical and maximum value. 11. Device resetting time of Erase is changed from 500us to 100us. 12. Timing of Status Read Cycle before Power On sequence is described. 13. Device ID of K9PFGD8X5M is added. 14. Device ID table definitions is amended. 15. Get feature command is deleted. 16. Busy time for Set and Get feature(tFEAT) is deleted. 17. Timing diagram of Driver Strength Register Setting is amended. 18. Interleaving operations for K9PFGD8X5M are added.	Oct. 22 , 2009	

1.0 Introduction

1.1 GENERAL DESCRIPTION

Offered in 4Gx8bit, the K9GBGD8X0M is a 32G-bit NAND Flash Memory with spare 2,076M-bit. The device is offered in 3.3V Vcc & VccQ. (3.3V & 1.8V) and also uses the toggle mode interface to achieve a high data transfer rate. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 2ms on the (8K+512)Byte page and an erase operation can be performed in typical 1.5ms on a (1M+64K)Byte block. Data in the data register can be read out at 133Mbps with 15ns cycle time. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The K9GBGD8X0M is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

1.2 FEATURES

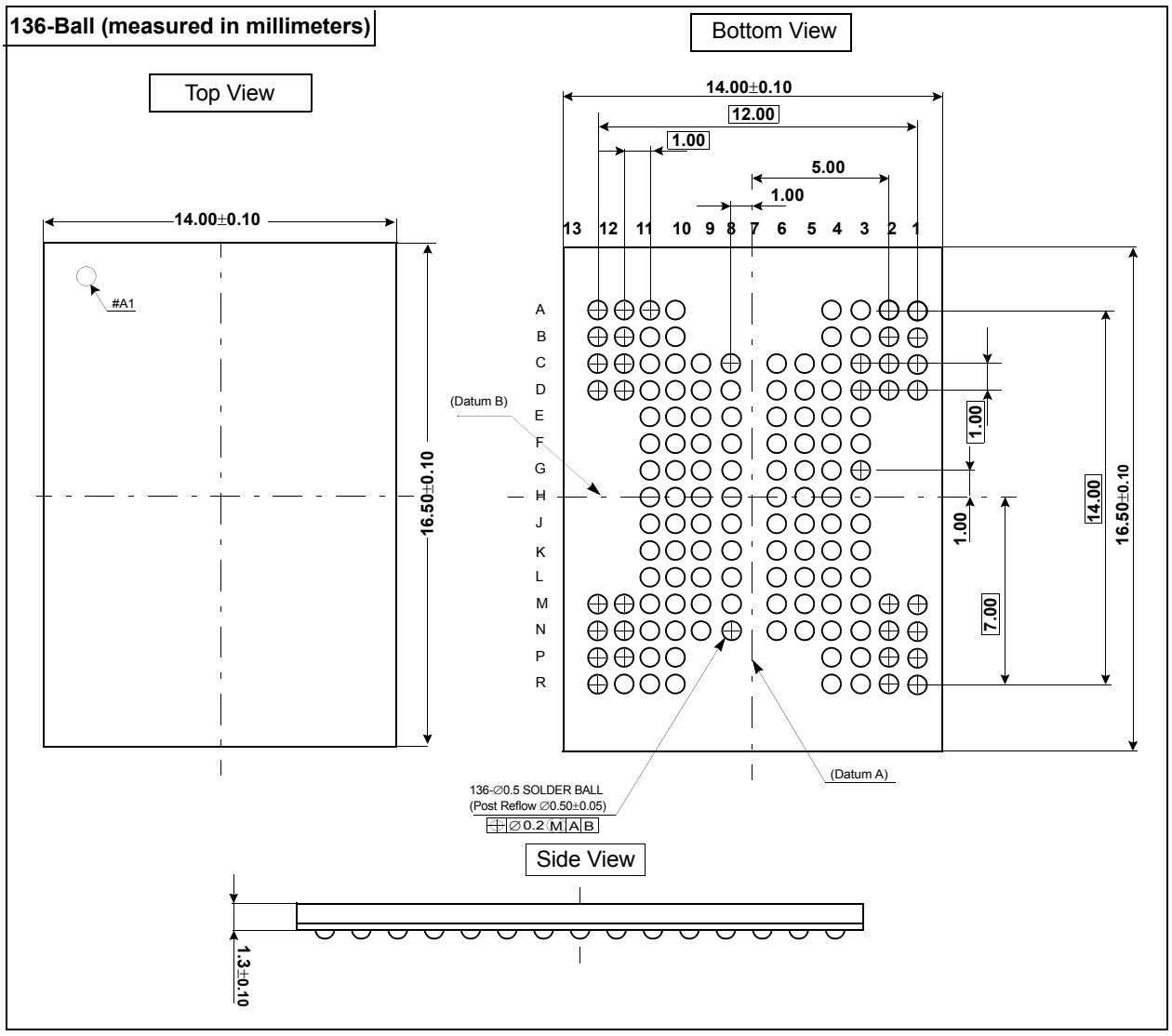
- Voltage Supply :
  - Core : 2.7V ~ 3.6V
  - I/O : 2.7V ~ 3.6V / 1.7V ~ 1.95V
- Organization
  - Memory Cell Array : (4G + 259.5M) x 8bit
  - Data Register : (8K + 512) x 8bit
- Automatic Program and Erase
  - Page Program : (8K + 512)Byte
  - Block Erase : (1M + 64K)Byte
- Page Read Operation
  - Page Size : (8K + 512)Byte
  - Random Read : 80μs(Typ.) , 100μs(Max.)
  - Data Transfer rate : 133Mbps(VccQ:3.3V) / 66Mbps(VccQ:1.8V)
- Fast Write Cycle Time
  - Page Program time : 2ms(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Toggle Mode DDR Data Interface
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - ECC Requirement : 24bits/1Kbyte
  - Endurance & Data Retention : Please refer to the Qualification report
- Command Driven Operation
- Scalable I/O Driver
- Package
  - K9GBGD8U0M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9GBGD8S0M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9LCGD8U1M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9LCGD8S1M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9HDGD8U5M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9HDGD8S5M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9PFGD8U7M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9PFGD8S7M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9PFGD8U5M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)
  - K9PFGD8S5M-BCB0: Pb/Halogen Free Package 136-Ball FBGA (14 x 16.5 /1.0mm pitch)

1.3 PRODUCT LIST

Part Number	Density	Interface	Organization	Vcc Range	VccQ Range	PKG Type
K9GBGD8U0M-B	32Gb	Toggle mode	x8	2.7V ~ 3.6V	2.7V ~ 3.6V	136 FBGA
K9GBGD8S0M-B					1.7V ~ 1.95V	
K9LCGD8U1M-B	64Gb				2.7V ~ 3.6V	
K9LCGD8S1M-B					1.7V ~ 1.95V	
K9HDGD8U5M-B	128Gb				2.7V ~ 3.6V	
K9HDGD8S5M-B					1.7V ~ 1.95V	
K9PFGD8U7M-B	256Gb				2.7V ~ 3.6V	
K9PFGD8S7M-B					1.7V ~ 1.95V	
K9PFGD8U5M-B	256Gb				2.7V ~ 3.6V	
K9PFGD8S5M-B					1.7V ~ 1.95V	

1.4 PACKAGE DIMENSIONS

1.4.1 136-Ball FBGA (measured in millimeters)



1.4.2 Ball Assignment(Top view): 1$\overline{CE}$ Single Channel(K9GBGD8X0M)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C
B	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
C	N/U	N/U	VccQ	VccQ	NU	VSS		VCC	NU	VccQ	VccQ	N/U	N/U
D	N/U	N/U	VssQ	NU	VssQ	NU		NU	VssQ	NU	VssQ	N/U	N/U
E			N/U	N/U	N/U	N/U		N/U	N/U	N/U	N/U		
F			VssQ	VccQ	N/U	N/U		R	R	VccQ	VssQ		
G			N/U	N/U	N/U	N/U		N/U	N/U	N/U	N/U		
H			VSS	VCC	R/$\overline{B}$	N/U		N/U	N/U	VCC	VSS		
J			N/U	N/U	$\overline{CE}$	N/U		NU	$\overline{WP}$	N/U	N/U		
K			VssQ	VccQ	N/U	N/U		CLE	ALE	VccQ	VssQ		
L			DQ7	DQ6	NU	$\overline{WE}$		N/U	N/U	DQ1	DQ0		
M	N/U	N/U	VssQ	DQ5	VssQ	$\overline{RE}$		DQS	VssQ	DQ2	VssQ	N/U	N/U
N	N/U	N/U	VccQ	VccQ	DQ4	VCC		VSS	DQ3	VccQ	VccQ	N/U	N/U
P	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
R	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C

1.4.3 Ball Assignment(Top view) : 2$\overline{CE}$ Dual Channel(K9LCGD8X1M)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C
B	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
C	N/U	N/U	VccQ	VccQ	DQ3-2	VSS		VCC	DQ4-2	VccQ	VccQ	N/U	N/U
D	N/U	N/U	VssQ	DQ2-2	VssQ	DQS-2		$\overline{RE}$2	VssQ	DQ5-2	VssQ	N/U	N/U
E			DQ0-2	DQ1-2	N/U	N/U		$\overline{WE}$2	N/U	DQ6-2	DQ7-2		
F			VssQ	VccQ	ALE2	CLE2		N/U	N/U	VccQ	VssQ		
G			N/U	N/U	$\overline{WP}$2	N/U		N/U	$\overline{CE}$2	N/U	N/U		
H			VSS	VCC	R/$\overline{B}$1	N/U		N/U	R/$\overline{B}$2	VCC	VSS		
J			N/U	N/U	$\overline{CE}$1	N/U		N/U	$\overline{WP}$1	N/U	N/U		
K			VssQ	VccQ	N/U	N/U		CLE1	ALE1	VccQ	VssQ		
L			DQ7-1	DQ6-1	N/U	$\overline{WE}$1		N/U	N/U	DQ1-1	DQ0-1		
M	N/U	N/U	VssQ	DQ5-1	VssQ	$\overline{RE}$1		DQS-1	VssQ	DQ2-1	VssQ	N/U	N/U
N	N/U	N/U	VccQ	VccQ	DQ4-1	VCC		VSS	DQ3-1	VccQ	VccQ	N/U	N/U
P	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
R	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C

1.4.4 Ball Assignment(Top view) : 4$\overline{CE}$ Dual Channel(K9HDGD8X5M / K9PFGD8X5M)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C
B	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
C	N/U	N/U	VccQ	VccQ	DQ3-2	VSS		VCC	DQ4-2	VccQ	VccQ	N/U	N/U
D	N/U	N/U	VssQ	DQ2-2	VssQ	DQS-2		$\overline{RE}$2	VssQ	DQ5-2	VssQ	N/U	N/U
E			DQ0-2	DQ1-2	N/U	N/U		$\overline{WE}$2	N/U	DQ6-2	DQ7-2		
F			VssQ	VccQ	ALE2	CLE2		N/U	N/U	VccQ	VssQ		
G			N/U	N/U	$\overline{WP}$2	NU		$\overline{CE}$4	$\overline{CE}$2	N/U	N/U		
H			VSS	VCC	R/$\overline{B}$1	R/$\overline{B}$3		R/$\overline{B}$4	R/$\overline{B}$2	VCC	VSS		
J			N/U	N/U	$\overline{CE}$1	$\overline{CE}$3		NU	$\overline{WP}$1	N/U	N/U		
K			VssQ	VccQ	N/U	N/U		CLE1	ALE1	VccQ	VssQ		
L			DQ7-1	DQ6-1	N/U	$\overline{WE}$1		N/U	N/U	DQ1-1	DQ0-1		
M	N/U	N/U	VssQ	DQ5-1	VssQ	$\overline{RE}$1		DQS-1	VssQ	DQ2-1	VssQ	N/U	N/U
N	N/U	N/U	VccQ	VccQ	DQ4-1	VCC		VSS	DQ3-1	VccQ	VccQ	N/U	N/U
P	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
R	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C

1.4.5 Ball Assignment (Top view): 8$\overline{CE}$ Dual Channel(K9PFGD8X7M)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C
B	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
C	N/U	N/U	VccQ	VccQ	DQ3-2	VSS		VCC	DQ4-2	VccQ	VccQ	N/U	N/U
D	N/U	N/U	VssQ	DQ2-2	VssQ	DQS-2		$\overline{RE}$2	VssQ	DQ5-2	VssQ	N/U	N/U
E			DQ0-2	DQ1-2	N/U	N/U		$\overline{WE}$2	NU	DQ6-2	DQ7-2		
F			VssQ	VccQ	ALE2	CLE2		$\overline{CE}$8	$\overline{CE}$6	VccQ	VssQ		
G			N/U	N/U	$\overline{WP}$2	NU		$\overline{CE}$4	$\overline{CE}$2	N/U	N/U		
H			VSS	VCC	R/$\overline{B}$1	R/$\overline{B}$3		R/$\overline{B}$4	R/$\overline{B}$2	VCC	VSS		
J			N/U	N/U	$\overline{CE}$1	$\overline{CE}$3		NU	$\overline{WP}$1	N/U	N/U		
K			VssQ	VccQ	$\overline{CE}$5	$\overline{CE}$7		CLE1	ALE1	VccQ	VssQ		
L			DQ7-1	DQ6-1	NU	$\overline{WE}$1		N/U	N/U	DQ1-1	DQ0-1		
M	N/U	N/U	VssQ	DQ5-1	VssQ	$\overline{RE}$1		DQS-1	VssQ	DQ2-1	VssQ	N/U	N/U
N	N/U	N/U	VccQ	VccQ	DQ4-1	VCC		VSS	DQ3-1	VccQ	VccQ	N/U	N/U
P	N/U	N/U	N/U	N/U						N/U	N/U	N/U	N/U
R	N.C	N.C	N.C	N.C						N.C	N.C	N.C	N.C

1.5 PIN DESCRIPTION

Pin Name	Pin Function
DQ_0 ~ DQ_7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the I/O bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
DQS	**Data Strobe** Output with read data, input with write data. Edge-aligned with read data, centered in write data.
Vcc	**POWER** V_{CC} is the power supply for device.
VccQ	**I/O POWER** The VccQ is the power supply for input and/or output signals.
Vss	**GROUND**
VssQ	**I/O GROUND** The VssQ is the power supply ground
N.C	**NO CONNECTION** Lead is not internally connected.
N/U	**NOT USE** Nothing should be connected with it.

NOTE :
Connect all VCC and VSS pins of each device to common power supply outputs.
Do not leave VCC or VSS disconnected.

The K9LCGDX1M has two $\overline{CE}$ pins($\overline{CE}$1 and $\overline{CE}$2) and R/$\overline{B}$ pins(R/$\overline{B}$1 and R/$\overline{B}$2).
The K9HDGDX5M has four $\overline{CE}$ pins($\overline{CE}$1 to $\overline{CE}$4) and R/$\overline{B}$ pins(R/$\overline{B}$1 to R/$\overline{B}$4).
The K9PFGDX5M has four $\overline{CE}$ pins($\overline{CE}$1 to $\overline{CE}$4) and R/$\overline{B}$ pins(R/$\overline{B}$1 to R/$\overline{B}$4).
The K9PFGDX7M has eight $\overline{CE}$ pins($\overline{CE}$1 to $\overline{CE}$8) and four R/$\overline{B}$ pins(R/$\overline{B}$1 to R/$\overline{B}$4).

Table 1. Command Sets

Function	1st Set	2nd Set	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID(1)	90h	-	
Device Identification Table Read	ECh	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(2)	85h	-	
Random Data Output(2)	05h	E0h	
Read Status	70h	-	O
Chip1 Status	F1h	-	O
Chip2 Status(4)	F2h	-	O
Set Feature	EFh	-	
Two-Plane Read	60h----60h	30h	
Two-Plane Read for Copy-Back	60h----60h	35h	
Two-Plane Random Data Output	00h----05h	E0h	
Two-Plane Page Program(3)	80h----11h	81h----10h	
Two-Plane Copy-Back Program(3)	85h----11h	81h----10h	
Two-Plane Block Erase	60h----60h	D0h	

NOTE :

1) Two sets of ID bytes are defined depending on following address which is either 00h(Samsung Legacy) or 40h(JEDEC) after Read ID.

2) Random Data Input/Output can be executed in a page.

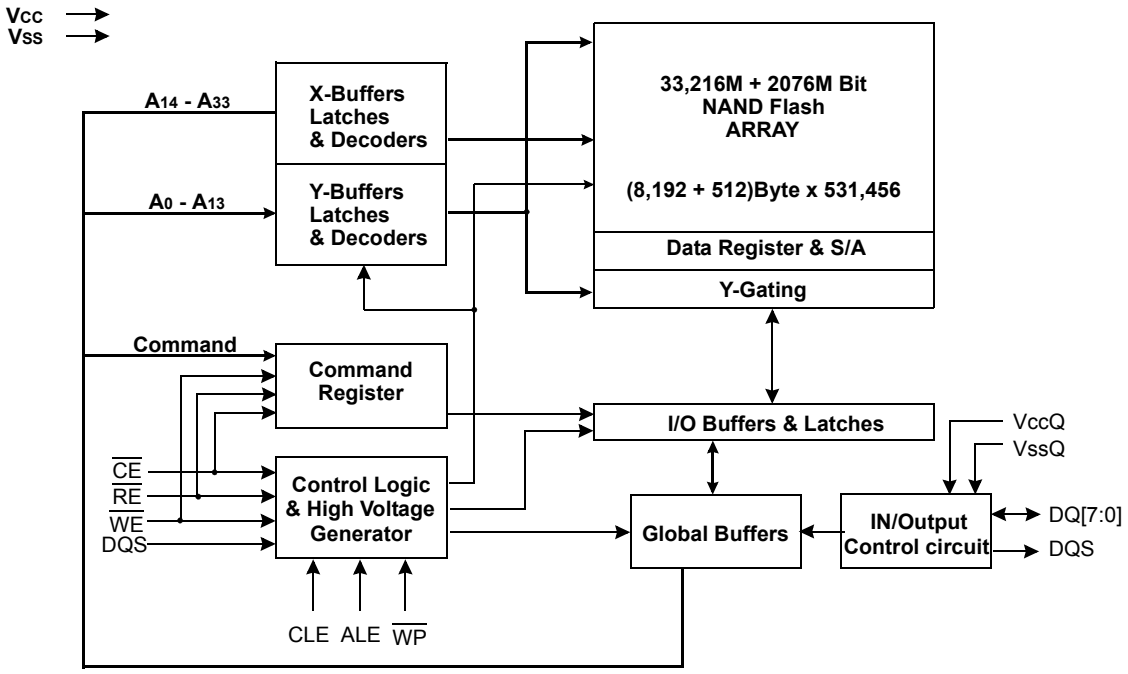
3) Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h and FFh.

4) Chip2 Status Command is supported to K9PFGD8X5M only

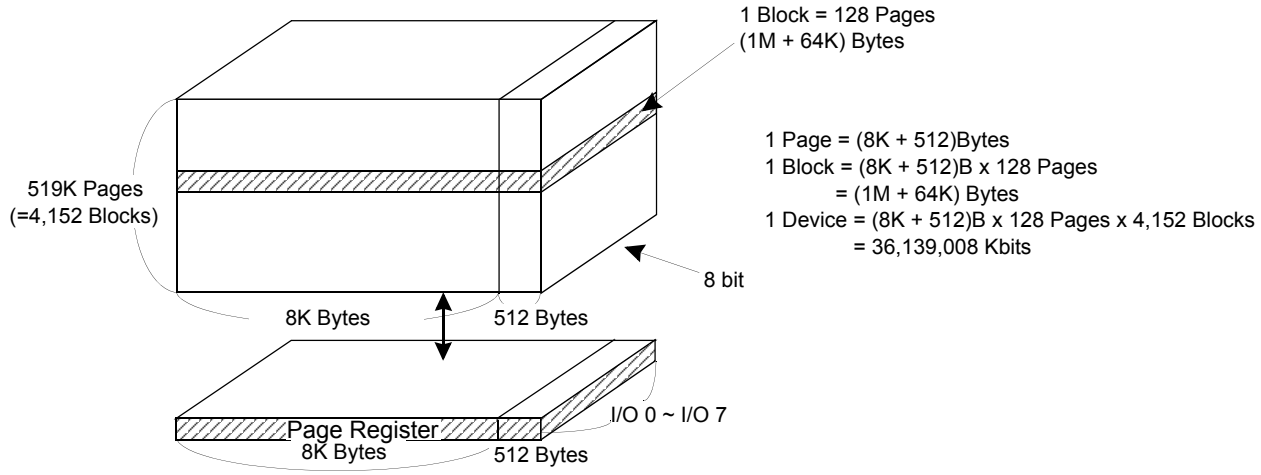
Caution :

Any undefined command inputs are prohibited except for above command set of Table 1.

K9GBGD8X0M Functional Block Diagram



K9GBGD8X0M Array Organization



1 Page = (8K + 512)Bytes
1 Block = (8K + 512)B x 128 Pages
= (1M + 64K) Bytes
1 Device = (8K + 512)B x 128 Pages x 4,152 Blocks
= 36,139,008 Kbits

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1st Cycle	A_0(1)	A_1	A_2	A_3	A_4	A_5	A_6	A_7
2nd Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	*L	*L
3rd Cycle	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}
4th Cycle	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	A_{28}	A_{29}
5th Cycle	A_{30}	A_{31}	A_{32}	A_{33}	A_{34}*	*L	*L	*L

Column Address

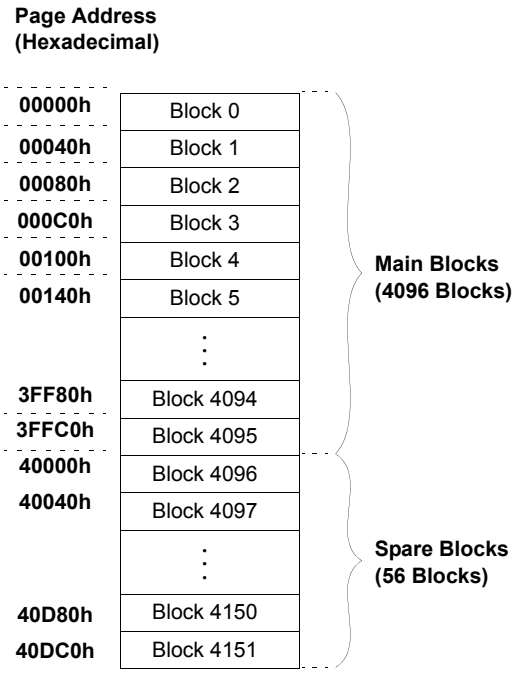
Row Address;
Page Address : A_{14} ~ A_{20}
Plane Address : A_{21}
Block Address : A_{22} ~ A_{33}
***A_{34} : chip Add of K9PFGD8X5M**

NOTE :
1) A_0 must be set to "Low".
2) Data input / outputUnit Shuld be 2-byte(16bit).

Column Address : Starting Address of the Register.
*** L must be set to "Low".**
*** The device ignores any additional input of address cycles than required.**

Spare Blocks Arrangement

The device has 56 spare blocks to increase valid blocks. Extended blocks can be accessed by the following address.



2.0 Product Introduction

2.1 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol		Rating	Unit
Voltage on any pin relative to V_{SS}		V_{CC}		-0.6 to + 4.6	V
		V_{IN}	3.3VccQ	-0.6 to + 4.6	
			1.8VccQ	-0.2 to + 4.6	
		$V_{I/O}$	3.3VccQ	-0.6 to + 4.6	
			1.8VccQ	-0.2 to + 4.6	
Temperature Under Bias	K9XXGD8XXM-XCB0	T_{BIAS}		-10 to +125	°C
Storage Temperature	K9XXGD8XXM-XCB0	T_{STG}		-65 to +150	°C
Short Circuit Current		Ios		5	mA

NOTE :
1) Minimum DC voltage is -0.2V on input/output pins. During transitions to 1.8VccQ, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is 2.4V at 1.8VccQ which, during transitions, may overshoot to VccQ+2.0V for periods <20ns.
2) Minimum DC voltage is -0.6V on input/output pins. During transitions to 3.3VccQ, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is 4.6V at 3.3VccQ which, during transitions, may overshoot to VccQ+2.0V for periods <20ns.
3) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.2 RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9XXGD8XXM-XCB0 :T_A=0 to 70°C)

Parameter	Symbol	K9XXGD8XXM			Unit
		Min	Typ.	Max	
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Voltage	V_{SS}	0	0	0	V
Supply Voltage for I/O signaling (1.8V)	VccQ	1.7	1.8	1.95	V
Supply Voltage for I/O signaling (3.3V)	VccQ	2.7	3.3	3.6	V
Ground Voltage for I/O signaling	VssQ	0	0	0	V

2.3 DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions		1.8VccQ			3.3VccQ			Unit
					Min	Typ	Max	Min	Typ	Max	
Operating Current	Page Read with Serial Access	I_{CC1}	tRC=15ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA		-	30	50	-	30	50	mA
	Program	I_{CC2}	-								
	Erase	I_{CC3}	-								
Stand-by Current(CMOS)		I_{SB}(1)	$\overline{CE}$=VccQ-0.2, $\overline{WP}$=0V/VccQ		-	10	50	-	10	50	μA
Input Leakage Current		I_{LI}(2)	V_{IN}=0 to VccQ(max)		-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}(2)	V_{OUT}=0 to VccQ(max)		-	-	±10	-	-	±10	
Input High Voltage		V_{IH}(3)	-		0.8 xVccQ	-	VccQ +0.3	0.8 xVccQ	-	VccQ +0.3	V
Input Low Voltage, All inputs		V_{IL}(3)	-		-0.3	-	0.2 xVccQ	-0.3	-	0.2 xVccQ	
Output High Voltage Level		V_{OH}	1.8VccQ	3.3VccQ	VccQ-0.1	-	-	2.4	-	-	
			I_{OH}=-100μA	I_{OH}=-400μA							
Output Low Voltage Level		V_{OL}	I_{OL}= 100μA	I_{OL}= 2.1mA	-	-	0.1	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.2V	V_{OL}=0.4V	3	4	-	8	10	-	mA

NOTE :
1. The typical value of the K9LCGD8X1M's I_{SB} is 20μA and maximum value is 100μA.
   The typical value of the K9HDGD8X5M's I_{SB} is 40μA and maximum value is 200μA.
   The typical value of the K9PFGD8X7M's I_{SB} is 80μA and maximum value is 400μA.
2. The maximum value of the K9LCGD8X1M's I_{LI} and I_{LO} are ±20μA.
   The maximum value of the K9HDGD8X5M's I_{LI} and I_{LO} are ±40μA.
   The maximum value of the K9PFGD8X7M's I_{LI} and I_{LO} are ±80μA.
3. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to VccQ +0.4V for durations of 20ns or less.
4. Typical value is measured at V_{cc}=3.3V, TA=25°C. Not 100% tested.

2.4 VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
K9GBGD8X0M	N_{VB}	4,036	-	4,152	Blocks
K9LCGD8X1M		8,072		8,304	
K9HDGD8X5M		16,144		16,608	
K9PFGD8X7M		32,288		33,216	
K9PFGD8X5M					

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3) The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

2.5 AC TEST CONDITION

(K9XXGD8XXM-XCB0: TA=0 to 70°C,VCC=2.7V~3.6V, unless otherwise noted)

Parameter	K9XXGD8XXM
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	VccQ/2
Output Load	1 TTL GATE and CL= 5pF(K9GBGD8X0M, K9LCGD8X1M, K9HDGD8X5M)
	1 TTL GATE and CL= 3pF(K9PFGD8X7M,K9PFGD8X5M)

2.6 CAPACITANCE(TA=25°C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	K9GBGD8X0M K9LCGD8X1M		K9HDGD8X5M		K9PFGD8X7M K9PFGD8X5M		Unit
			Min	Max	Min	Max	Min	Max	
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	-	13	-	23	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	-	13	-	23	pF

NOTE :
1) Capacitance is periodically sampled and not 100% tested.

2.7 MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(5clock)
H	L	L	↑	H	X	H	Write Mode	Command Input
L	H	L	↑	H	X	H		Address Input(5clock)
L	L	L	H	H	↓↑	H	Data Input	
L	L	L	H	↓↑	↓↑	X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	0V/V_{CC}(2)	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

2.8 Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	2	5	ms
Dummy Busy Time for Multi Plane Program	t_{DBSY}		0.5	1	µs
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	t_{BERS}	-	1.5	10	ms

NOTE :
1)Typical program time is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2) Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25°C temperature.

2.9 AC Timing Characteristics for toggle-mode NAND flash

Parameter	Sym-bol	66Mbps		80Mbps		133Mbps		Unit
		Min	Max	Min	Max	Min	Max	
CLE/ALE Setup Time	t_{CALS}	15	-	15	-	15	-	ns
CLE/ALE Hold Time	t_{CALH}	5	-	5	-	5	-	ns
DQS Setup Time for data input start	t_{CDQSS}	100	-	100	-	100	-	ns
DQS Hold Time for data input finish	t_{CDQSH}	100	-	100	-	100	-	ns
Command Write cycle to Address Write cycle Time for Random data input	t_{CWAW}	300	-	300	-	300	-	ns
$\overline{CE}$ Setup Time	t_{CS}	20	-	20	-	20	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	5	-	5	-	ns
Command/Address Setup Time	t_{CAS}	5	-	5	-	5	-	ns
Command/Address Hold Time	t_{CAH}	5	-	5	-	5	-	ns
Data Setup Time	t_{DS}	4	-	3.3	-	2.0	-	ns
Data Hold Time	t_{DH}	3.6	-	3	-	1.8	-	ns
Write Cycle Time	t_{WC}	25	-	25	-	25	-	ns
$\overline{WE}$ High pulse width	t_{WH}	11	-	11	-	11	-	ns
$\overline{WE}$ Low pulse Width	t_{WP}	11	-	11	-	11	-	ns
Address to Data Loading Time	t_{ADL}	300	-	300	-	300	-	ns
Data Transfer from Cell to Register	t_R	-	100	-	100	-	100	µs
Ready to $\overline{RE}$ High	t_{RR}	20	-	20	-	20	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10	-	10	-	10	-	ns
ALE Low to $\overline{RE}$ Low	t_{AR}	10	-	10	-	10	-	ns
CLE to $\overline{RE}$ Low	t_{CLR}	10	-	10	-	10	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	-	100	-	100	ns
Read Cycle Time	t_{RC}	30	-	25	-	15	-	ns
$\overline{RE}$ High pulse width	t_{REH}	13	-	11	-	6.5	-	ns
$\overline{RE}$ Low pulse width	t_{RP}	13	-	11	-	6.5		ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	-	30	-	30	ns
CLE High to Output Hi-Z	t_{CLHZ}	-	30	-	30	-	30	ns
Data Strobe Cycle Time	t_{DSC}	30	-	25	-	15	-	ns
DQS Input Low Pulse Width	t_{DQSL}	13	-	11	-	6.5	-	ns
DQS Input High Pulse Width	t_{DQSH}	13	-	11	-	6.5	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	120	-	120	-	120	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random data out	t_{WHR2}	300	-	300	-	300	-	ns

$\overline{RE}$ to DQS and DQ delay	t_{DQSRE}	-	25	-	25	-	25	ns
Read Preamble	t_{RPRE}	15	-	15	-	15	-	ns
Read Postamble	t_{RPST}	tDQSRE+0.5xtRC	-	tDQSRE+0.5xtRC	-	tDQSRE+0.5xtRC	-	ns
Read Postamble Hold Time	t_{RPSTH}	5		5		5	-	ns
Write Preamble	t_{WPRE}	15		15		15	-	ns
Write Postamble	t_{WPST}	6.5		6.5		6.5	-	ns
Write Postamble Hold Time	t_{WPSTH}	5		5		5	-	ns
Output skew among data output and corresponding DQS	t_{DQSQ}	-	2.5	-	2	-	1.4	ns
DQS hold skew factor	t_{QHS}	-	2.5	-	2	-	1.4	ns
Output hold time from DQS	t_{QH}	$t_{QH} = t_{REH/tRP} - t_{QHS}$						ns
Output data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$						ns
Device Resetting Time (Read/Program/Erase)	t_{RST}(1)	10/30/100						μs

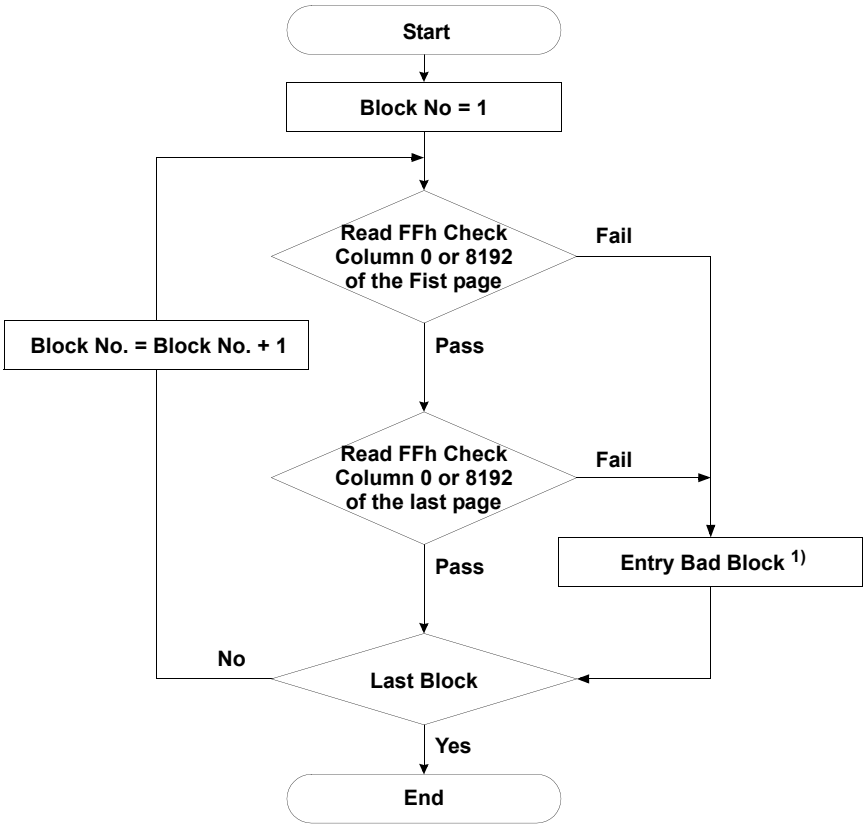
3.0 NAND Flash Technical Notes

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the shipment.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the first or the last page of every initial invalid block has non-FFh data at the column address of 8,192.The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart. Any intentional erasure of the initial invalid block information is prohibited.



Flow chart to create initial invalid block table.

Note:

1. No erase operation is allowed to detected bad blocks.

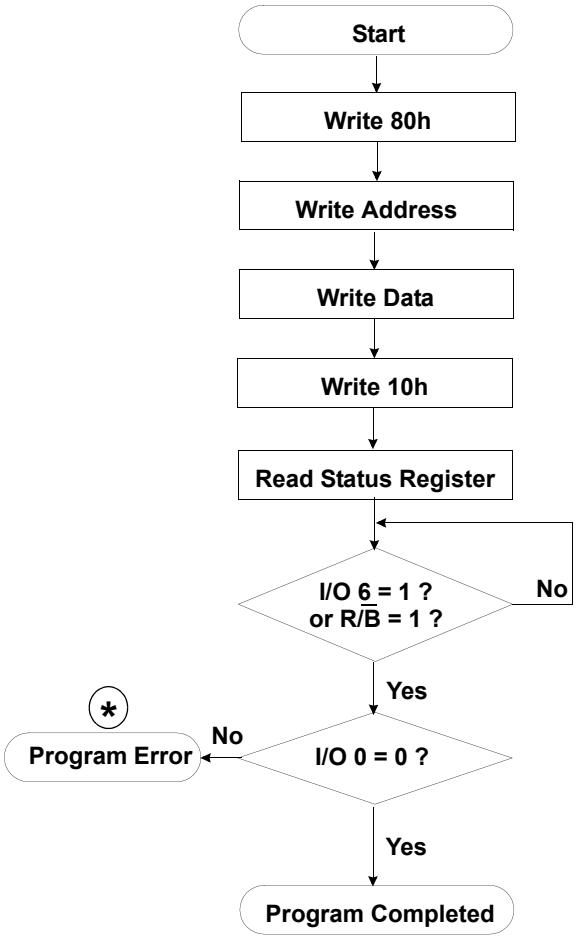
3.3 Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to TBD-Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> RS Code, BCH Code etc.
Example) 8bit correction / 1KByte

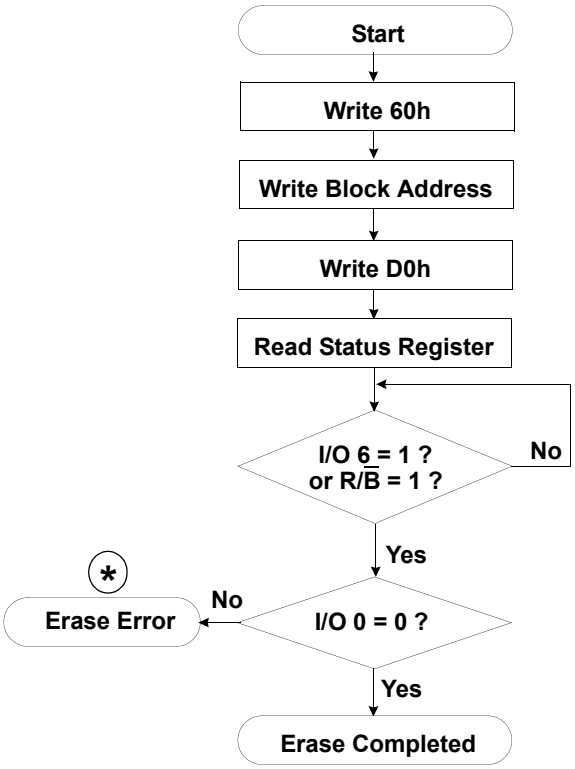
Program Flow Chart



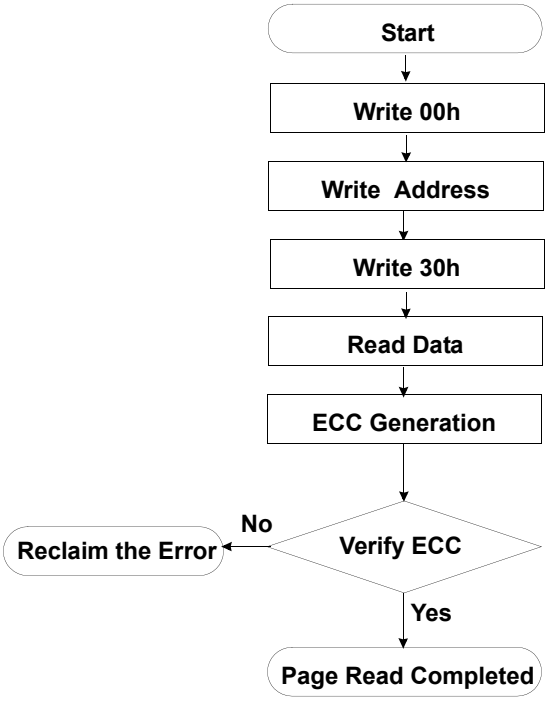
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes (Continued)

Erase Flow Chart

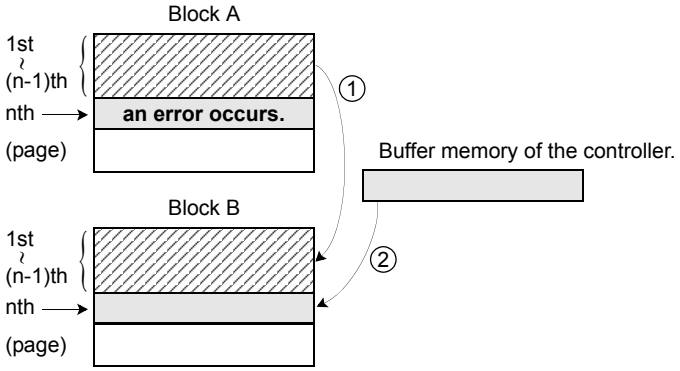


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

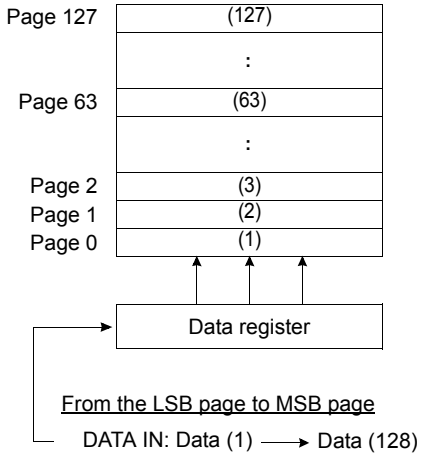
Block Replacement

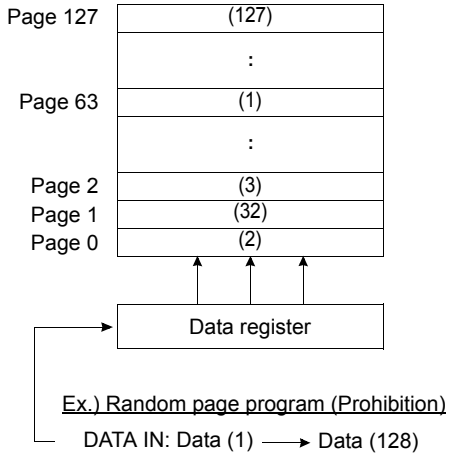


* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.





NOTE :

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9XXGD8XXM	I/O 0 ~ I/O 7	8,704byte	A0~A7	A8~A13	A14~A21	A22~A29	A30~A33
K9PFGD8X5M	I/O 0 ~ I/O 7	8,704byte	A0~A7	A8~A13	A14~A21	A22~A29	A30~A34

3.5 Interleaving Operation

K9PFGD8X5M device is composed of two chips sharing $\overline{CE}$ pin. It provides interleaving operation between two chips.
This interleaving operation improves the system throughput almost twice compared to non-interleaving operation.

At first, the host issues a operation command to one of the LSB chips, say (chip #1). Due to DDP device goes into busy state. During this time, MSB chip (chip #2) is in ready state. So it can execute the operation command issued by the host.

After the execution of operation by LSB chip (chip #1), it can execute another operation regardless of MSB chip (chip #2). Before that the host needs to check the status of LSB chip (chip #1) by issuing F1h command. Only when the status of LSB chip (chip #1) becomes ready status, host can issue another operation command. If LSB chip (chip #1) is in busy state, the host has to wait for LSB chip (chip #1) to get into ready state.

Similarly, MSB chip (chip #2) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (chip #2) by issuing F2h command. When MSB chip (chip #2) shows ready state, host can issue another operation command to MSB chip (chip #2).

This interleaving algorithm improves the system throughput almost twice. The host can issue page operation command to each chip individually. This reduces the time lag for the completion of operation.

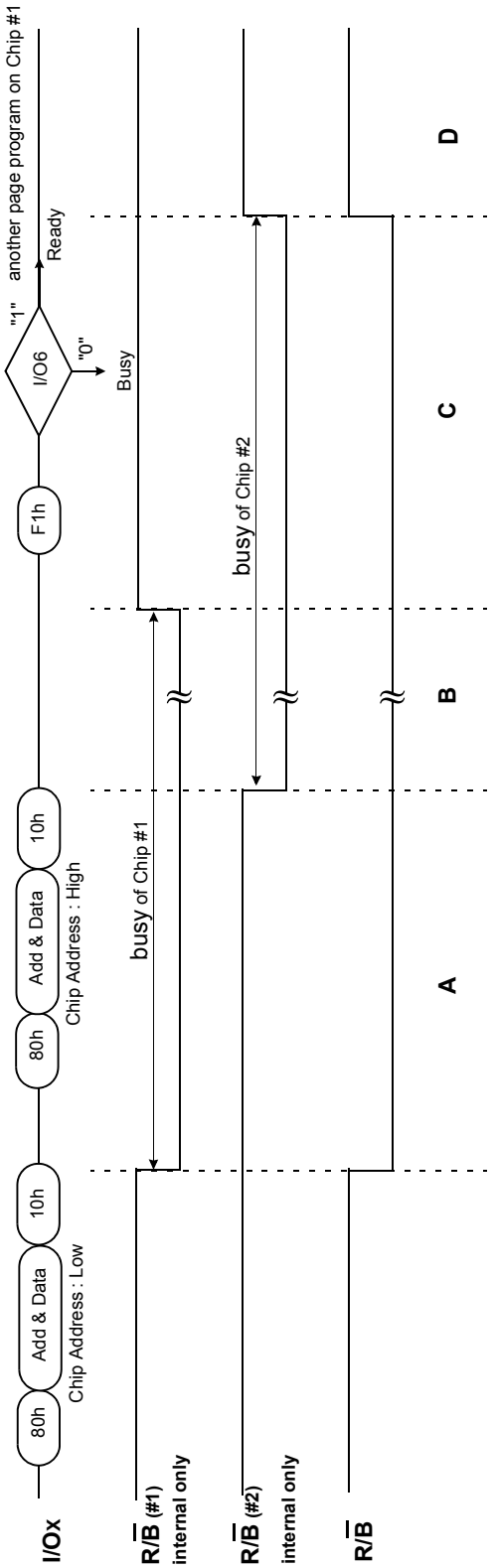
NOTES : During interleave operations, 70h command is prohibited.

Table . F1h/F2h Read Status Register Definition

I/O No.	Page Program	Block Erase	Read	Definition	
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 3	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Not Use	Not Use	Not Use	Don't -cared	
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

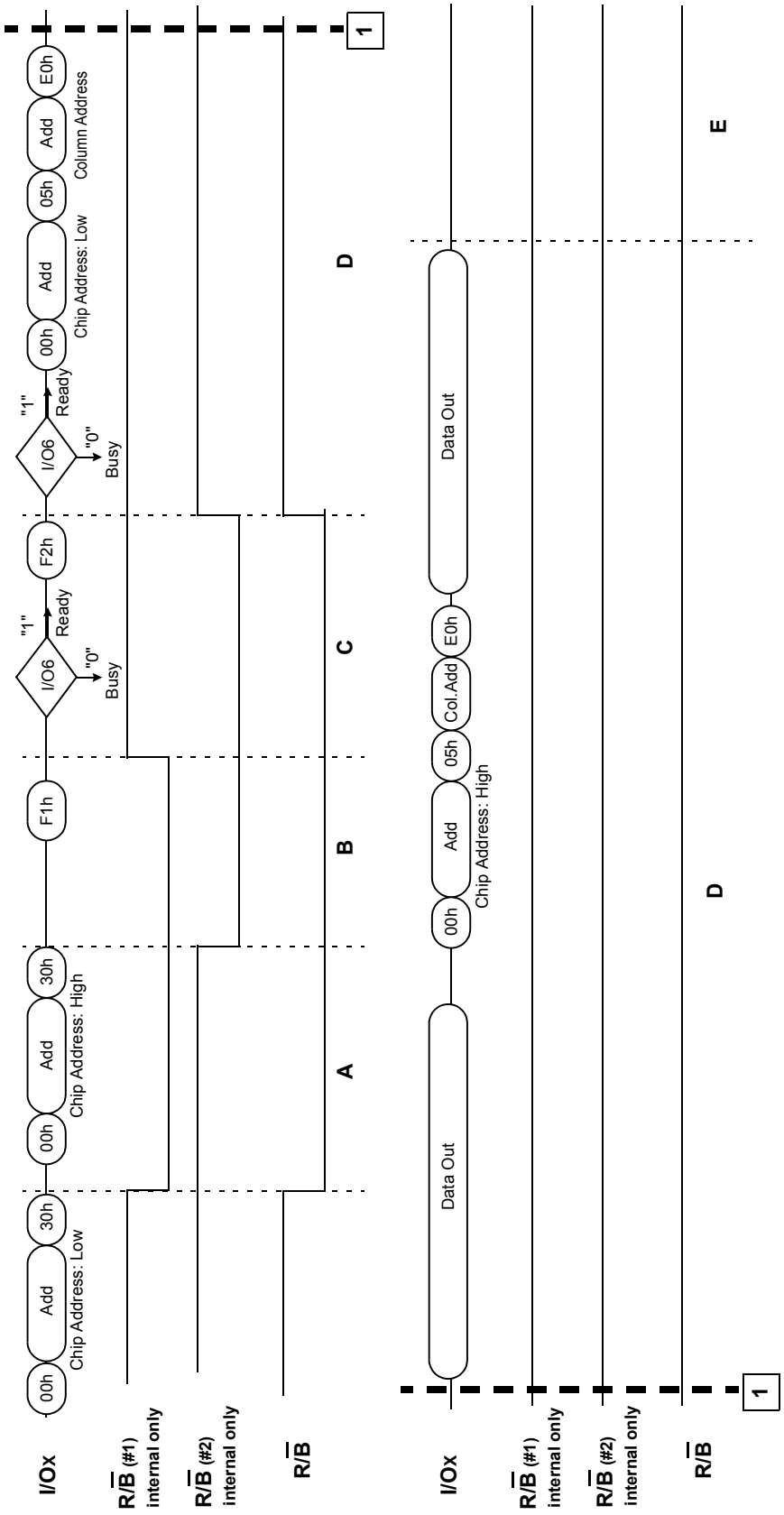
3.5.1Interleaving Page Program



State A : Chip #1 is executing page program operation and chip #2 is in ready state. So the host can issue page program command to chip #2.
State B : Both chip #1 and chip #2 are executing page program operation.
State C : Page program on chip #1 is terminated, but page program on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another page program command to chip #1.
State D : Chip #1 and Chip #2 are ready.

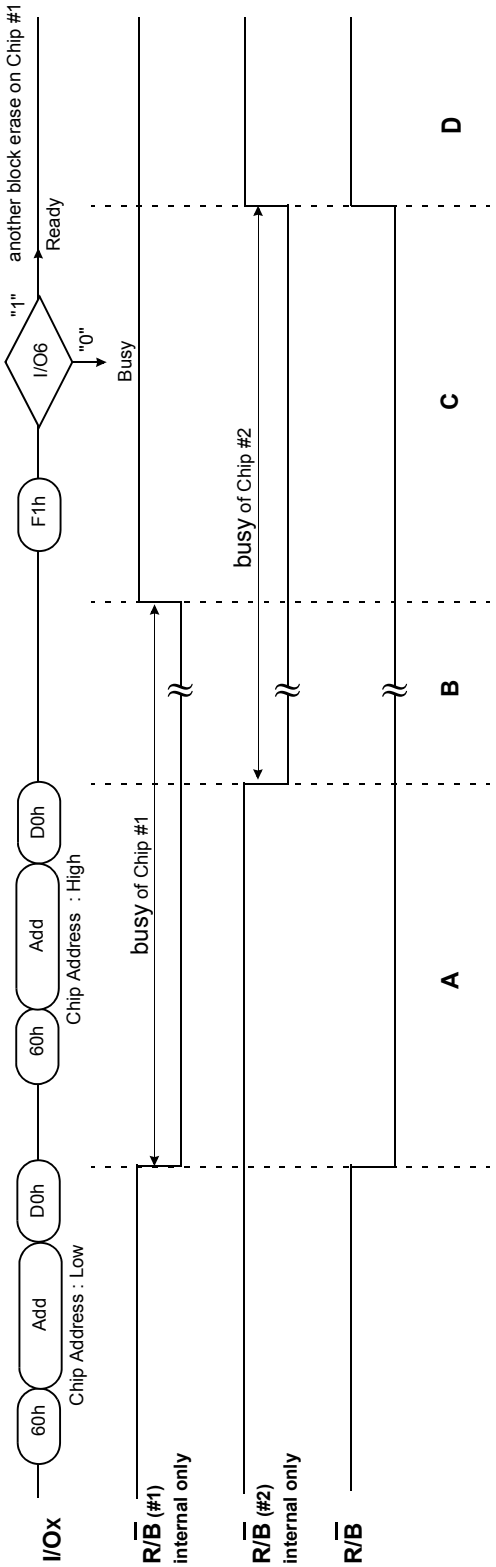
According to the above process, the system can operate page program on chip #1 and chip #2 alternately.

3.5.2 Interleaving Page Read



State A : Chip #1 is executing page read operation, and chip #2 is in ready state. So the host can issue page read command to chip #2.
State B : Both chip #1 and chip #2 are executing page read operation.
State C : Page read on chip #1 is completed and chip #2 is still executing page read operation.
State D : Before the host read the data, the host should check the Ready/Busy status for both chips by F1h and F2h commands.
State E : Chip #1 and Chip #2 are ready.
Note : *F1h command is required to check the status of chip #1.
F2h command is required to check the status of chip #2.

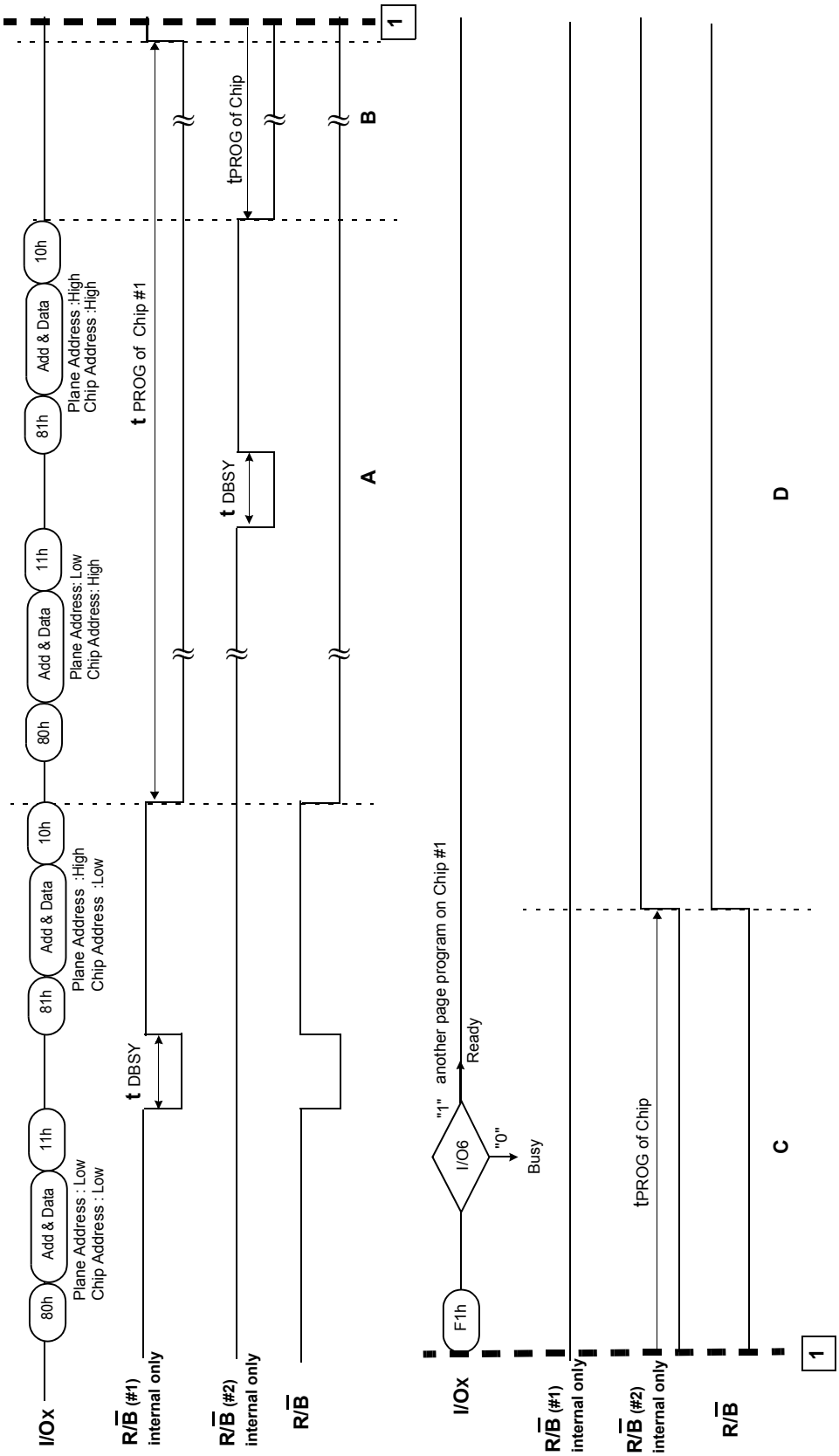
3.5.3 Interleaving Block Erase



State A : Chip #1 is executing block erase operation, and chip #2 is in ready state. So the host can issue block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing block erase operation.
State C : Block erase on chip #1 is terminated, but block erase on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another block erase command to chip #1.
State D : Chip #1 and Chip #2 are ready.

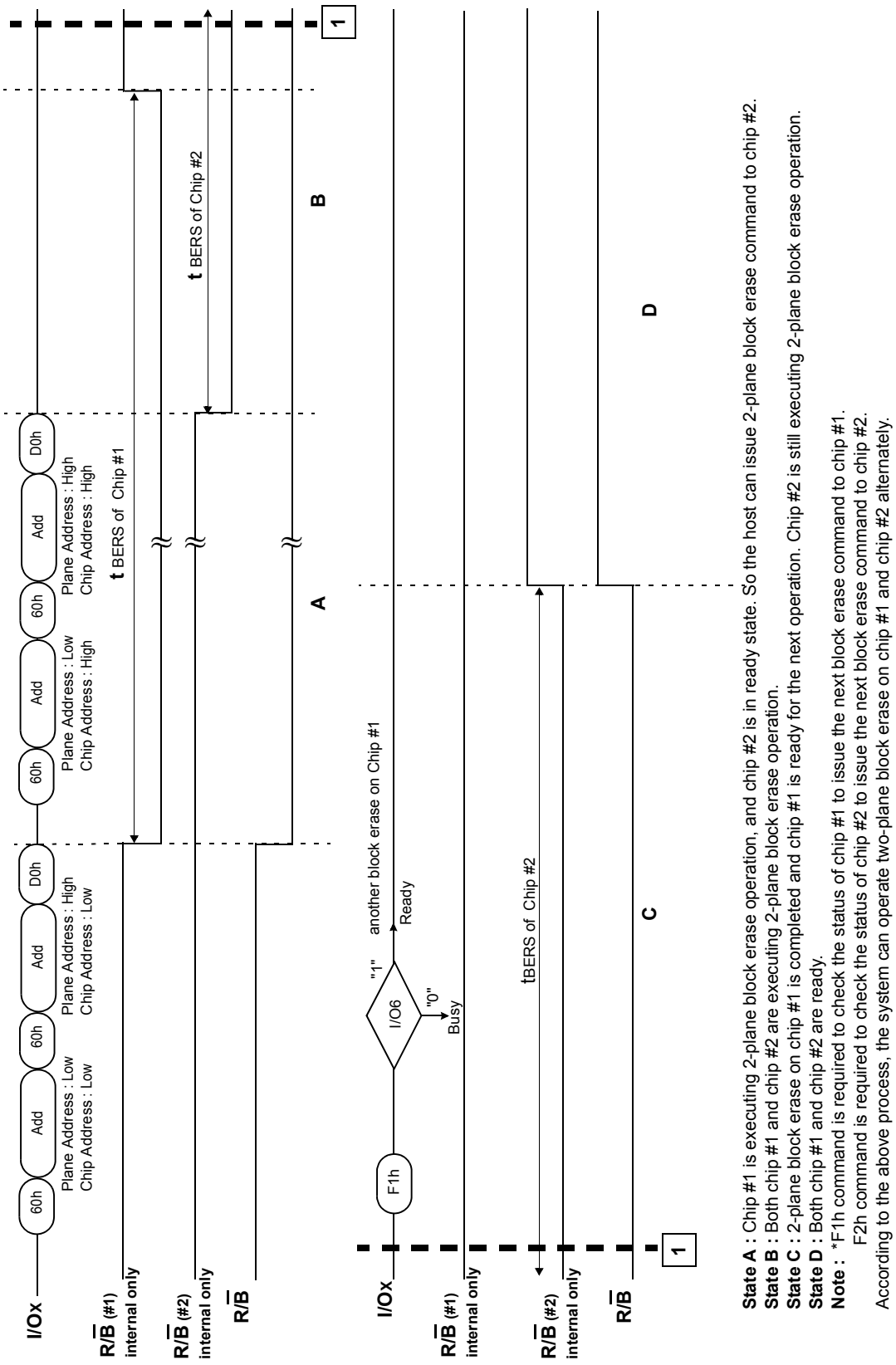
According to the above process, the system can operate block erase on chip #1 and chip #2 alternately.

3.5.4 Interleaving Two-Plane Page Program



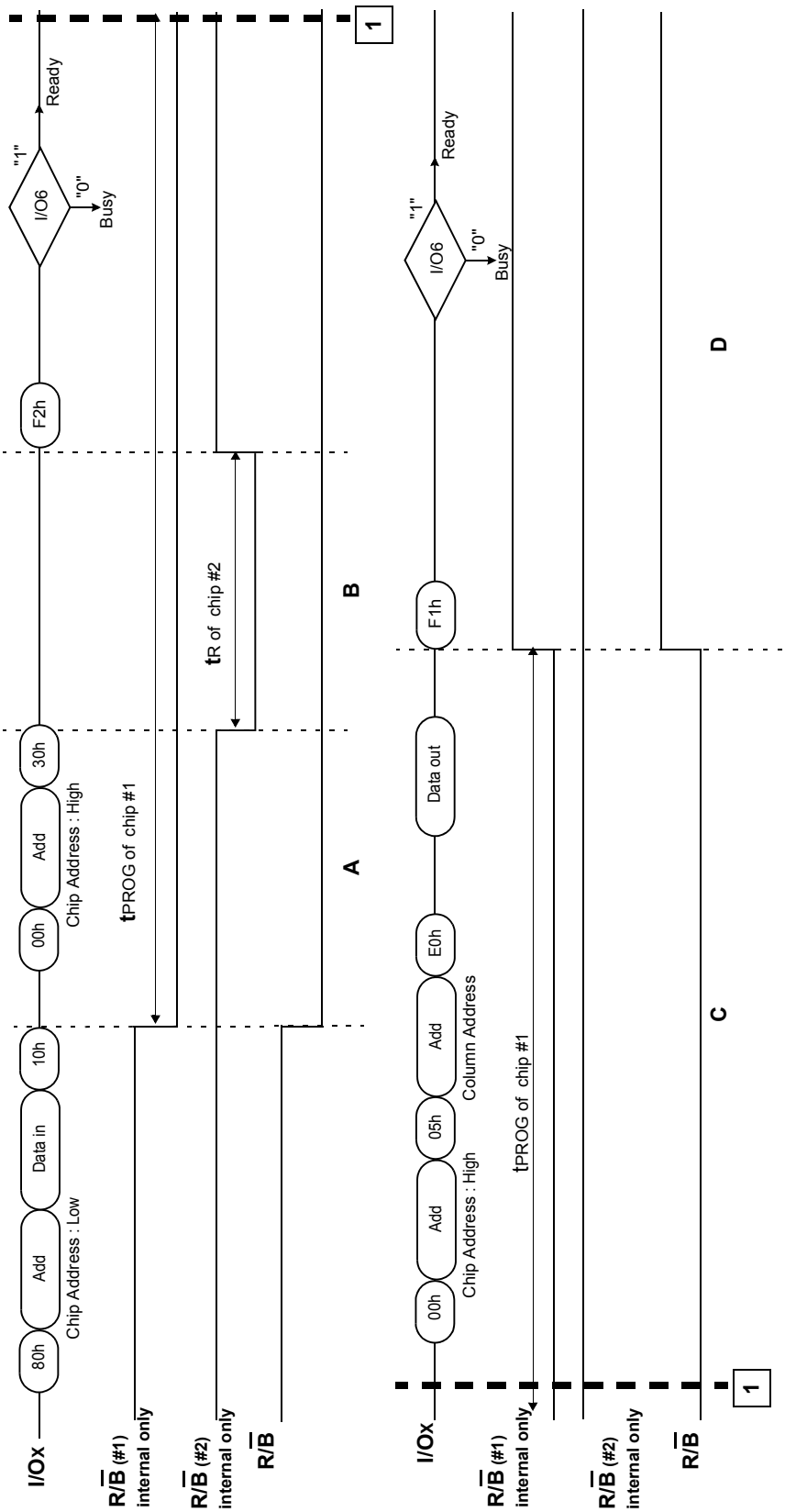
State A : Chip #1 is executing 2-plane page program operation, and chip #2 is in ready state. So the host can issue 2-plane page program command to chip #2.
State B : Both chip #1 and chip #2 are executing 2-plane page program operation.
State C : 2-plane page program on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing 2-plane page program operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next page program command to chip #1.
F2h command is required to check the status of chip #2 to issue the next page program command to chip #2.
According to the above process, the system can operate two-plane page program on chip #1 and chip #2 alternately.

3.5.5 Interleaving Two-Plane Block Erase



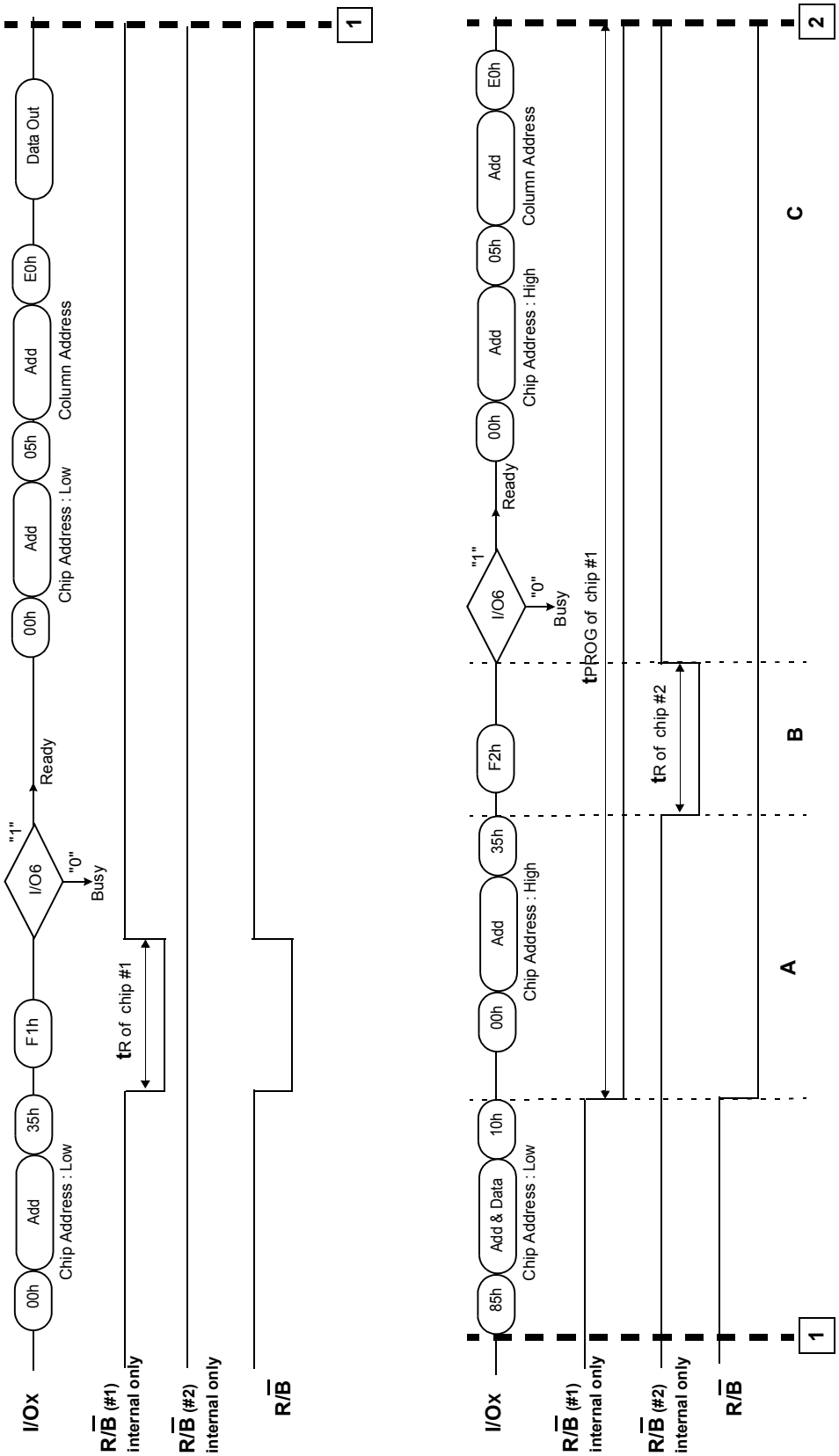
State A : Chip #1 is executing 2-plane block erase operation, and chip #2 is in ready state. So the host can issue 2-plane block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing 2-plane block erase operation.
State C : 2-plane block erase on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing 2-plane block erase operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next block erase command to chip #1.
F2h command is required to check the status of chip #2 to issue the next block erase command to chip #2.
According to the above process, the system can operate two-plane block erase on chip #1 and chip #2 alternately.

3.5.6 Interleaving Read to Page Program

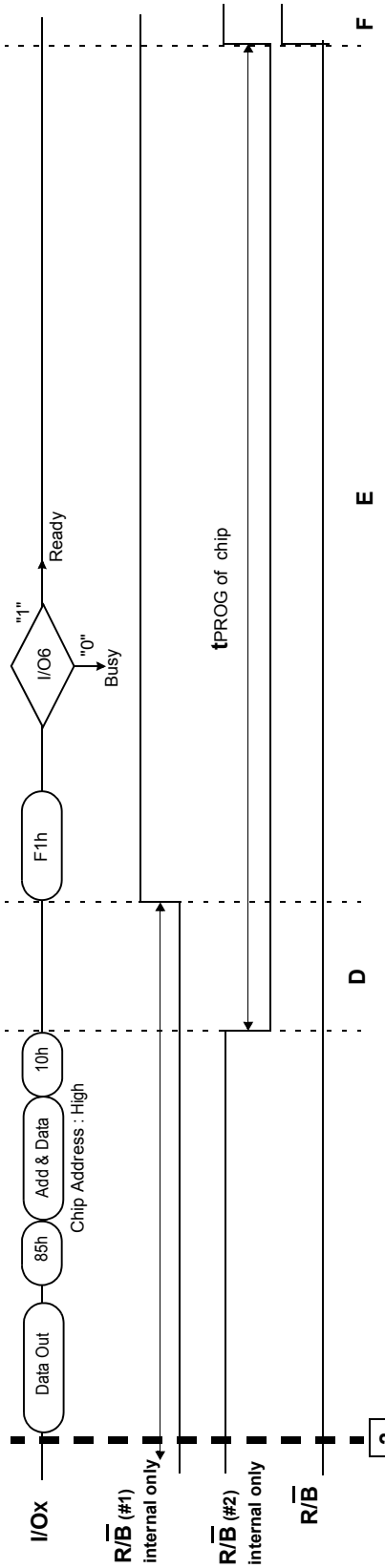


State A : Chip #1 is executing page program operation, and chip #2 is in ready state. So the host can issue read command to chip #2.
State B : Both chip #1 is executing page program operation and chip #2 is executing read operation.
State C : Read operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing page program operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave read to page porgram on chip #1 and chip #2 alternatively.

3.5.7 Interleaving Copy-Back Program (1/2)

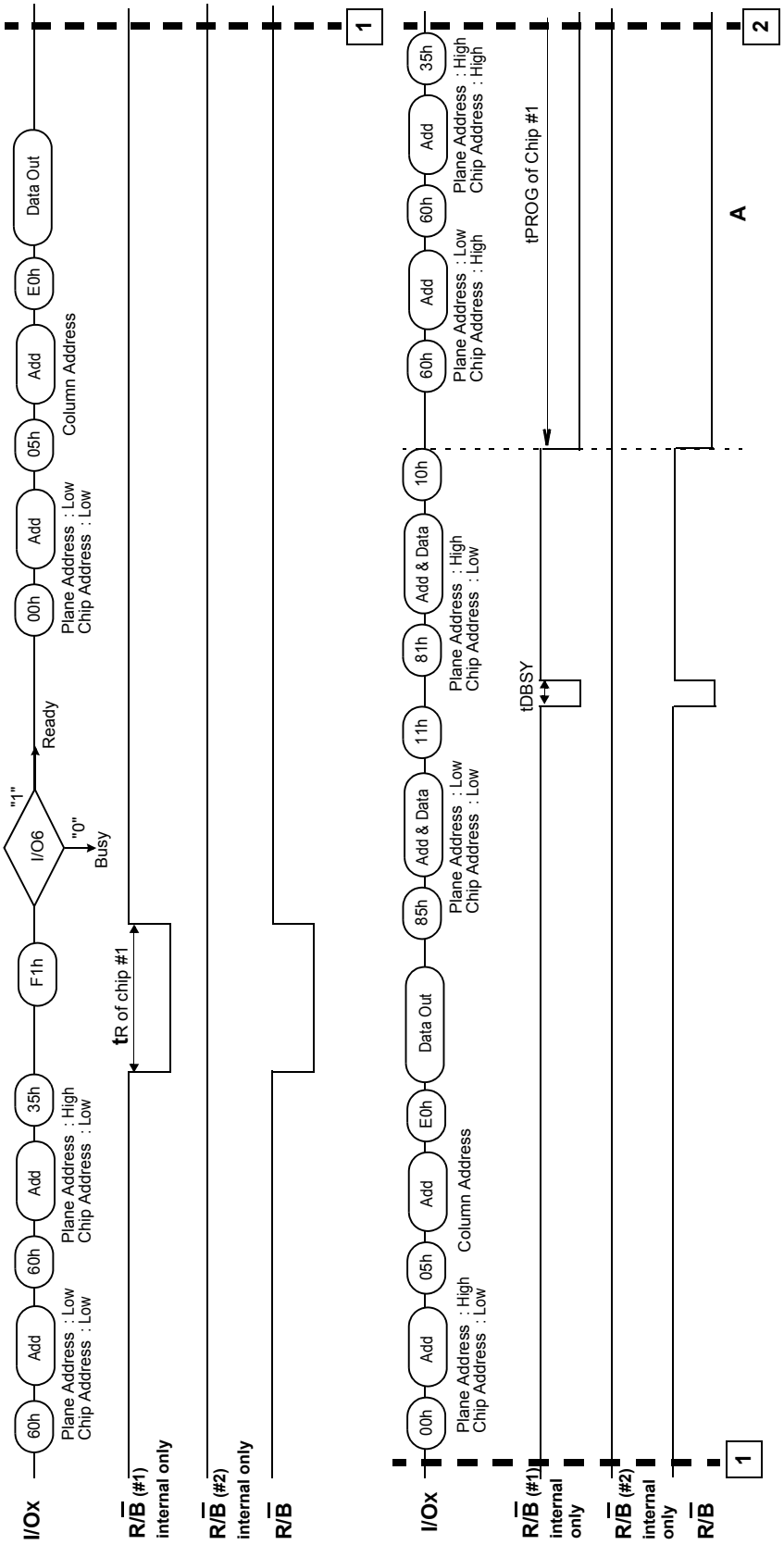


3.5.8 Interleaving Copy-Back Program (2/2)

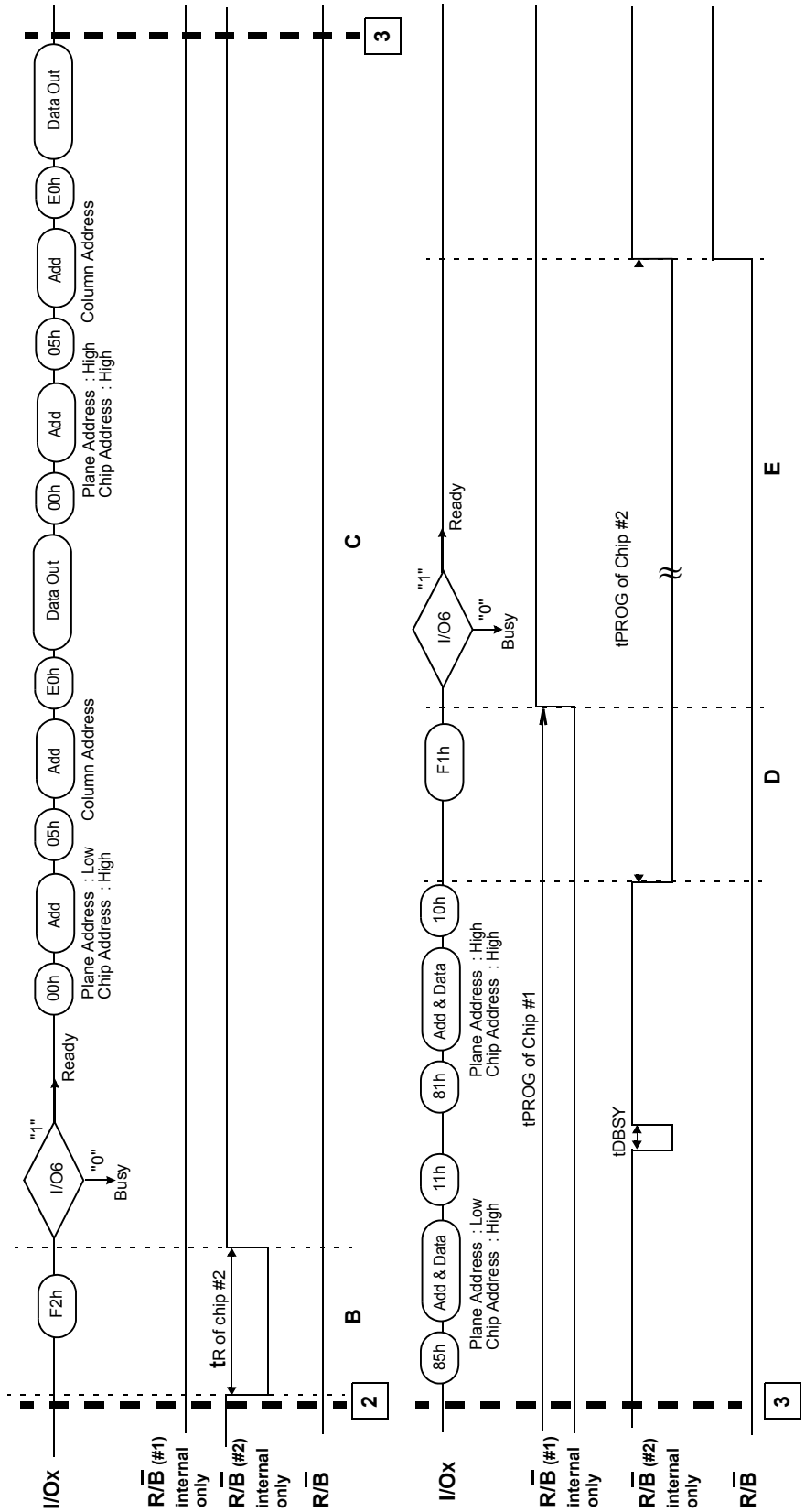


State A : Chip #1 is executing copy-back program operation, and chip #2 is in ready state. So the host can issue read for copy-back command to chip #2.
State B : Chip #1 is executing copy-back program operation and chip #2 is executing read for copy-back operation.
State C : Read for copy-back operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing copy-back program operation.
State D : Both chip #1 and chip #2 are executing copy-back program operation.
State E : Chip #2 is still executing a copy-back program operation, and chip #1 is in ready for the next operation.
State F : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave copy-back program on chip #1 and chip #2 alternatively.

3.5.9 Interleaving Two-Plane Copy Back Program (1/2)



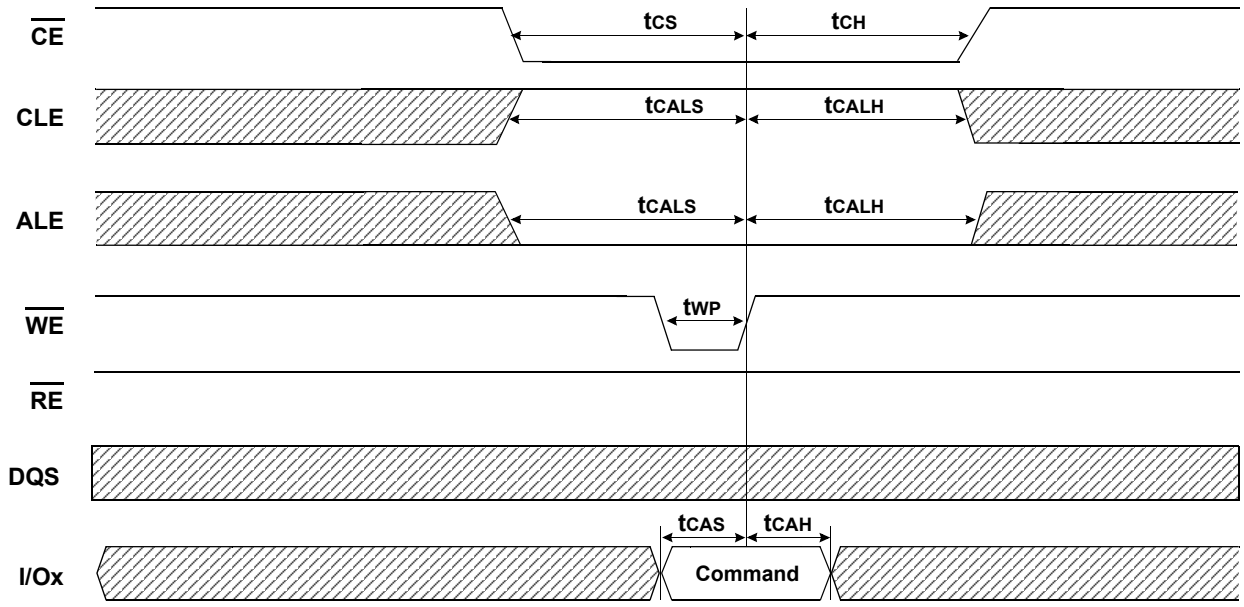
3.5.10 Interleaving Two-Plane Copy Back Program (2/2)



State A : Chip #1 is executing 2-plane copy-back program operation, and chip #2 is in ready state. So the host can issue 2-plane read for copy-back command to chip #2.
State B : Chip #1 is executing 2-plane copy-back program operation and chip #2 is executing 2-plane read for copy-back operation.
State C : 2-plane read for copy-back operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing 2-plane copy-back program operation.
State D : Both chip #1 and chip #2 are executing 2-plane copy-back program operation.
State E : Chip #2 is still executing a 2-plane copy-back program operation, and chip #1 is in ready for the next operation.
State F : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave 2-plane copy-back program on chip #1 and chip #2 alternatively.

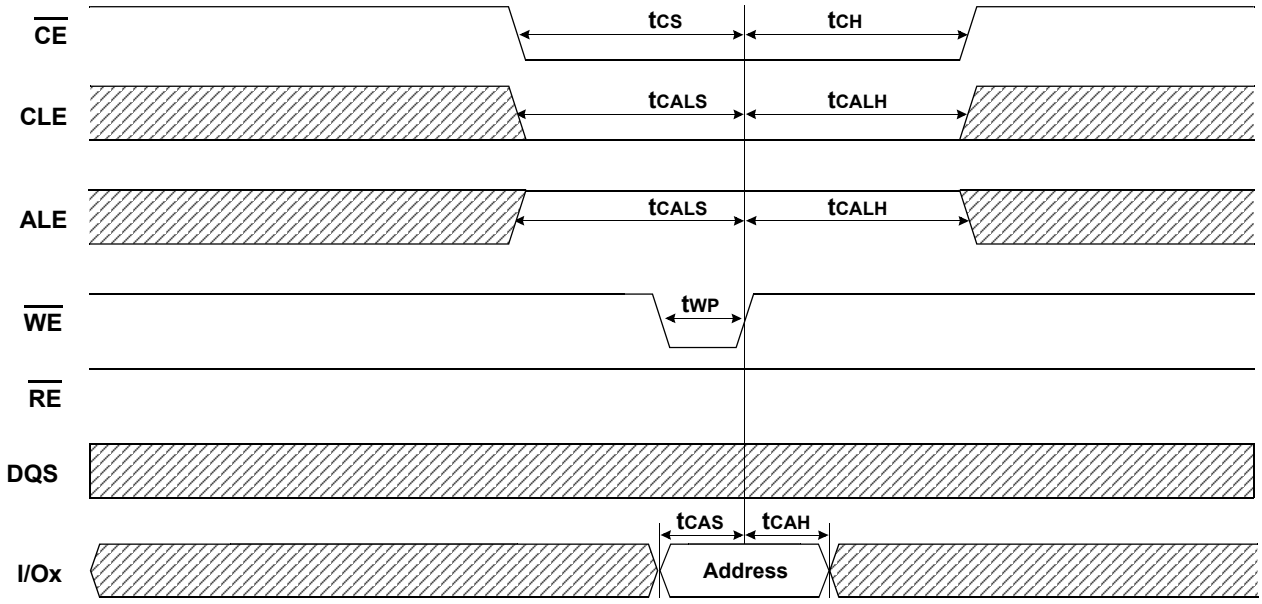
4.0 TIMING DIAGRAMS

4.1 Command Latch Cycle

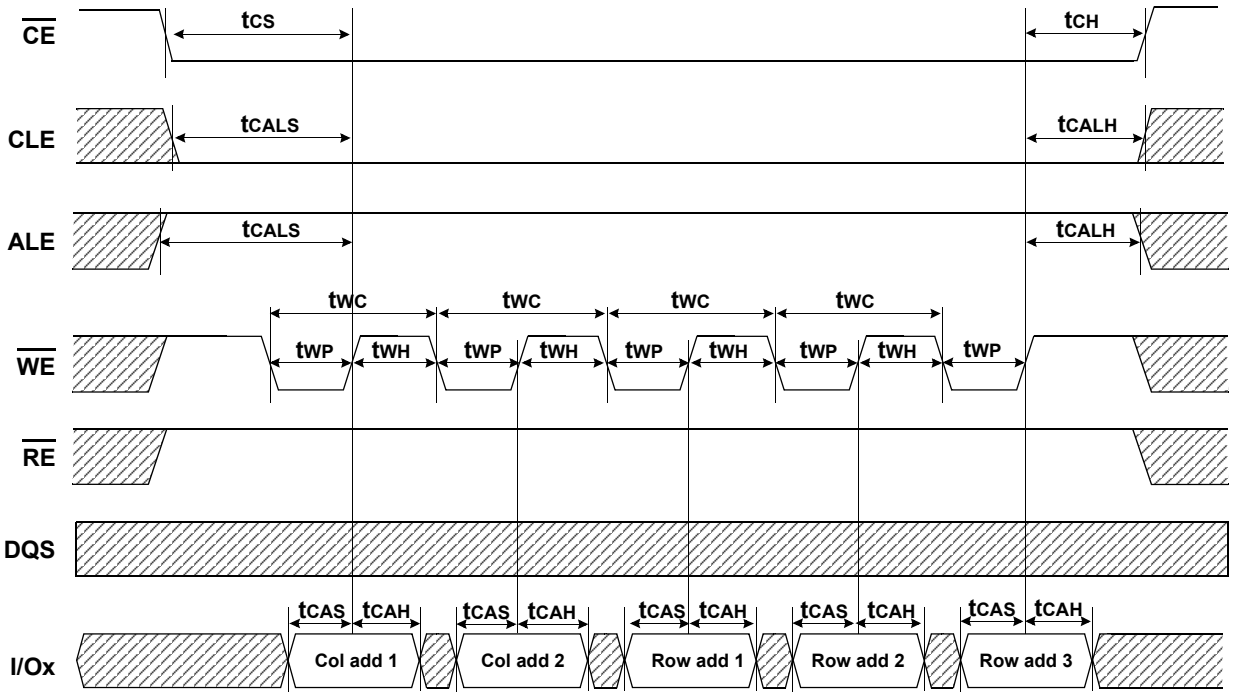


NOTE :
1. Command information is lached by $\overline{WE}$ going high, when $\overline{CE}$ is Low, CLE is High, and ALE is Low.
2. DQS should be set to 'Low' when these commands(85h, 10h, 11h) is input.

4.2 Address Latch Cycle

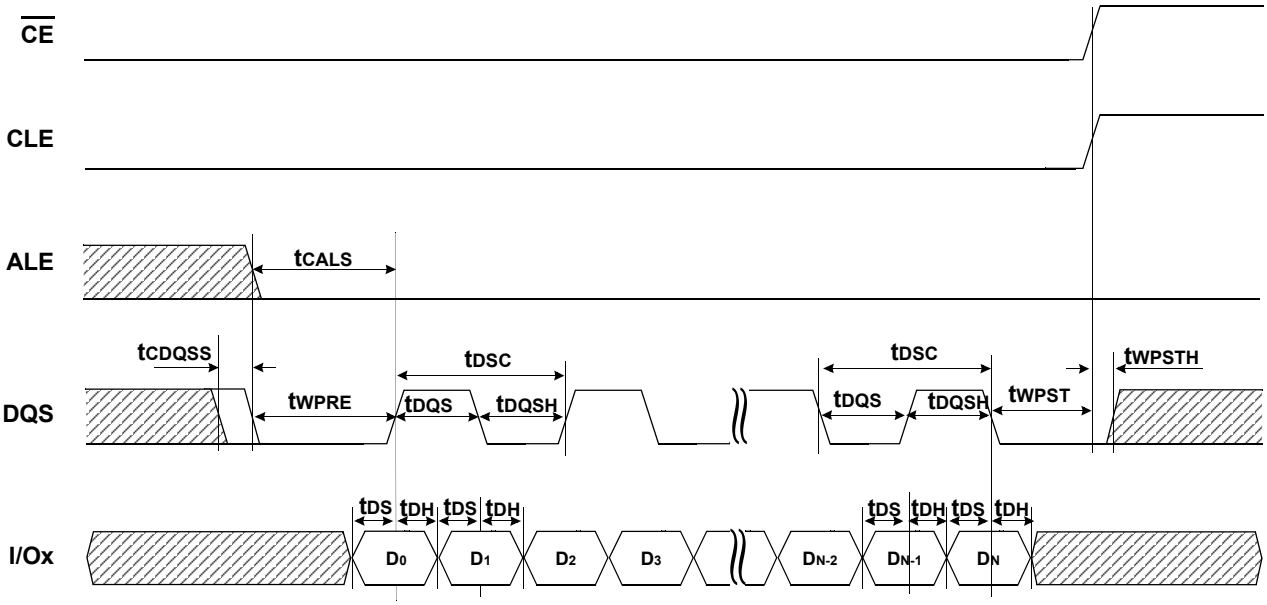


NOTE :
Address information is lached by $\overline{WE}$ going high, when $\overline{CE}$ is Low, CLE is Low, and ALE is High.



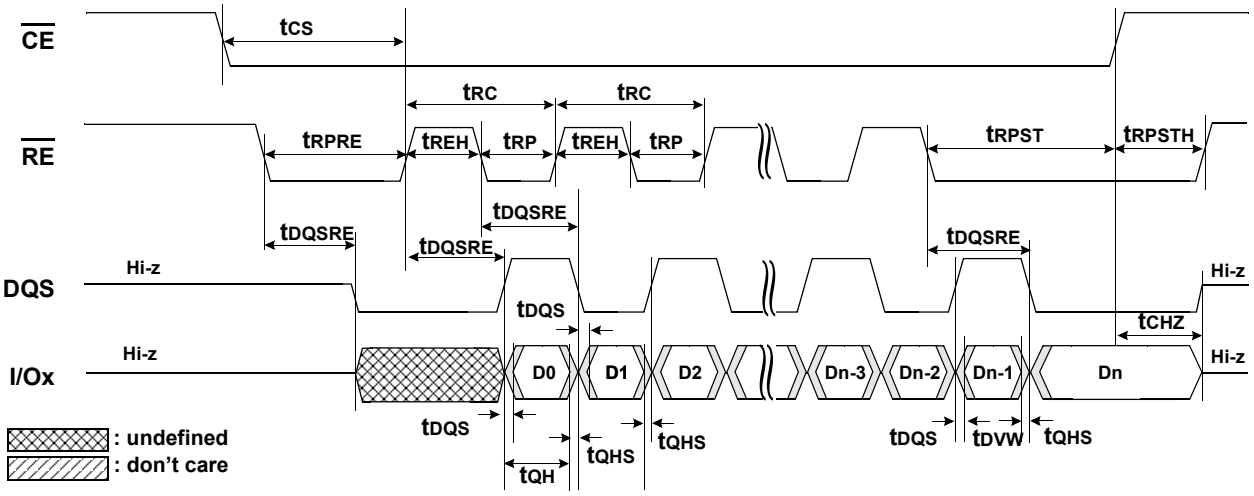
NOTE :
Row address consists of page address and block address.

4.3 Basic Data Input Timing



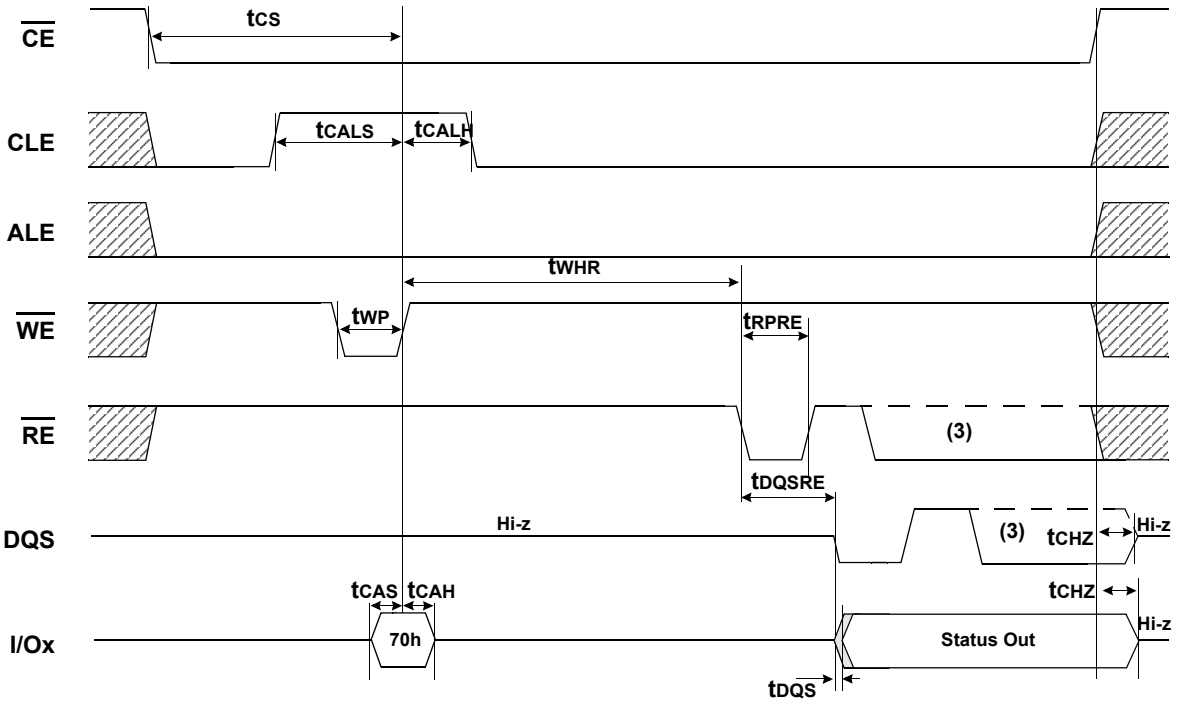
NOTE :
1) Data-input condition should be satisfied before DQS toggling for data input; data-input condition is that $\overline{CE}$ & CLE & ALE are low and $\overline{RE}$ & $\overline{WE}$ are high
2) DQS should be either high or low before data-input condition is set.
3) Data-input condition should be kept during DQS toggling for data input including pre-amble and post-amble time.
4) Becase using toggle DDR interface, an even number of bytes should be always transferred when both data input and data output

4.4 Basic Data Output Timing



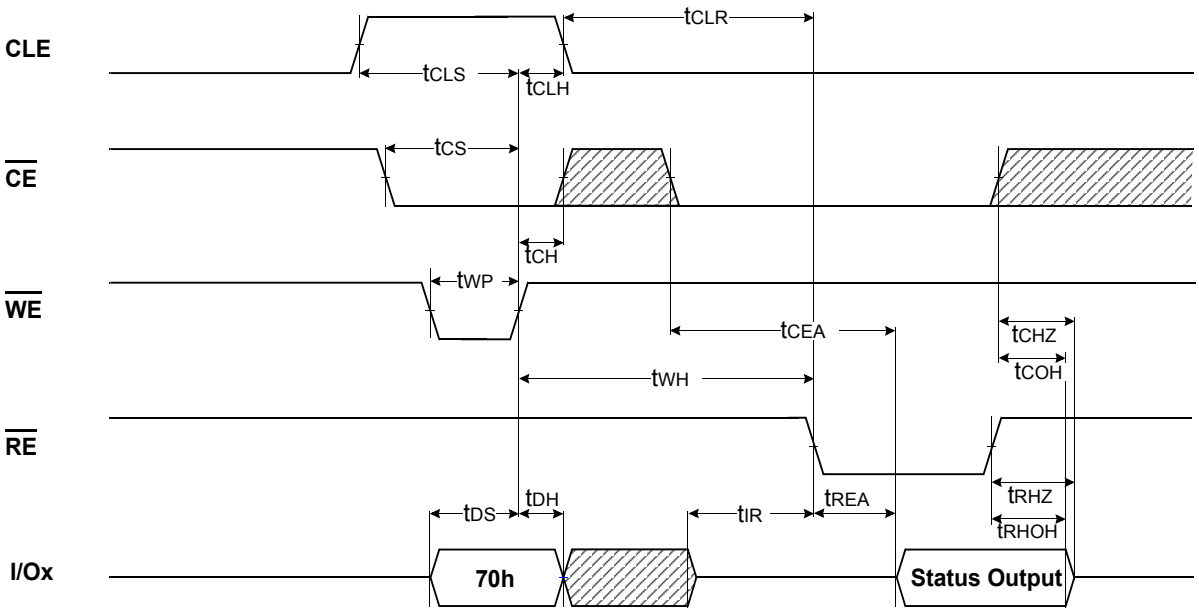
NOTE :
1) Data-output condition should be satisfied before $\overline{RE}$ toggling for data output; data-output condition is that $\overline{CE}$ & CLE & ALE are low and $\overline{WE}$ is high
2) $\overline{RE}$ should be either high or low before data-output condition is set.
3) Data-output condition should be kept during $\overline{RE}$ toggling for data output including pre-amble and post-amble time.
4) DQS and Data out buffers are turned on when $\overline{RE}$ is low for pre-amble operation under data-out condition
5) DQS and Data out buffers turn from valid value to high-z if either $\overline{CE}$ or CLE goes High.
6) an even number of bytes should be always transferred when both data input and data output

4.5 Status Read Cycle

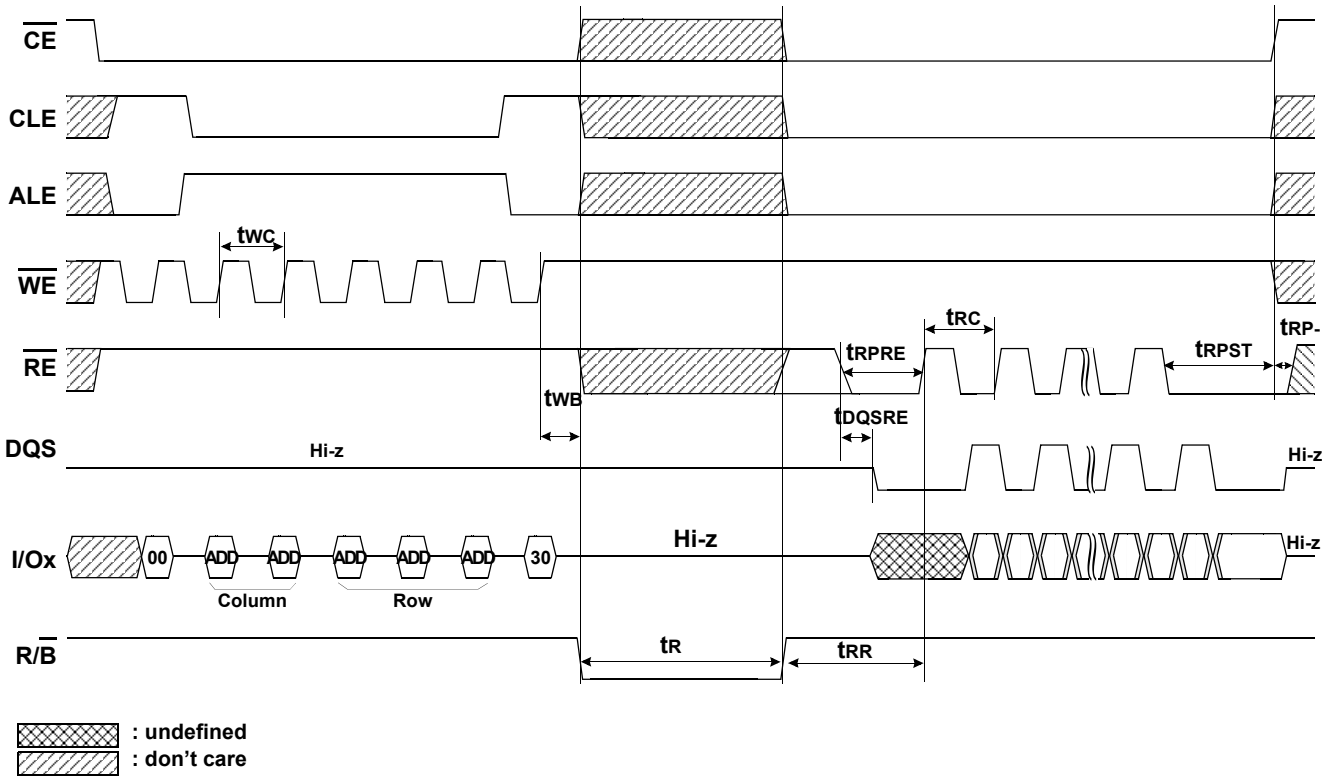


NOTE :
1) Even thougn toggle-mode NAND uses both low and high-going edges of DQS for reads, Status read operation repeates same output until device status changes
2) DQS and Data out buffers turn from valid value to high-z when $\overline{CE}$ or $\overline{CLE}$ goes High
3) $\overline{RE}$ can toggle more than once.

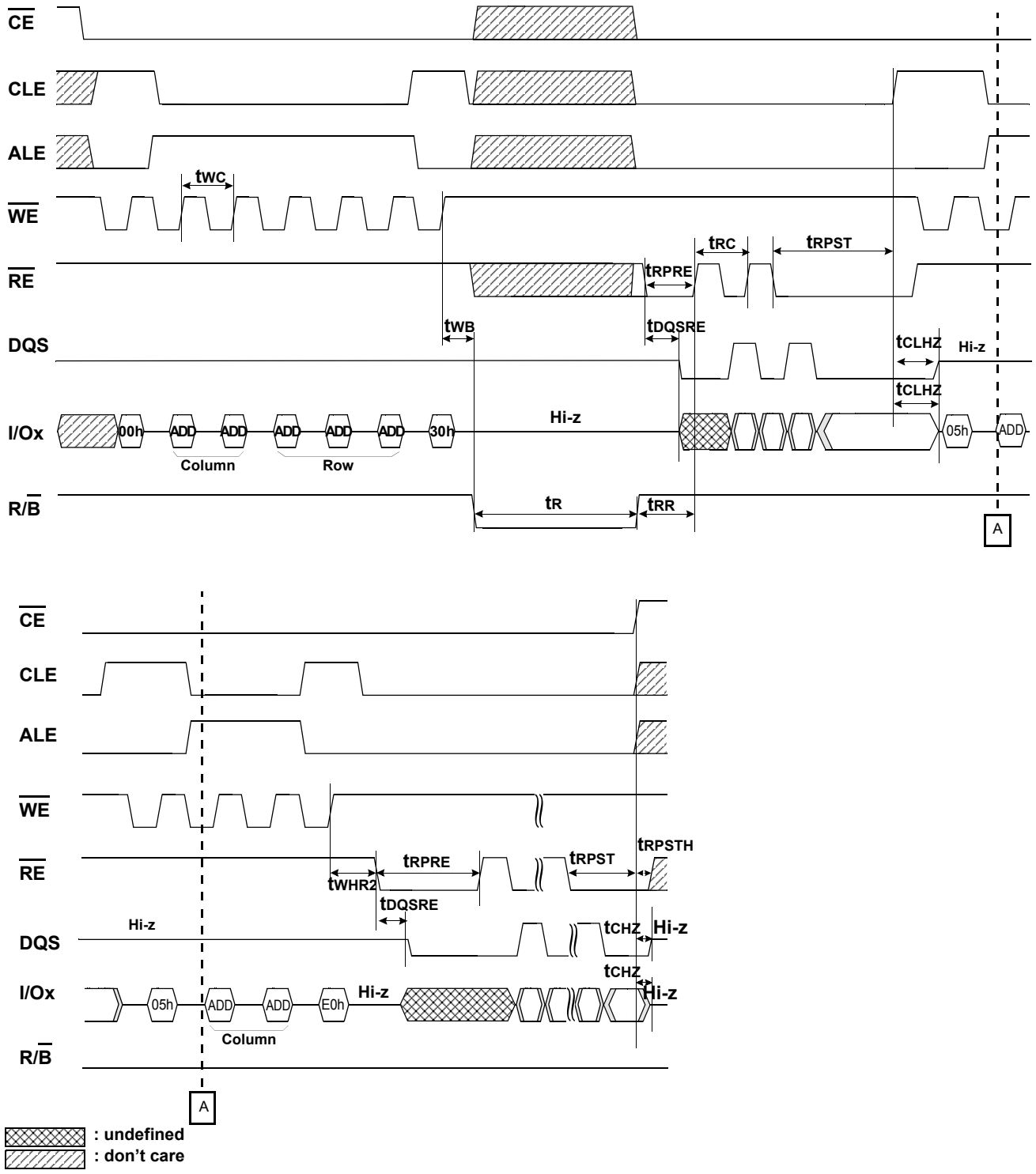
(Statas read cycle before power on seguence .)



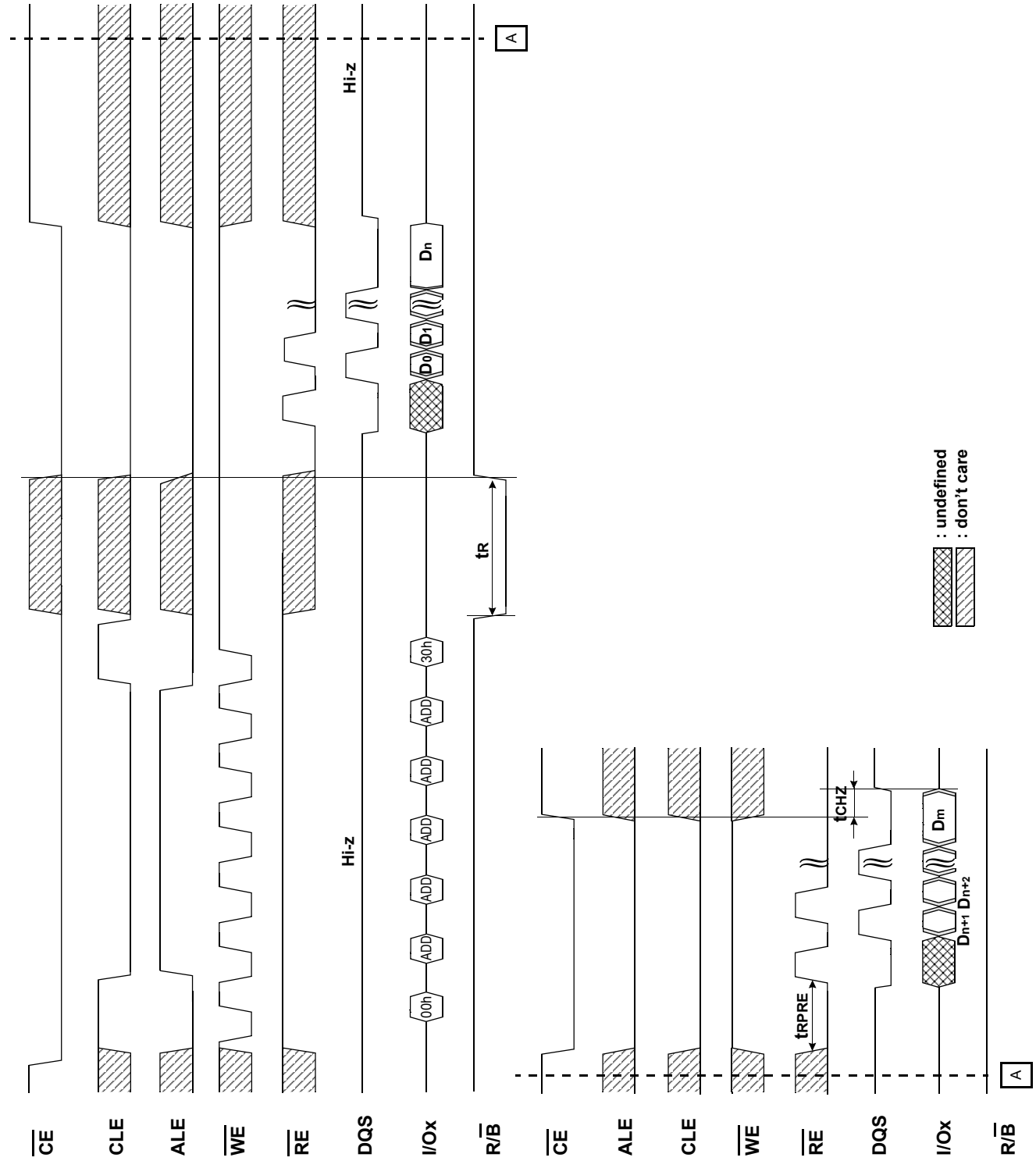
4.6 Read Operation



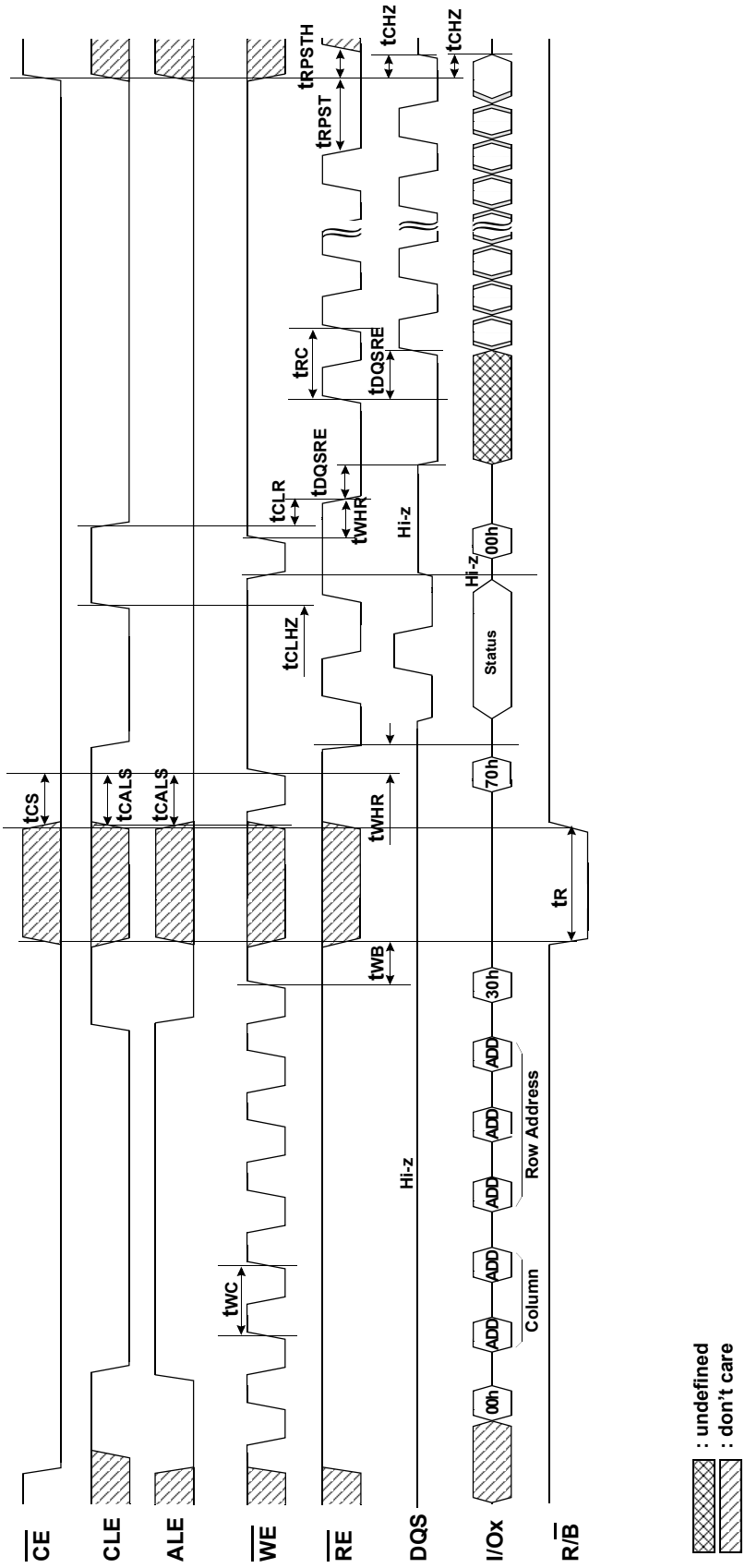
4.7 Page Read Operation with Random Data Output



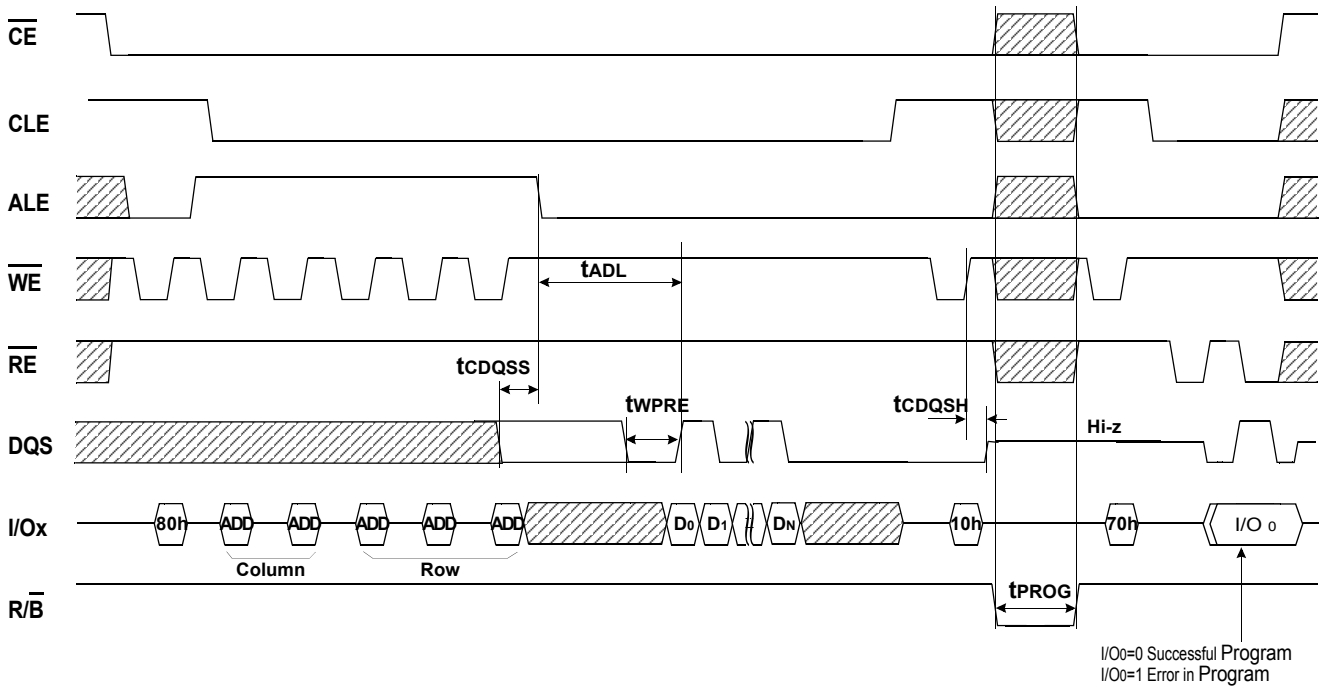
4.8 Read Hold Operation with CE high



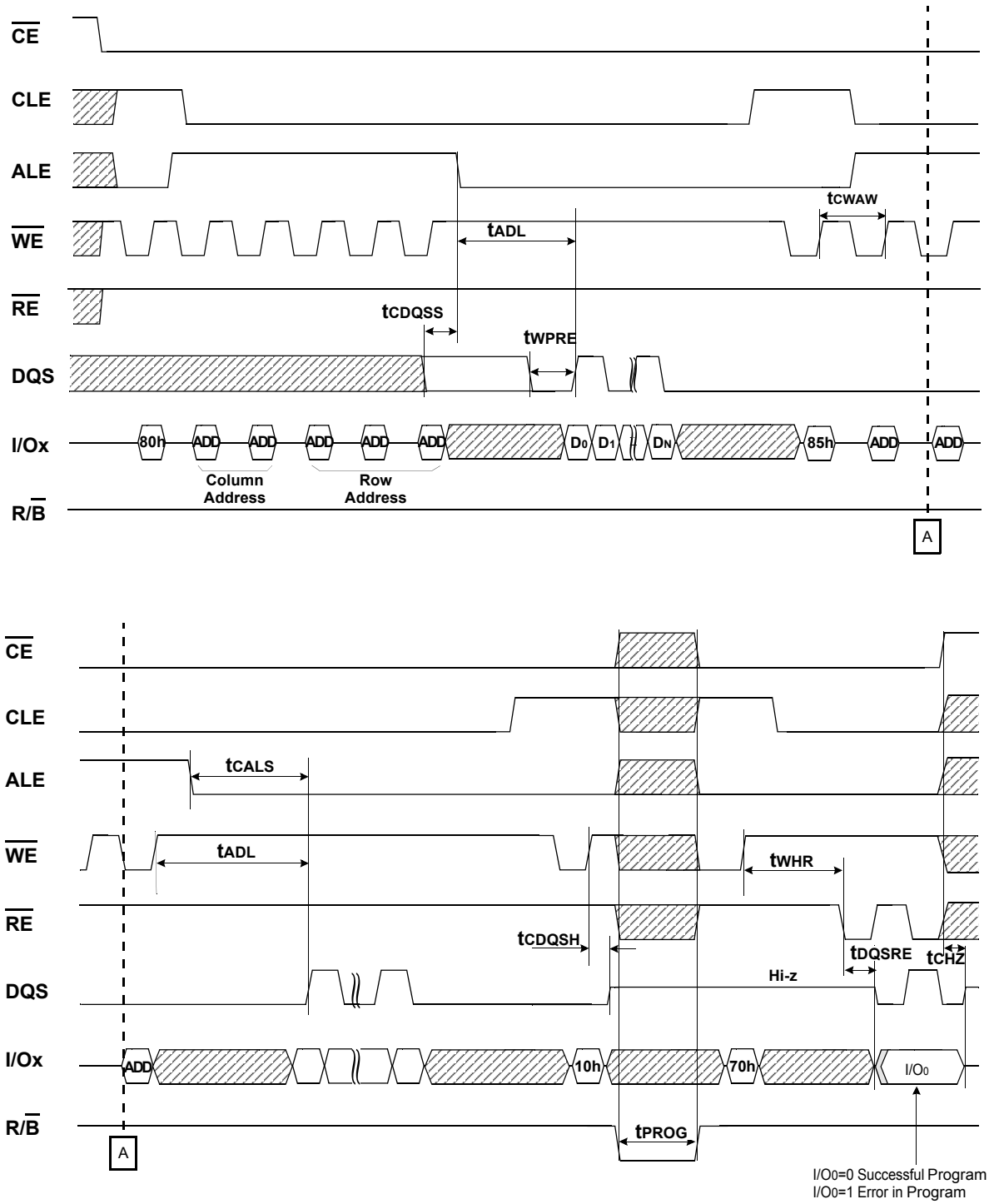
4.9 Data Out After Status Read



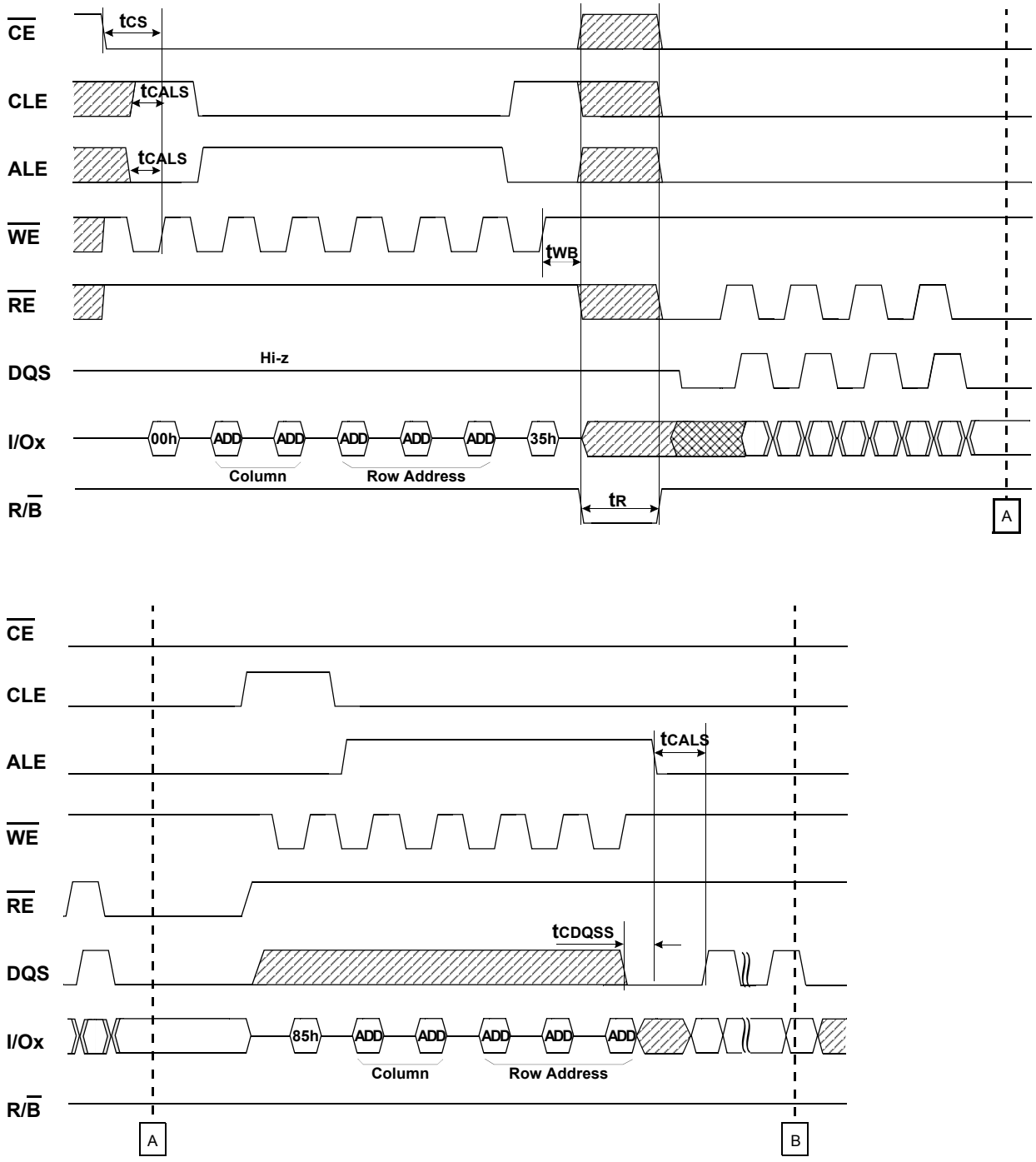
4.10 Page Program Operation



4.11 Page Program Operation with Random Data Input

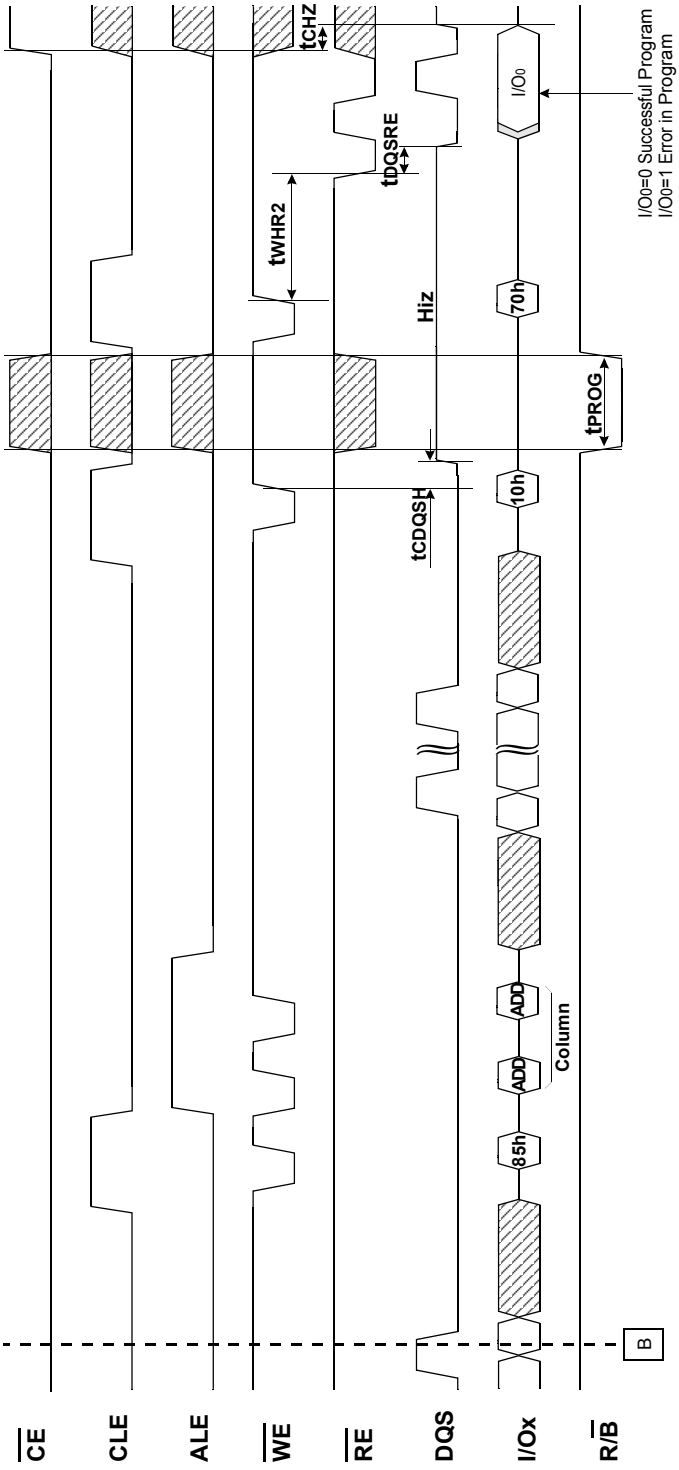


4.12 Copy-Back Program Operation with Random Data Input (1)

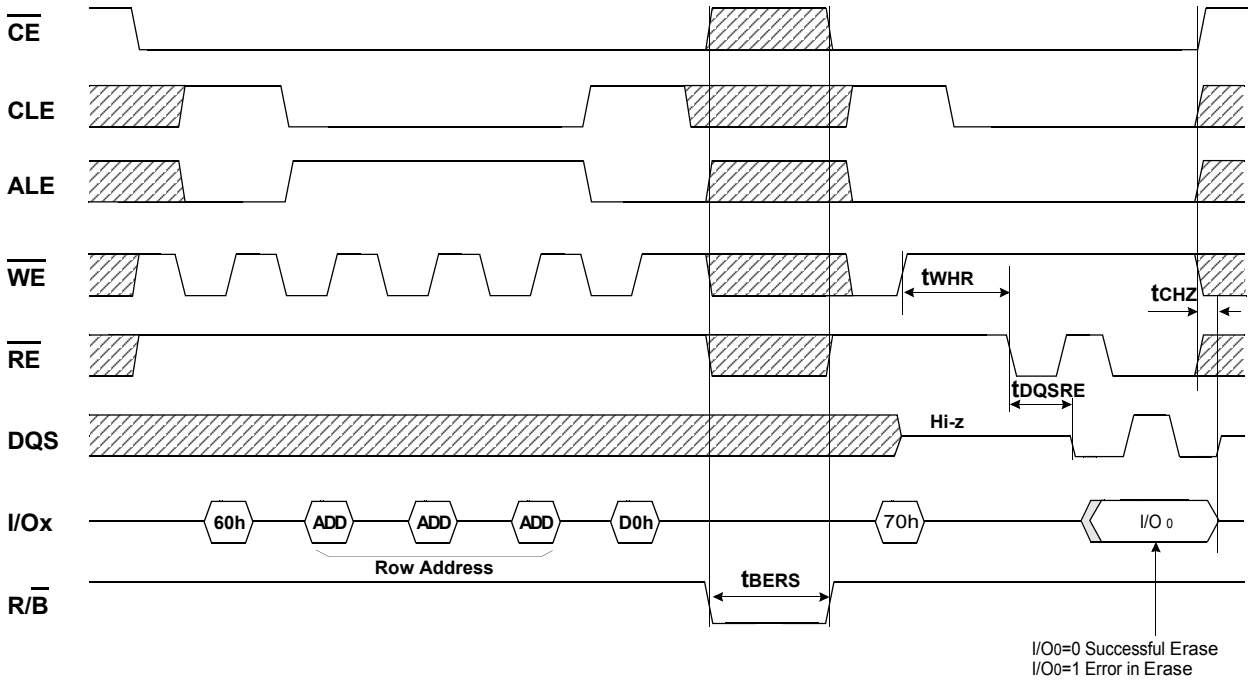


: undefined
: don't care

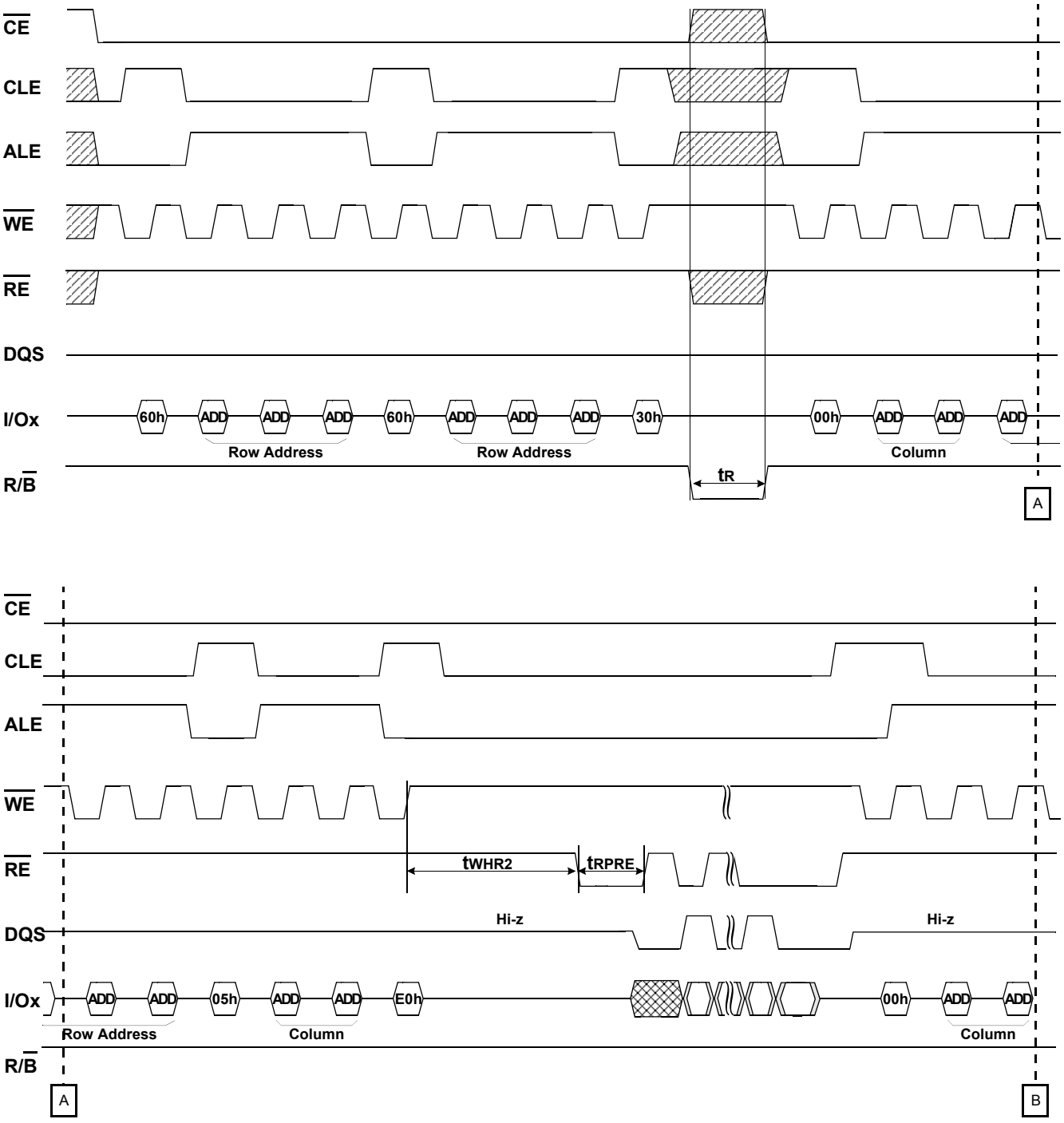
4.13 Copy-Back Program Operation with Random Data Input (2)



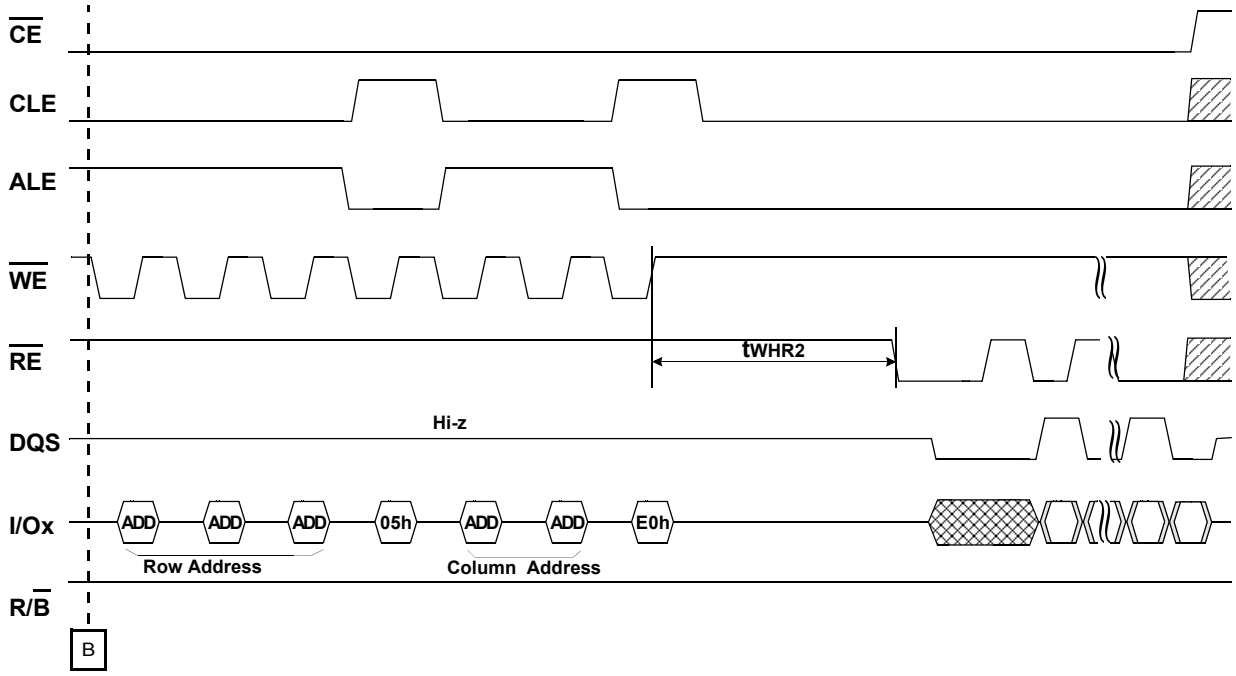
4.14 Block Erase Operation



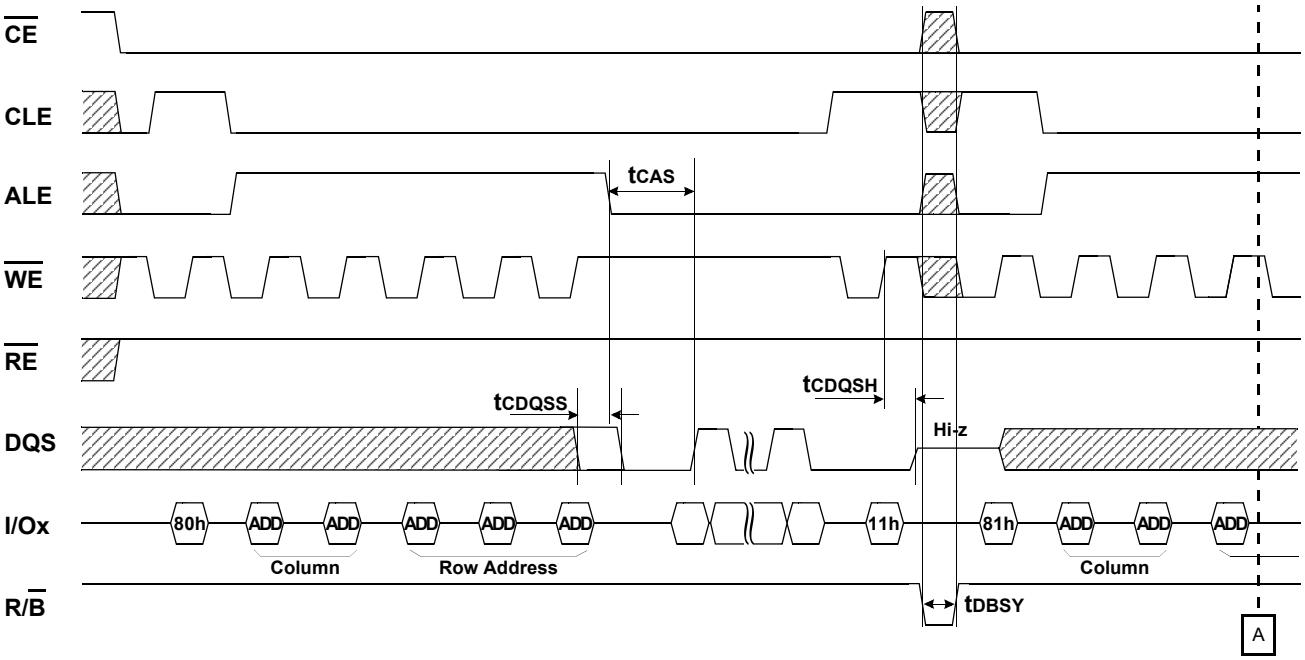
4.15 Two-Plane Page Read with Two-Plane Random Data Out (1/2)

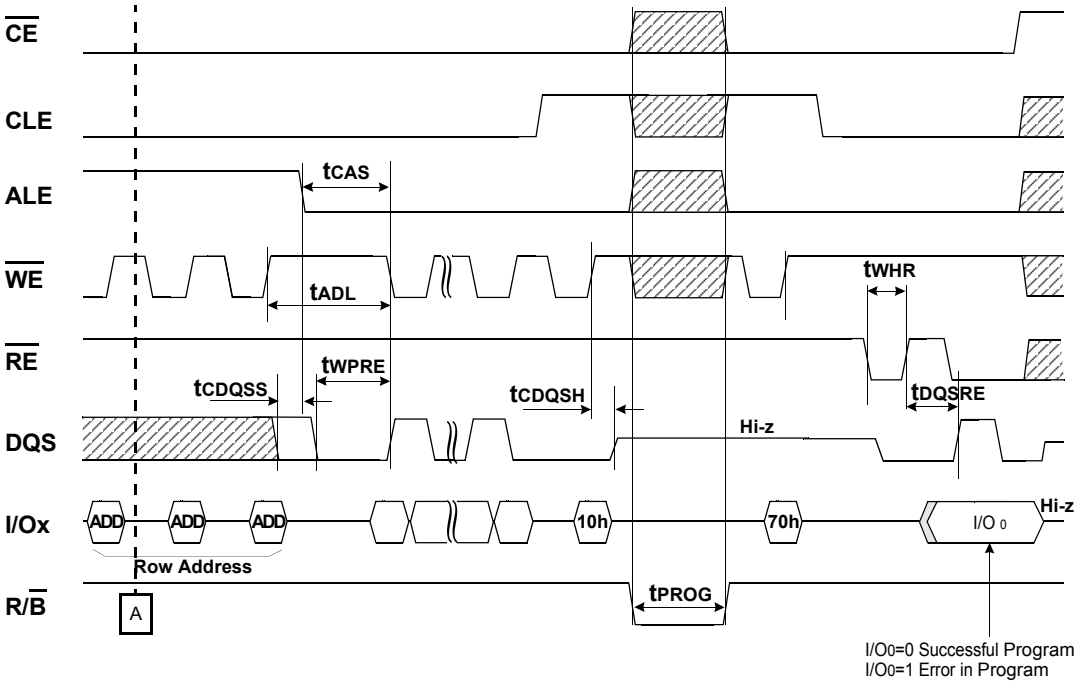


4.16 Two-Plane Page Read with Two-Plane Random Data Out (2/2)

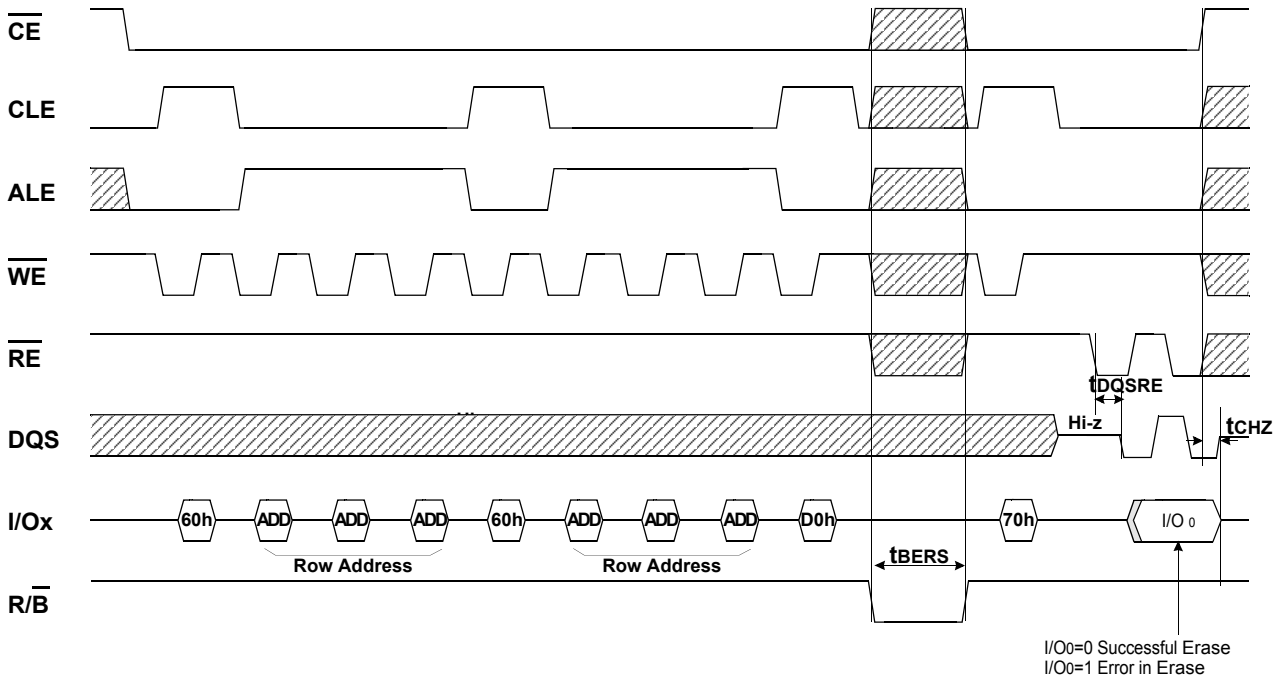


4.17 Two-Plane Page Program

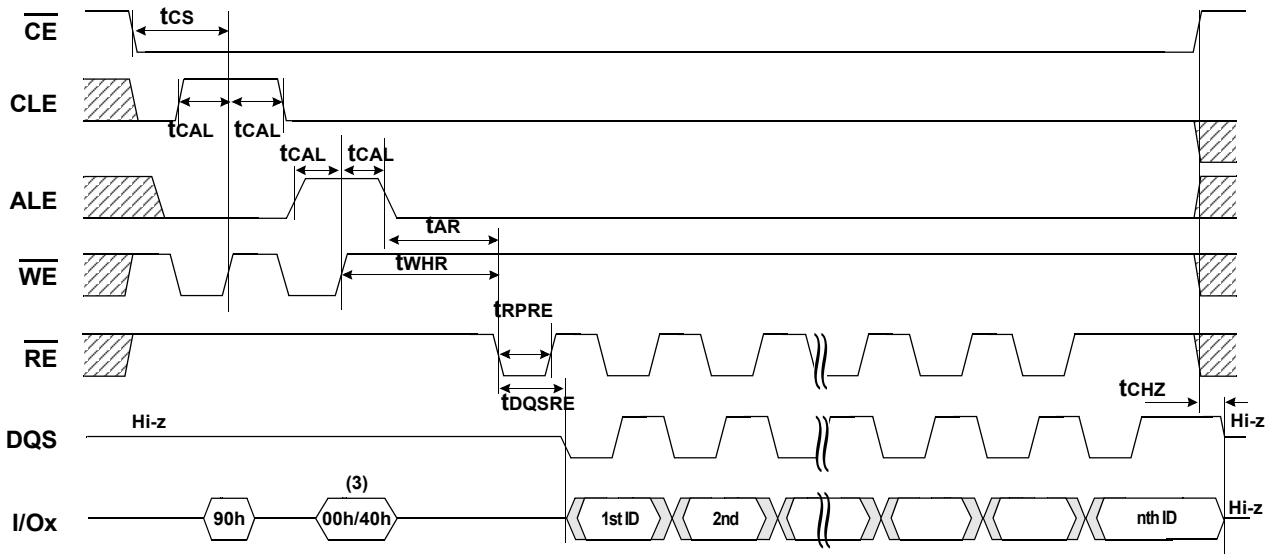




4.18 Two-Plane Block Erase Operation



4.19 Read ID Operation



NOTE :
1) Even thougn toggle-mode NAND uses both low- and high-going edges of DQS for reads, ID read operation repeates each data byte twice, so that ID read timing becomes identical to that of legacy NAND
2) DQS and DQ drivers turn from valid value to high-z when $\overline{CE}$ or CLE goes High.
3) Address 00h is for Samsung legacy and 40h is for new JEDEC ID information.

4.20 00h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBGD8X0M	ECh	D7h	14h	76h	54h	C2h
K9LCGD8X1M						
K9HDGD8X5M						
K9PFGD8X7M						
K9PFGD8X5M	ECh	DEh	55h	76h	58h	C2h

4.21 40h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBGD8X0M	4Ah	45h	44h	45h	43h	02h
K9LCGD8X1M						
K9HDGD8X5M						
K9PFGD8X7M						
K9PFGD8X5M						

00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size,Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleaving operation between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	2KB 4KB 8KB Reserved						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	128KB 256KB 512KB 1MB Reserved Reserved Reserved Reserved	0 0 0 0 1 1 1 1		0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1			
Redundant Area Size (byte / Page Size)	Reserved 128B 218B 400B 436B 512B Reserved Reserved		0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
ECC Level	1bit 2bit 4bit 8bit 16bit 24bit Reserved Reserved		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0						0	0

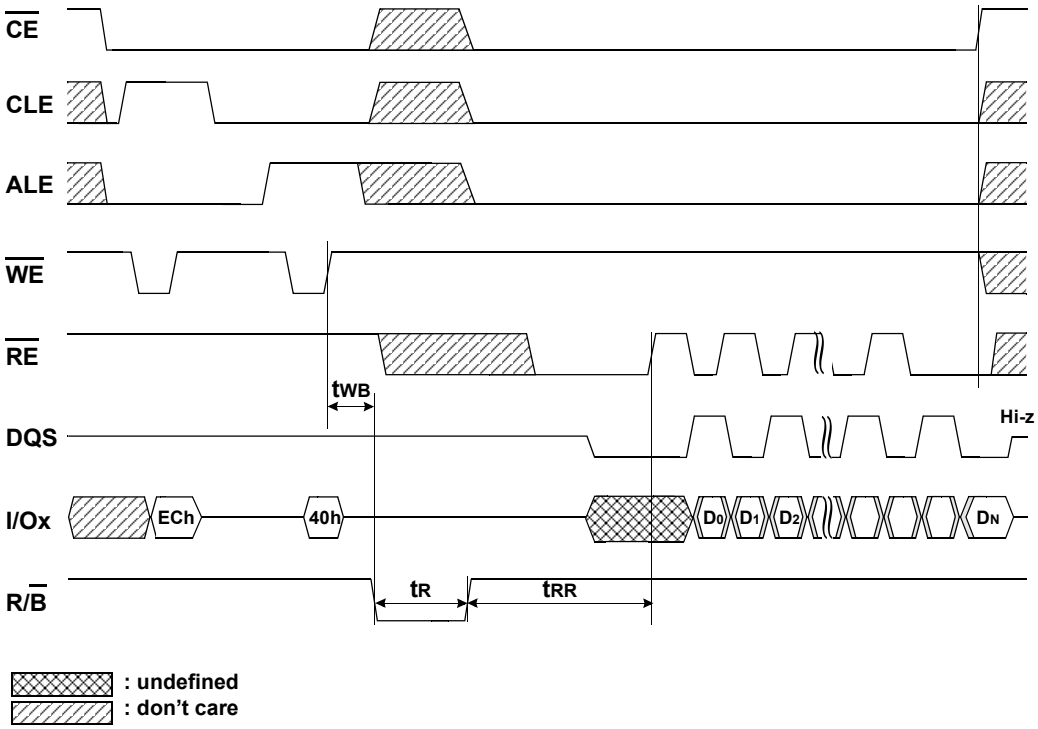
6th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Device Version	50nm 40nm 30nm Reserved Reserved Reserved Reserved Reserved						0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 0
EDO	Not Support Support		0 1						
Interface	Conventional Mode Toggle Mode	0 1							
Reserved				0	0	0			

40h Address ID Definition Table

Byte	Description	II/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
0	J	0	1	0	0	1	0	1	0
1	E	0	1	0	0	0	1	0	1
2	D	0	1	0	0	0	1	0	0
3	E	0	1	0	0	0	1	0	1
4	C	0	1	0	0	0	0	1	1
5	Legacy Asynchronous SDR Toggle Mode DDR Synchronous DDR	0	0	0	0	0 0 0	0 0 1	0 1 0	1 0 0

4.22 Device ID Table Read Operation



NOTE :
1) Device ID Table Definition is under discussion at JEDEC.
2) Device ID Table Read operation timing is identical to that of normal read operation.

5.0 Device Operation

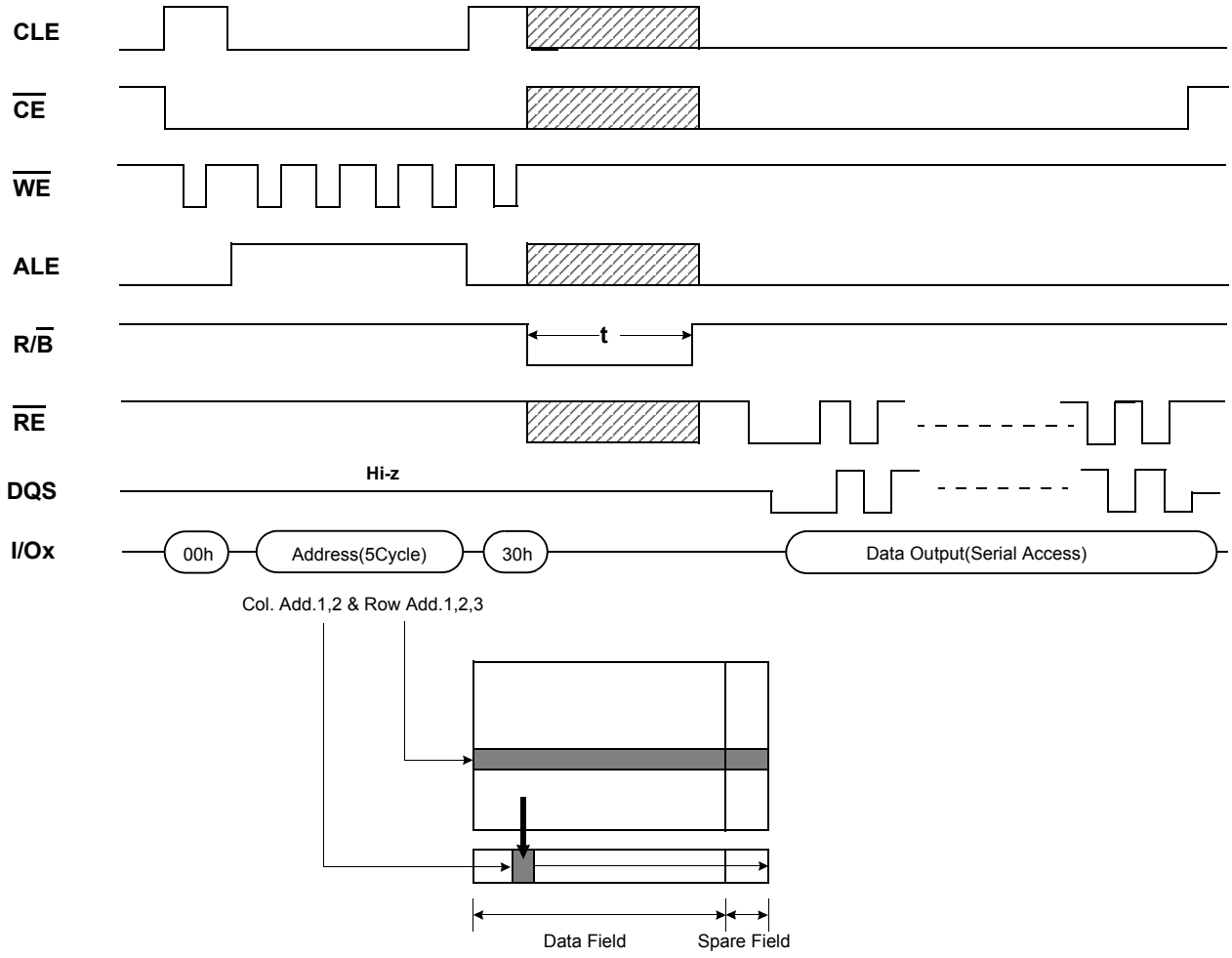
5.1 Toggle Mode Interface

The K9GBGD8X0M uses the toggle mode interface to achieve a high data transfer rate, in which data in the register can be read out at rising and falling edges of DQS, and also the controller can load data into the device at rising and falling edges of DQS. Thus, an even number of bytes is always transferred. The least significant bit of the column address shall always be zero in the toggle mode interface. If the least significant bit of the column address is set to one , then the results are corrupted.
The device uses the toggle mode to achieve the high data transfer rate in which mode a strobe signal for the DQS data bus is used for data in/out transfers. DQS is bi-directional and not used for command, address cycles but for all data transfer. The latching edge of DQS is aligned to the transition of the DQ bus for data transfers between the device and the controller(Read/Program).

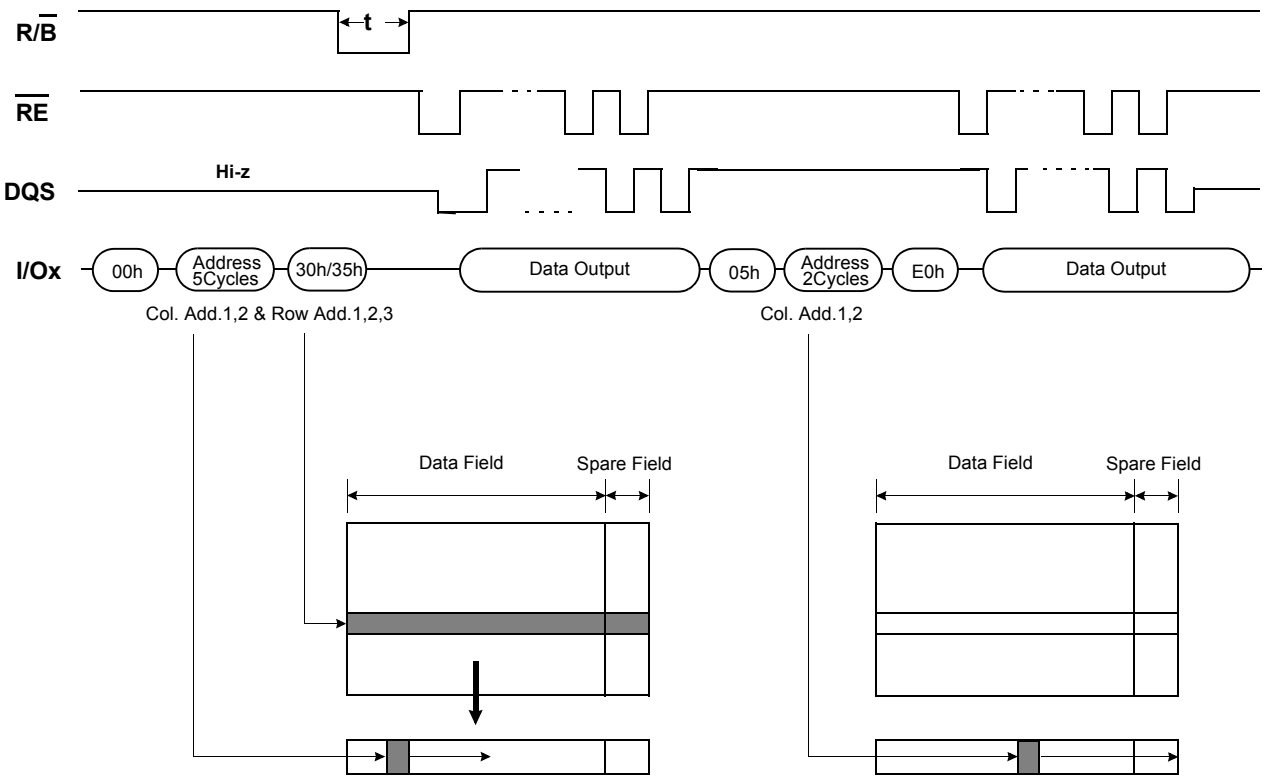
5.2 PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. The 8,704 bytes of data within the selected page are transferred to the data registers in less than 400μs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 15ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive toggle of the $\overline{RE}$ makes the device output the data starting from the selected column address up to the last column address. And $\overline{RE}$ generates DQS strobe signal which is synchronized with $\overline{RE}$. The controller can define the time to fetch the data from the device referring to the both edge of DQS strobe signal. The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Read Operation



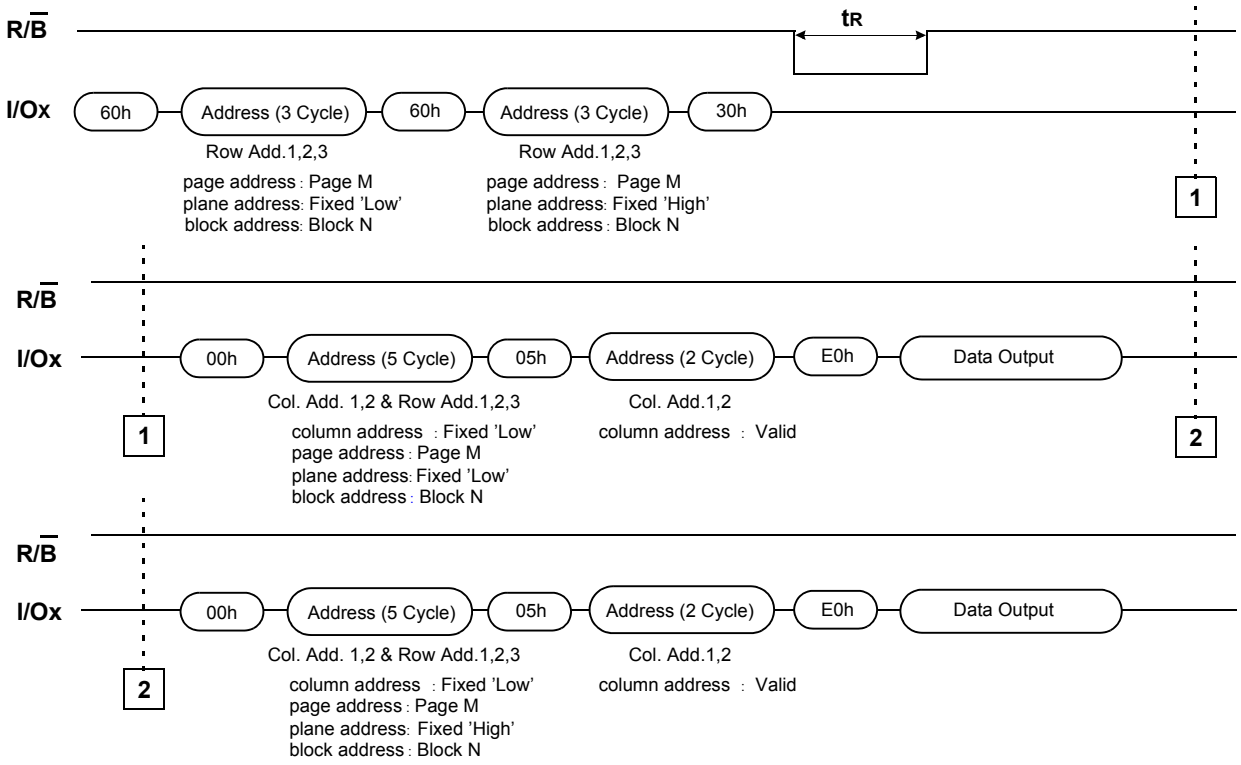
Random Data Output In a Page



5.3 TWO-PLANE PAGE READ

Two-Plane Page Read is an extension of Page Read, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a random read of two pages. Two-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. In this case, only same page of same block can be selected from each plane. After Read Confirm command(30h) the 17,408 bytes of data within the selected two page are transferred to the data registers in less than tR. The system controller can detect the completion of data transfer(tR) by monitoring the output of R/B pin.
Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences.
Two-Plane Read must be used in the block which has been programmed with Two-Plane Page Program.

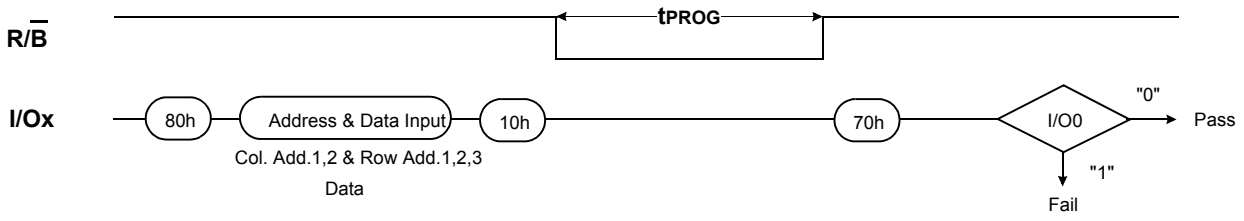
Two-Plane Page Read Operation with Two-Plane Random Data Out



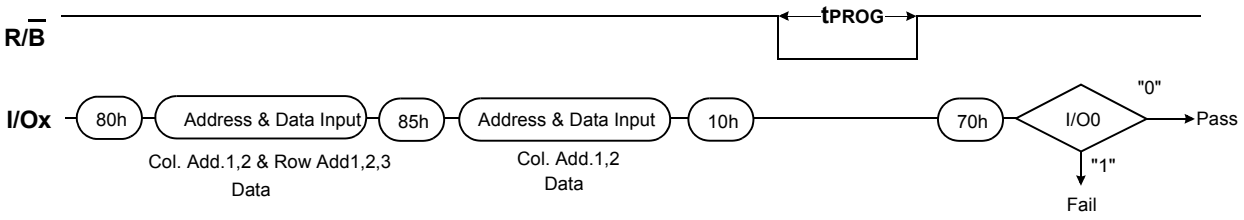
5.4 PAGE PROGRAM

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 time for the page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 8,704bytes of data may be loaded into the data registers, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five address cycle inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Program & Read Status Operation



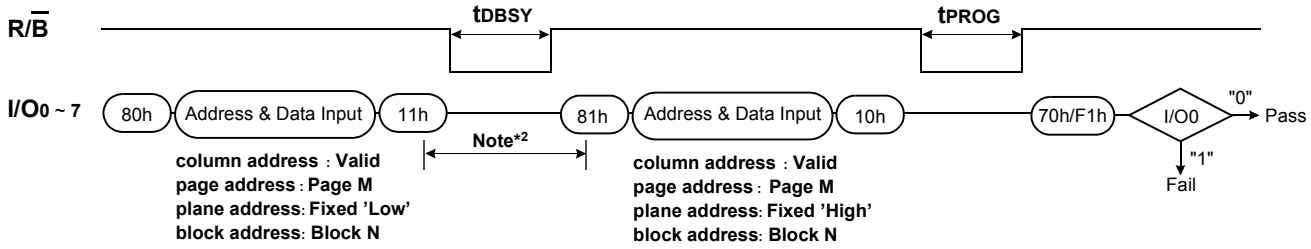
Random Data Input In a Page



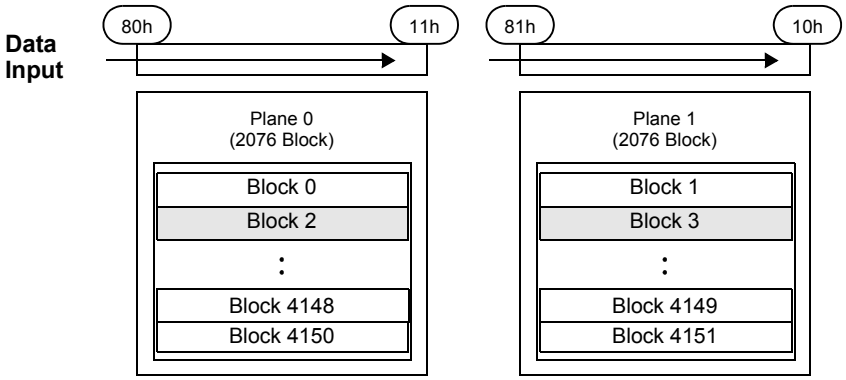
5.5 TWO-PLANE PAGE PROGRAM

Two-Plane Page Program is an extension of Page Program, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a simultaneous programming of two pages.
After writing the first set of data up to 8,704 byte into the selected data registers, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program.
Restriction in addressing with Two-Plane Page Program is shown below.

Two-Plane Page Program



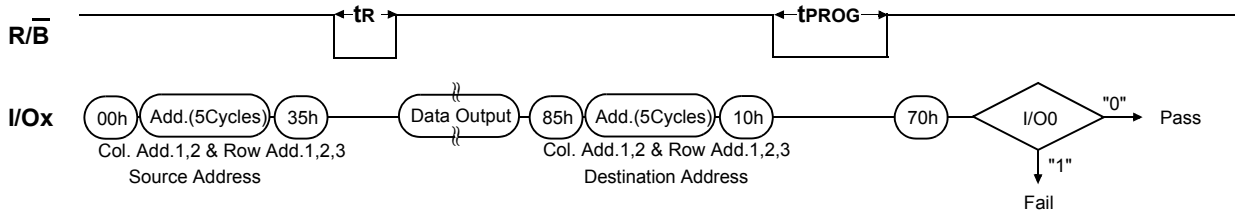
NOTE :
1) Any command between 11h and 81h is prohibited except 70h/F1h and FFh.



5.6 COPY-BACK PROGRAM

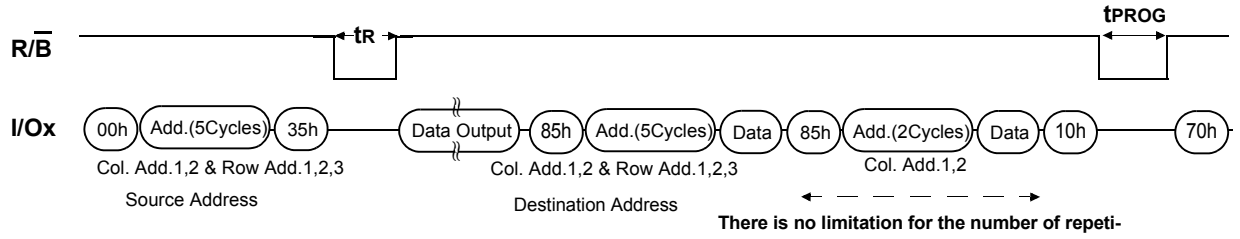
Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance can be improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 8,704-byte data into the internal data buffer. Bit errors are checked by sequential reading the data. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown below.

Page Copy-Back Program Operation



NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.

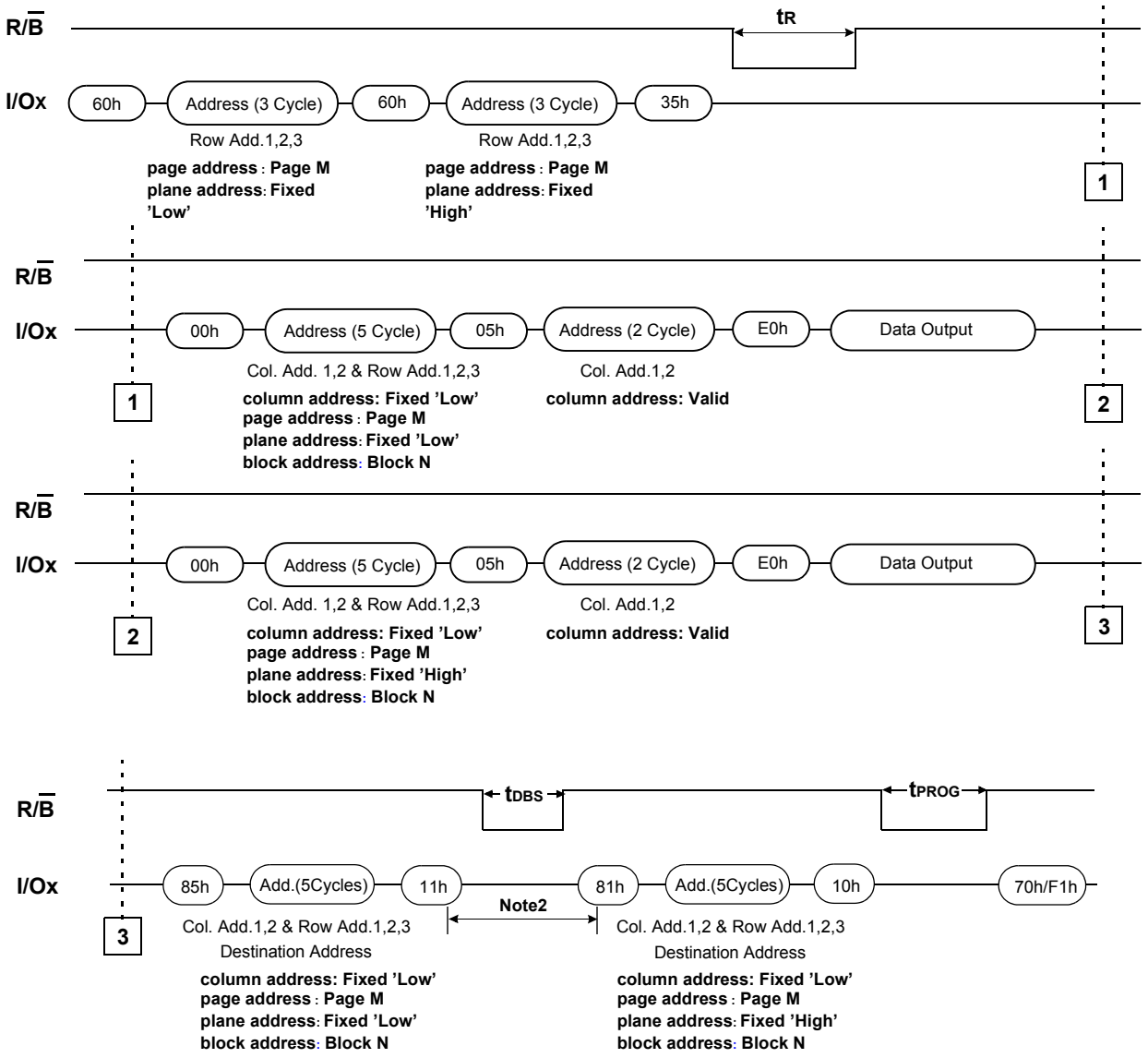
Page Copy-Back Program Operation with Random Data Input

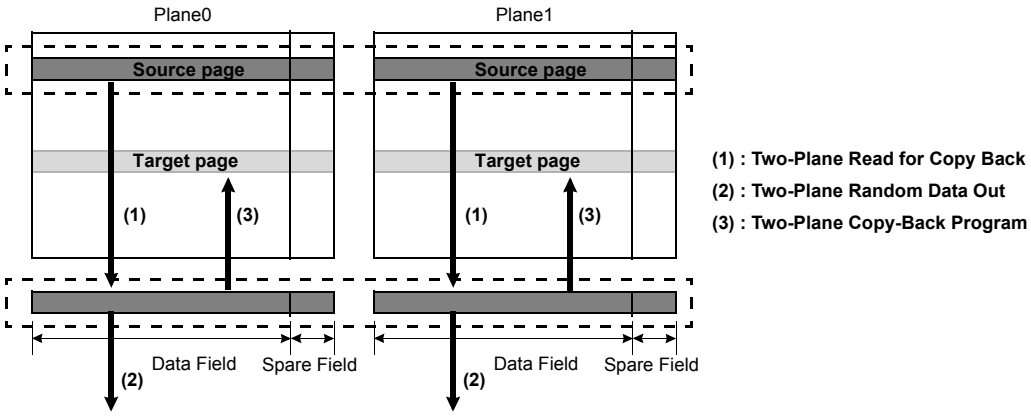


5.7 TWO-PLANE COPY-BACK PROGRAM

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a simultaneous programming of two pages.

Two-Plane Copy-Back Program Operation

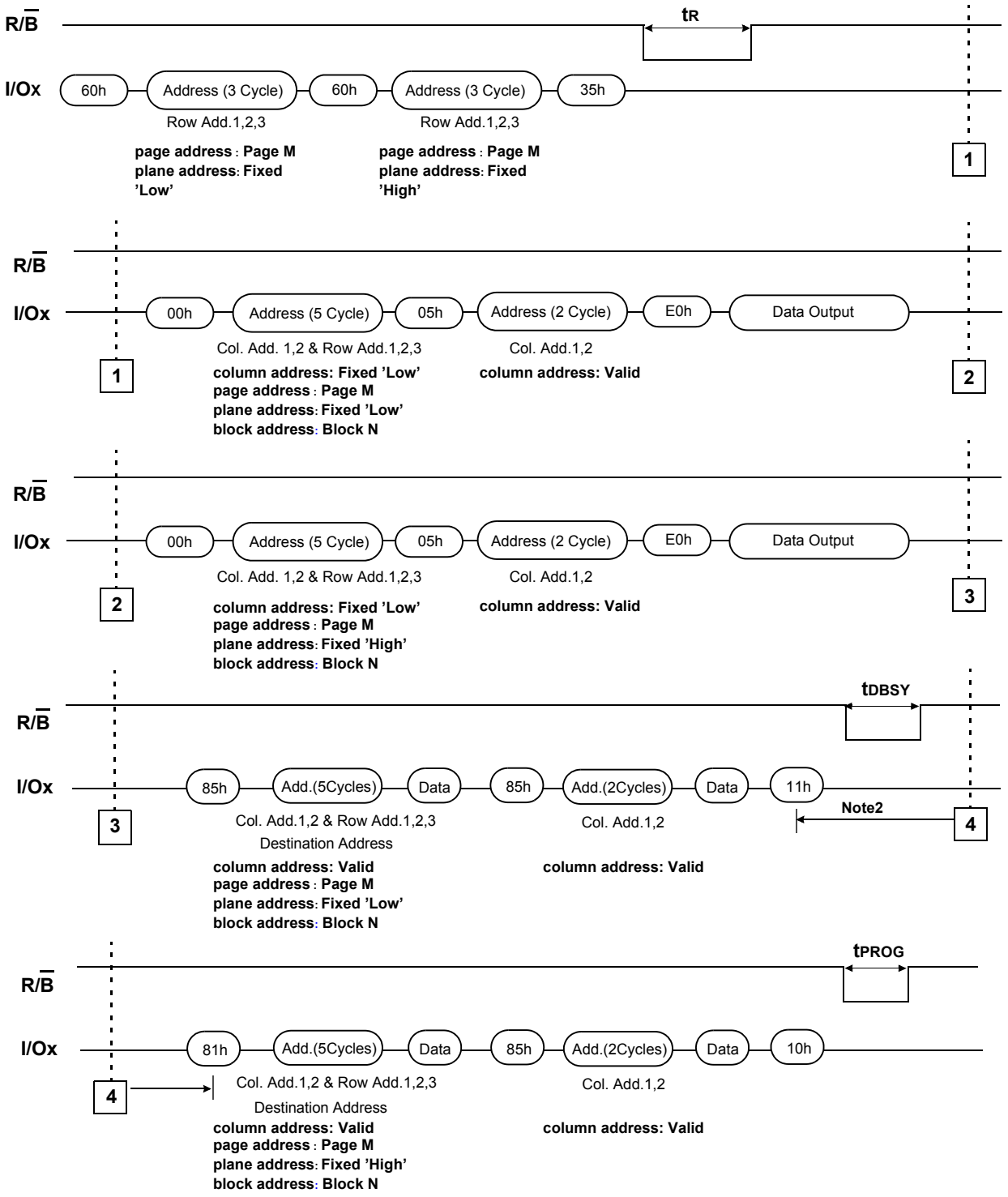




(1) : Two-Plane Read for Copy Back
(2) : Two-Plane Random Data Out
(3) : Two-Plane Copy-Back Program

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

Two-Plane Copy-Back Program Operation with Random Data Input

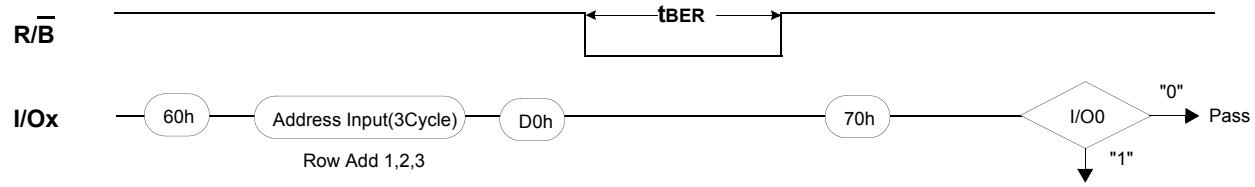


NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

5.8 BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erase process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Refer to the details below.

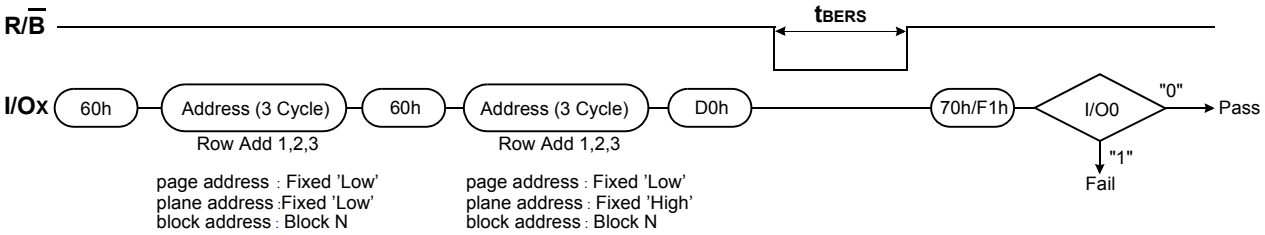
Block Erase Operation



5.9 TWO-PLANE BLOCK ERASE

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/$\overline{B}$ pin or Ready/Busy status bit (I/O 6).

Two-Plane Block Erase Operation



5.10 READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{RE}$, whichever occurs last. This line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ does not need to be toggled for updated status. Refer to Table 2 for specific 70h Status Register definitions and Table 3 for specific F1h status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table 2. Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not Use	Pass : "0" Fail : "1"
I/O 1	Not Use	Not Use	Not Use	Don't -cared
I/O 2	Not Use	Not Use	Not Use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1" "1"otected

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

Table 3. F1h Read Status Register Definition

I/O No.	Page Program	Block Erase	Read	Definition
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

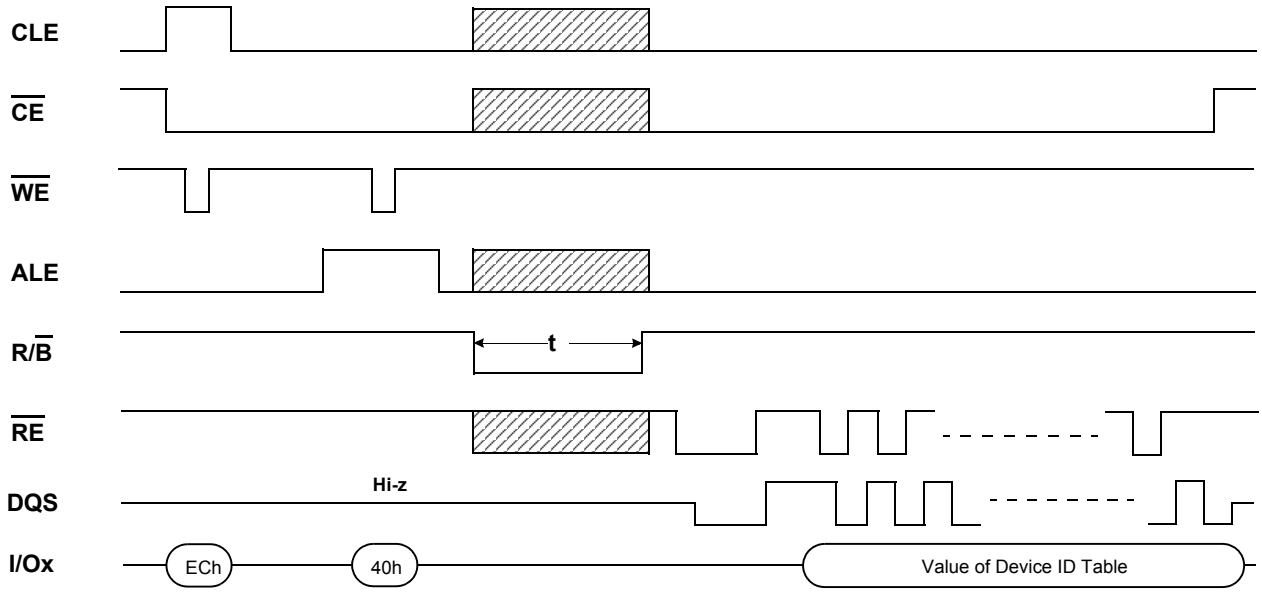
NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

5.11 DEVICE IDENTIFICATION TABLE READ OPERATION

The device supports the device ID table read operation to give more ID information such as the device's organization, features, timings and other parameters. Refer to the Device ID Table Read timing diagram below.

Values in the Device ID Table are static and shall not change.

Device ID Table Read



Device ID table definitions

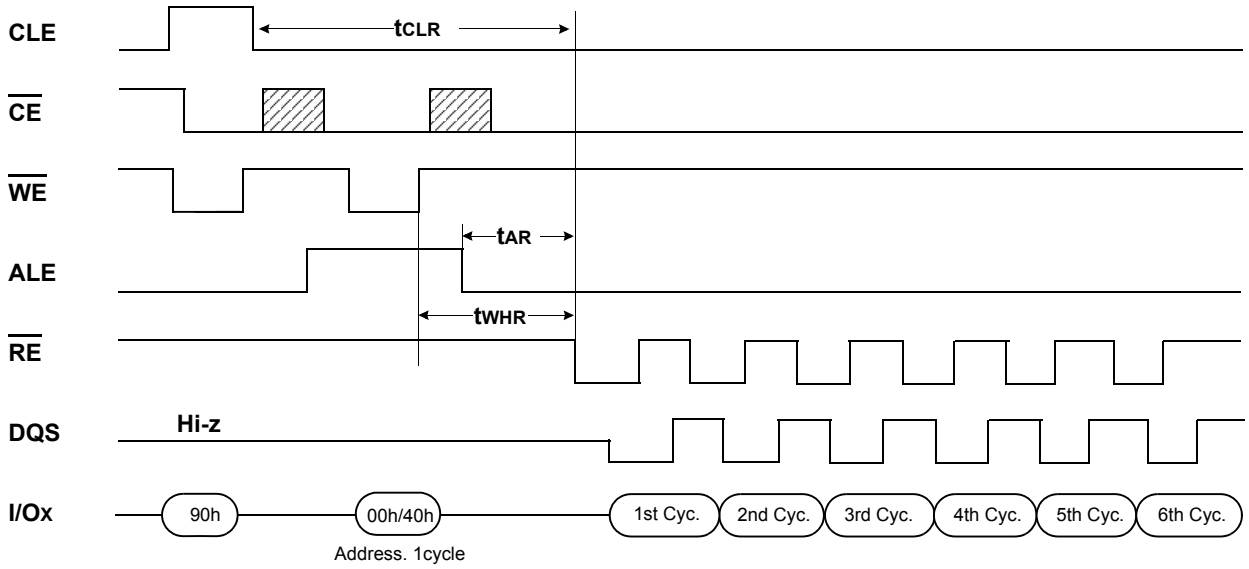
Byte	O/M	Description	Value
	Revision information and features block		
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)	4Ah, 45h, 53h, 44h
4-5	M	Revision number 2-15: Reserved (0) 1: 1 = supports revision 1.0 0: Reserved (0)	02h, 00h
6-7	M	Features supported 0-15 Reserved (0) <To be defined based on feature discussions.>	TBD
8-10	M	Optional commands supported 0-23: Reserved (0) <To be defined based on command set discussions.>	TBD
11-3111-31		Reserved (0)	All 00h
	Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)	53h, 41h, 4Dh, 53h 55h, 4Eh, 47h, 20h 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	4Bh, 39h, 36h, 41h, 47h 44h, 38h, 55h, 30h, 4Dh 20h, 20h, 20h, 20h, 20h 20h, 20h, 20h, 20h, 20h
64-69	M	JEDEC manufacturer ID (6 bytes)	ECh
70-71	TBD	TBD	TBD
72-79		Reserved (0)	
	Memory organization block		
80-83	M	Number of data bytes per page	04h, 20h, 00h, 00h
84-85	M	Number of spare bytes per page	00h, 02h
86-89	M	TBD	TBD
90-91	M	TBD	TBD
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit	38h, 10h, 00h, 00h
100	M	Number of logical unit	01h
101-255	TBD	TBD	TBD
	Redundant parameter pages		
255-511	M	Redundant parameter pages	Value of byte 0-255
512-767	M	Redundant parameter pages	Value of byte 0-255
From768	O	Additional redundant parameter pages.	TBD

NOTE :
Values in the Device ID Table are TBD

5.12 READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code(ECh), the device code, 3rd, 4th, 5th and 6th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

Read ID Operation



NOTE :
Address 00h is for Samsung legacy and 40h is for new JEDEC ID information.

5.12.1 00h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBGD8X0M	ECh	D7h	14h	76h	54h	C2h
K9LCGD8X1M						
K9HDGD8X5M						
K9PFGD8X7M						
K9PFGD8X5M	ECh	DEh	55h	76h	58h	C2h

5.12.2 40h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBGD8X0M	4Ah	45h	44h	45h	43h	02h
K9LCGD8X1M						
K9HDGD8X5M						
K9PFGD8X7M						
K9PFGD8X5M						

5.13 RESET

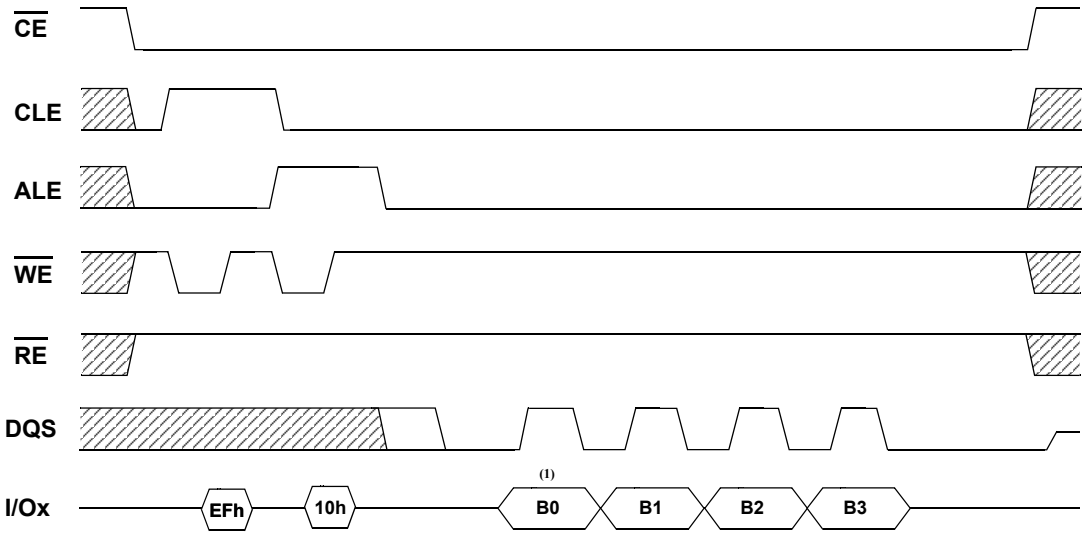
The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to Table 4 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written.

RESET Operation

5.14 OUTPUT DRIVER SETTING

The device supports four kinds of output driver setting for matching the system chracteristics. The nominal output drive strength is the power-on default value. The host is able to select a different drive strength setting using the SET FEATURES (EFh) command with following 10h address (drvier setting feature address). The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal value. The users can tune the output driver impedance of the data by setting the driver strength register value. (See Configuration Register Table) Table 5 shows which output driver would be tuned and the strength according to setting data. Upon power-up, the register will revert to the default setting. Table 6 & Table 7 shows the output driver strength impeddance values of each strength and pull-up and pull down output impedance mismatch.

Driver Strength Register Setting



NOTE :
1) B0-B3 are parameters identifying new settings for the feature specified.

Table 5. Output Driver setting Table

B0 Value	Driver Strength
00h~01h	Reserved
02h	Driver Multiplier : underdriver1
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	Driver Multiplier :overdriver1
07h	Reserved
08h	Reserved
09h	Reserved
0Ah ~0Fh	Reserved

Table 6. Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to VssQ	Minimum		Nominal		Maximum		Units
			VccQ(3.3V)	VccQ(1.8)	VccQ(3.3V)	VccQ(1.8)	VccQ(3.3V)	VccQ(1.8)	
Overdrive	Rpd	VccQ × 0.2	27.5	40.0	33.5	55.5	47.0	72.0	ohms
		VccQ × 0.5	31.0	58.0	39.0	82.5	60.5	108.5	ohms
		VccQ × 0.8	42.0	78.5	56.5	112.0	91.5	150.5	ohms
	Rpu	VccQ × 0.2	42.0	78.5	38.5	112.0	91.5	150.5	ohms
		VccQ × 0.5	31.0	58.0	44.5	82.5	60.5	108.5	ohms
		VccQ × 0.8	27.5	40.0	64.5	55.5	47.0	72.0	ohms
Nominal	Rpd	VccQ × 0.2	31.5	46.0	64.5	64.5	53.5	81.5	ohms
		VccQ × 0.5	35.0	67.0	44.5	95.5	69.5	125.0	ohms
		VccQ × 0.8	48.0	91.0	38.5	129.5	104.5	173.0	ohms
	Rpu	VccQ × 0.2	48.0	91.0	38.5	129.5	104.5	173.0	ohms
		VccQ × 0.5	35.0	67.0	44.5	95.5	69.5	125.0	ohms
		VccQ × 0.8	31.5	46.0	64.5	64.5	53.5	81.5	ohms
Underdrive	Rpd	VccQ × 0.2	34.5	58.0	42.0	80.0	58.5	103.0	ohms
		VccQ × 0.5	38.5	84.0	48.5	120.5	76.0	156.5	ohms
		VccQ × 0.8	52.5	113.5	70.5	163.5	114.0	219.5	ohms
	Rpu	VccQ × 0.2	52.5	113.5	70.5	163.5	114.0	219.5	ohms
		VccQ × 0.5	38.5	84.0	48.5	120.5	76.0	156.5	ohms
		VccQ × 0.8	34.5	58.0	42.0	80.0	58.5	103.0	ohms

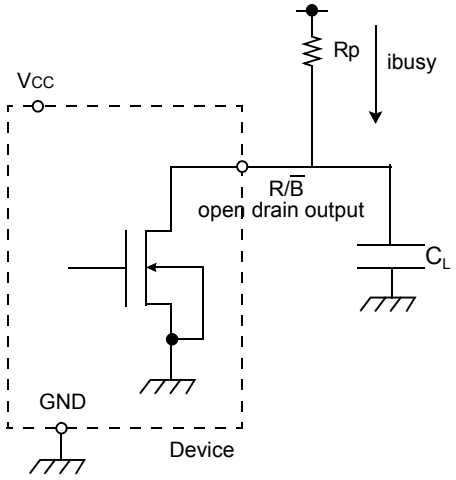
Table 7. Pull-up and Pull-down Output Impedance Mismatch

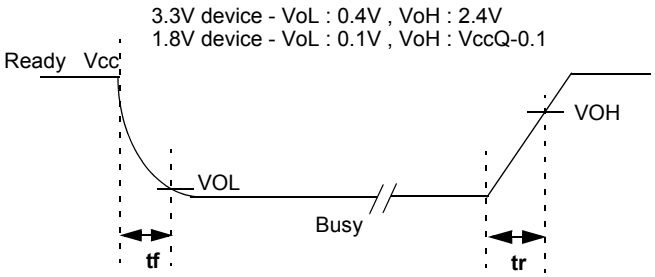
Drive Strength	Min		Max		Unit	Notes
	VccQ(3.3V)	VccQ(1.8)	VccQ(3.3V)	VccQ(1.8)		
Overdrive 1	0	0	6.7	32.0	ohms	1, 2
Nominal	0	0	8.3	40.0	ohms	1, 2
Underdrive	0	0	11.1	53.5	ohms	1, 2

NOTE :
1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2) Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5, $T_A = T_{OPER}$

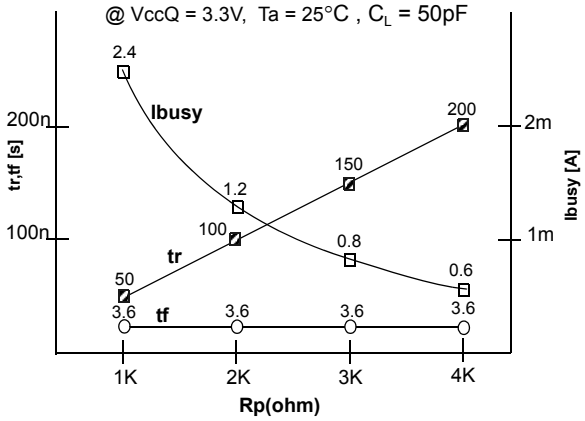
5.15 READY/$\overline{\text{BUSY}}$

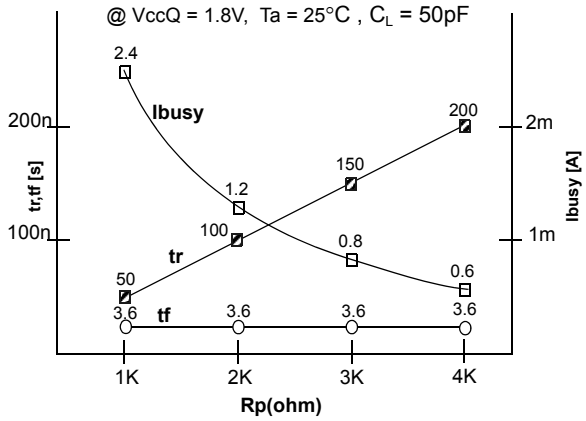
The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.





Rp vs tr ,tf & Rp vs ibusy





Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

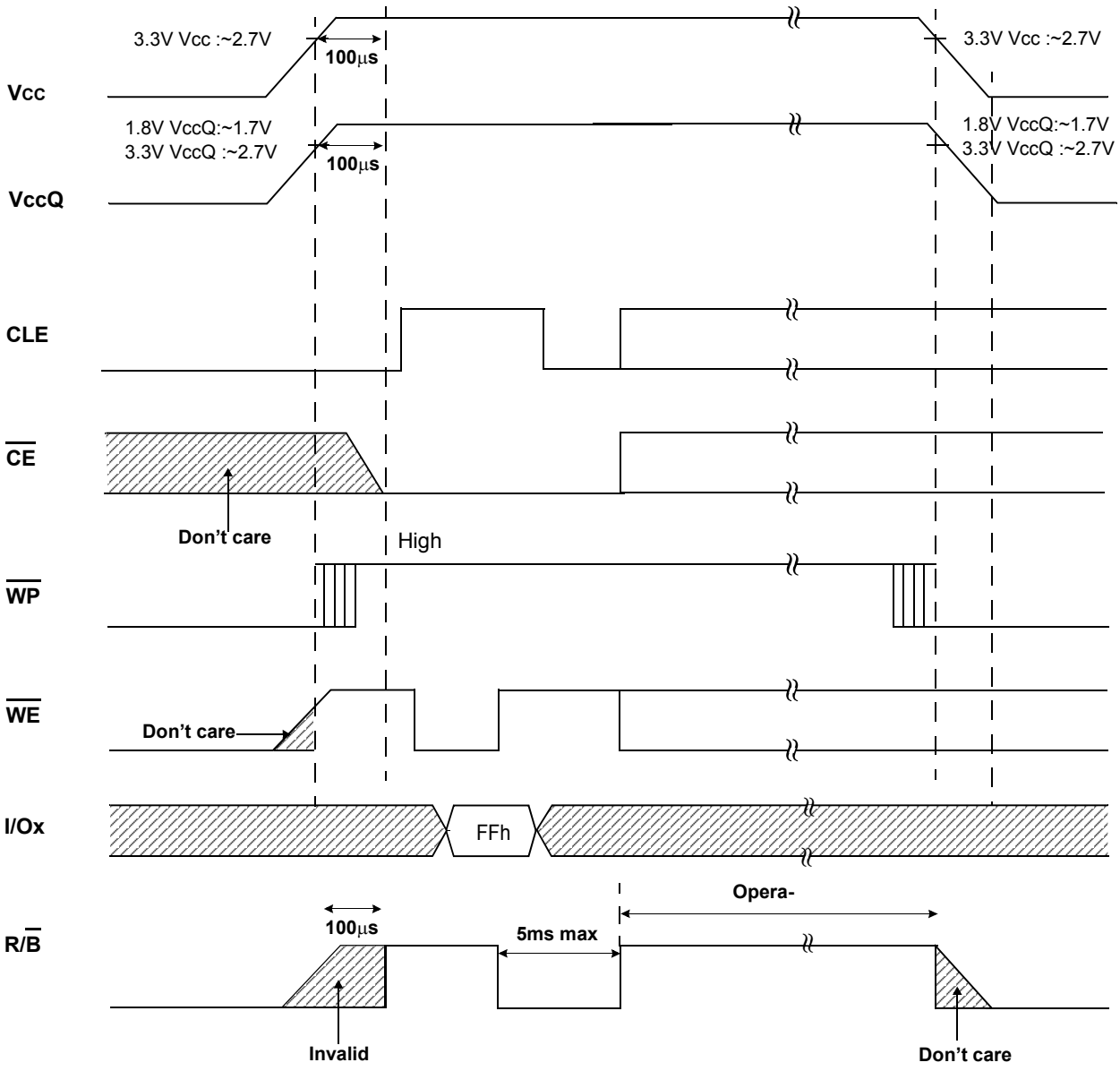
5.16 DATA PROTECTION & POWER UP SEQUENCE

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V(3.3V device). The Reset command(FFh) must be issued to all $\overline{CE}$s as the first command after the NAND Flash device is powered on. Each $\overline{CE}$ will be busy for a maximum of 5ms after a RESET command is issued. In this time period, the acceptable command is 70h/F1h.

Each NAND die will draw no more than 1st prior to execution of the first Reset command(FFh) after the device is powered on.

$\overline{WP}$ pin provices hardware protection and is recommanded to be kept at V_{IL} during power-up and power-down. The two step command sequence for program/erase provides additional software protection.

AC Waveforms for Power Transition



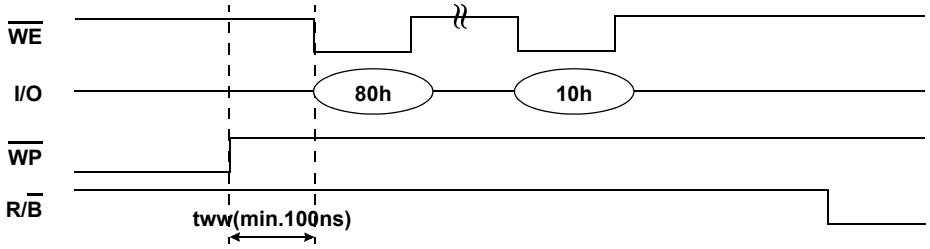
NOTE :
During the initialization, the device consumes a maximum current of 50mA (Icc1)

6.0 $\overline{WP}$ AC Timing guide

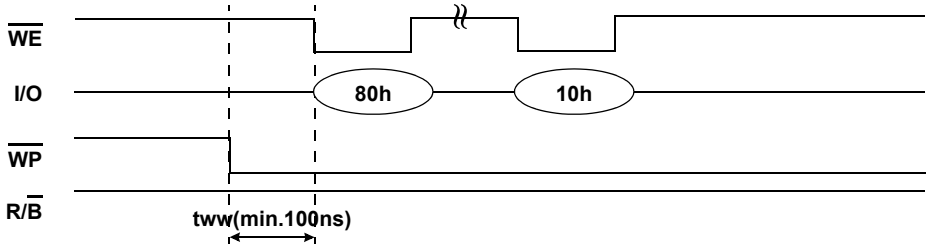
Enabling $\overline{WP}$ during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Program Operation

1. Enable Mode

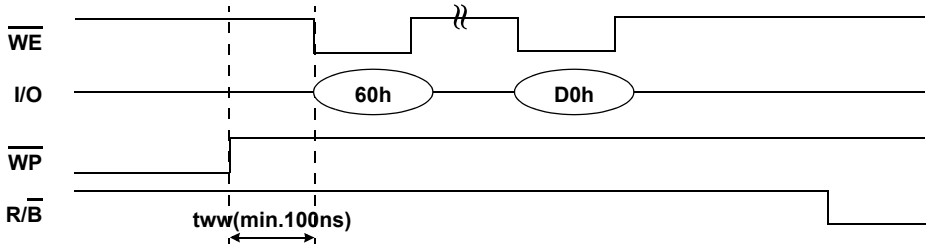


2. Disable Mode



Erase Operation

1. Enable Mode



2. Disable Mode