## Document Title

***256M Bit (16M x16) Synchronous Burst , Multi Bank NOR Flash Memory***

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Advanced | March 15, 2004 | Advance |
| 0.1 | Revision<br>- Change the speed code<br>7B : 90ns @54MHz ---> 7B : 88.5ns @54MHz | June 1, 2004 | Preliminary |
| 0.2 | Revision<br>- Change the device version ID<br>Top boot device : 22ECH --> 22FCH<br>Bottom boot device : 22EDH --> 22FDH<br>- Not support accelerated quad word program operation | July 5, 2004 | Preliminary |
| 0.3 | Revision<br>- Change the initial access time of asynchronous read mode<br>K8A56156ET(B)A-DE7C<br>tAA : 70ns--->80ns<br>tCE : 70ns--->80ns<br>- Support accelerated quad word program operation | August 3, 2004 | Preliminary |
| 0.4 | Revision<br>- Add the operation flow chart | August 23, 2004 | Preliminary |
| 0.5 | Revision<br>- Add the description of range limitation of data read out during program suspend.(Refer to "Program Suspend/Resume" paragragh) | September 6, 2004 | Preliminary |
| 0.6 | Revision<br>- Add the requirement and note of Quadruple word program operation | December 13, 2004 | Preliminary |
| 1.0 | Specification finalized | December 16, 2004 | |

## *256M Bit (16M x16) Synchronous Burst , Multi Bank NOR Flash Memory*

### FEATURES

- Single Voltage, 1.7V to 1.95V for Read and Write operations
- Organization
  - 16,772,216 x 16 bit ( Word Mode Only)
- Read While Program/Erase Operation
- Multiple Bank Architecture
  - 16 Banks (16Mb Partition)
- OTP Block : Extra 256Byte block
- Read Access Time (@ $C_L$=30pF)
  - Asynchronous Random Access Time : 90ns (54MHz) / 80ns (66MHz)
  - Synchronous Random Access Time : 88.5ns (54MHz) / 70ns (66MHz)
  - Burst Access Time : 14.5ns (54MHz) / 11ns (66MHz)
- Burst Length :
  - Continuous Linear Burst
  - Linear Burst : 8-word & 16-word with No-wrap & Wrap
- Block Architecture
  - Eight 4Kword blocks and five hundreds eleven 32Kword blocks
  - Bank 0 contains eight 4 Kword blocks and thirty-one 32Kword blocks
  - Bank 1 ~ Bank 15 contain four hundred eighty 32Kword blocks
- Reduce program time using the $V_{PP}$
- Support Single & Quad word accelerate program
- Power Consumption (Typical value, $C_L$=30pF)
  - Burst Access Current : 30mA
  - Program/Erase Current : 15mA
  - Read While Program/Erase Current : 40mA
  - Standby Mode/Auto Sleep Mode : 25uA
- Block Protection/Unprotection
  - Using the software command sequence
  - Last two boot blocks are protected by $\overline{WP}$=$V_{IL}$
  - All blocks are protected by $V_{PP}$=$V_{IL}$
- Handshaking Feature
  - Provides host system with minimum latency by monitoring RDY
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Program/Erase
- Hardware Reset ($\overline{RESET}$)
- Data Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase completion
- Endurance
  100K Program/Erase Cycles Minimum
- Data Retention : 10 years
- Extended Temperature : -25°C ~ 85°C
- Support Common Flash Memory Interface
- Low Vcc Write Inhibit
- Package : TBD

### GENERAL DESCRIPTION

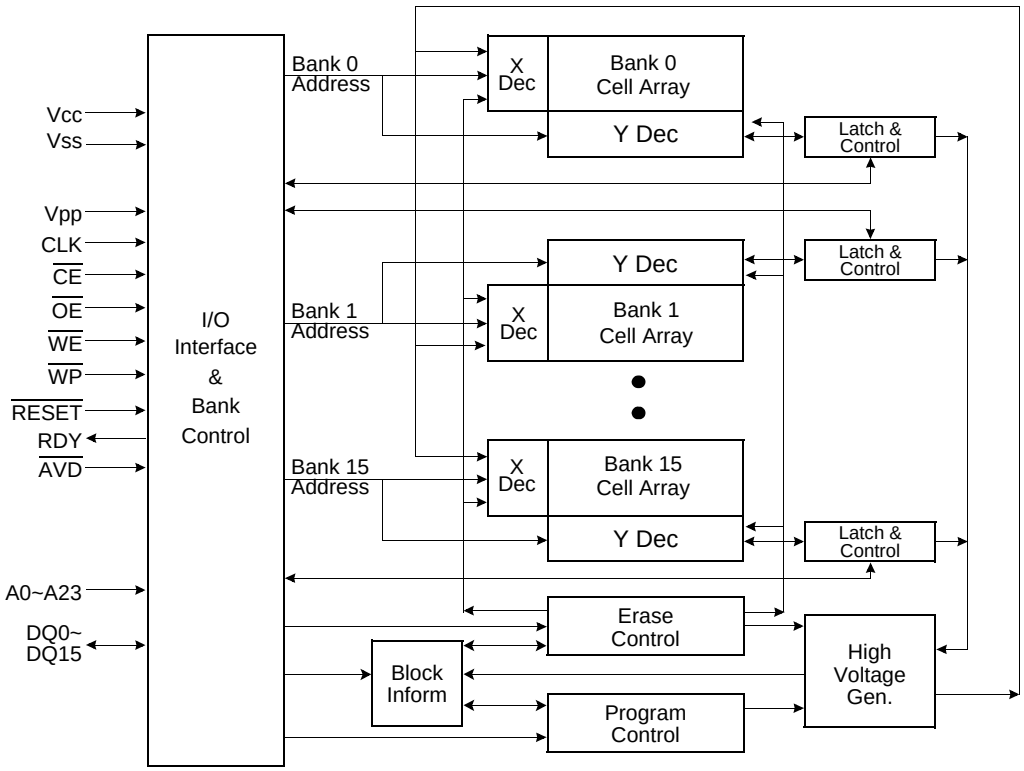
The K8A5615E featuring single 1.8V power supply is a 256Mbit Synchronous Burst Multi Bank Flash Memory organized as 16Mx16. The memory architecture of the device is designed to divide its memory arrays into 519 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The K8A5615E NOR Flash consists of sixteen banks. This device is capable of reading data from one bank while programming or erasing in the other bank. Regarding read access time, the K8A5615E provides an 14.5ns burst access time and an 88.5ns initial access time at 54MHz. At 66MHz, the K8A5615E provides an 11ns burst access time and 70ns initial access time. The device performs a program operation in units of 16 bits (Word) and an erase operation in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7 sec. The device requires 15mA as program/erase current in the extended temperature ranges.

The K8A5615E NOR Flash Memory is created by using Samsung's advanced CMOS process technology.

### PIN DESCRIPTION

| Pin Name | Pin Function |
|---|---|
| A0 - A23 | Address Inputs |
| DQ0 - DQ15 | Data input/output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{RESET}$ | Hardware Reset Pin |
| $V_{PP}$ | Accelerates Programming |
| $\overline{WE}$ | Write Enable |
| $\overline{WP}$ | Hardware Write Protection Input |
| CLK | Clock |
| RDY | Ready Output |
| $\overline{AVD}$ | Address Valid Input |
| Vcc | Power Supply |
| $V_{SS}$ | Ground |

## FUNCTIONAL BLOCK DIAGRAM



## ORDERING INFORMATION

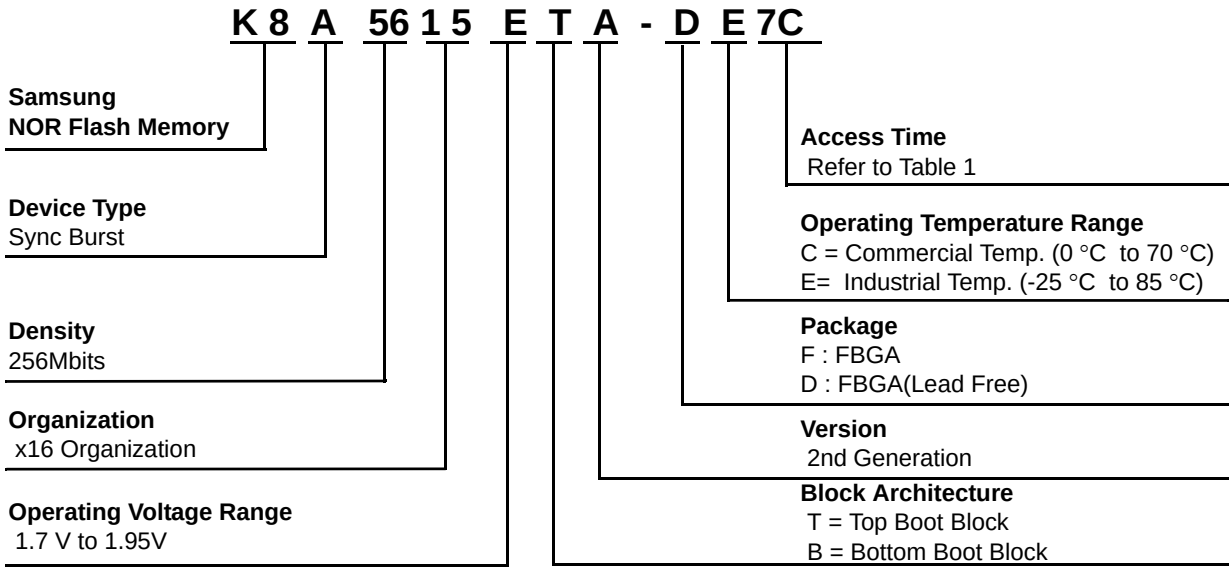



**Table 1. PRODUCT LINE-UP**

| | K8A5615E | | | | | |
|---|---|---|---|---|---|---|
| | Synchronous/Burst | | | Asynchronous | | |
| | Speed Option | 7B (54MHz) | 7C (66MHz) | Speed Option | 7B (54MHz) | 7C (66MHz) |
| $V_{CC}$=1.7V-1.95V | Max. Initial Access Time ($t_{IAA}$, ns) | 88.5 | 70 | Max Access Time ($t_{AA}$, ns) | 90 | 80 |
| | Max. Burst Access Time ($t_{BA}$, ns) | 14.5 | 11 | Max $\overline{CE}$ Access Time ($t_{CE}$, ns) | 90 | 80 |
| | Max. $\overline{OE}$ Access Time ($t_{OE}$, ns) | 20 | 20 | Max $\overline{OE}$ Access Time ($t_{OE}$, ns) | 20 | 20 |

**Table 2. K8A5615E DEVICE BANK DIVISIONS**

| Bank 0 | | Bank 1 ~ Bank 15 | |
|---|---|---|---|
| Mbit | Block Sizes | Mbit | Block Sizes |
| 16 Mbit | Eight 4Kwords, Thirty-one 32Kwords | 240 Mbit | Four hundred eighty 32Kwords |

**Table 3-1. Top Boot Block Address Table(K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 0 | BA518 | 4 Kwords | FFF000h-FFFFFFh |
| | BA517 | 4 Kwords | FFE000h-FFEFFFh |
| | BA516 | 4 Kwords | FFD000h-FFDFFFh |
| | BA515 | 4 Kwords | FFC000h-FFCFFFh |
| | BA514 | 4 Kwords | FFB000h-FFBFFFh |
| | BA513 | 4 Kwords | FFA000h-FFAFFFh |
| | BA512 | 4 Kwords | FF9000h-FF9FFFh |
| | BA511 | 4 Kwords | FF8000h-FF8FFFh |
| | BA510 | 32 Kwords | FF0000h-FF7FFFh |
| | BA509 | 32 Kwords | FE8000h-FEFFFFh |
| | BA508 | 32 Kwords | FE0000h-FE7FFFh |
| | BA507 | 32 Kwords | FD8000h-FDFFFFh |
| | BA506 | 32 Kwords | FD0000h-FD7FFFh |
| | BA505 | 32 Kwords | FC8000h-FCFFFFh |
| | BA504 | 32 Kwords | FC0000h-FC7FFFh |
| | BA503 | 32 Kwords | FB8000h-FBFFFFh |
| | BA502 | 32 Kwords | FB0000h-FB7FFFh |
| | BA501 | 32 Kwords | FA8000h-FAFFFFh |
| | BA500 | 32 Kwords | FA0000h-FA7FFFh |
| | BA499 | 32 Kwords | F98000h-F9FFFFh |
| | BA498 | 32 Kwords | F90000h-F97FFFh |
| | BA497 | 32 Kwords | F88000h-F8FFFFh |
| | BA496 | 32 Kwords | F80000h-F87FFFh |
| | BA495 | 32 Kwords | F78000h-F7FFFFh |
| | BA494 | 32 Kwords | F70000h-F77FFFh |
| | BA493 | 32 Kwords | F68000h-F6FFFFh |
| | BA492 | 32 Kwords | F60000h-F67FFFh |
| | BA491 | 32 Kwords | F58000h-F5FFFFh |
| | BA490 | 32 Kwords | F50000h-F57FFFh |
| | BA489 | 32 Kwords | F48000h-F4FFFFh |
| | BA488 | 32 Kwords | F40000h-F47FFFh |
| | BA487 | 32 Kwords | F38000h-F3FFFFh |
| | BA486 | 32 Kwords | F30000h-F37FFFh |
| | BA485 | 32 Kwords | F28000h-F2FFFFh |
| | BA484 | 32 Kwords | F20000h-F27FFFh |
| | BA483 | 32 Kwords | F18000h-F1FFFFh |
| | BA482 | 32 Kwords | F10000h-F17FFFh |
| | BA481 | 32 Kwords | F08000h-F0FFFFh |
| | BA480 | 32 kwords | F00000h-F07FFFh |
| Bank 1 | BA479 | 32 Kwords | EF8000h-EFFFFFh |
| | BA478 | 32 Kwords | EF0000h-EF7FFFh |
| | BA477 | 32 Kwords | EE8000h-EEFFFFh |
| | BA476 | 32 Kwords | EE0000h-EE7FFFh |
| | BA475 | 32 Kwords | ED8000h-EDFFFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 1 | BA474 | 32 Kwords | ED0000h-ED7FFFh |
| | BA473 | 32 Kwords | EC8000h-ECFFFFh |
| | BA472 | 32 Kwords | EC0000h-EC7FFFh |
| | BA471 | 32 Kwords | EB8000h-EBFFFFh |
| | BA470 | 32 Kwords | EB0000h-EB7FFFh |
| | BA469 | 32 Kwords | EA8000h-EAFFFFh |
| | BA468 | 32 Kwords | EA0000h-EA7FFFh |
| | BA467 | 32 Kwords | E98000h-E9FFFFh |
| | BA466 | 32 Kwords | E90000h-E97FFFh |
| | BA465 | 32 Kwords | E88000h-E8FFFFh |
| | BA464 | 32 Kwords | E80000h-E87FFFh |
| | BA463 | 32 Kwords | E78000h-E7FFFFh |
| | BA462 | 32 Kwords | E70000h-E77FFFh |
| | BA461 | 32 Kwords | E68000h-E6FFFFh |
| | BA460 | 32 Kwords | E60000h-E67FFFh |
| | BA459 | 32 Kwords | E58000h-E5FFFFh |
| | BA458 | 32 Kwords | E50000h-E57FFFh |
| | BA457 | 32 Kwords | E48000h-E4FFFFh |
| | BA456 | 32 Kwords | E40000h-E47FFFh |
| | BA455 | 32 Kwords | E38000h-E3FFFFh |
| | BA454 | 32 Kwords | E30000h-E37FFFh |
| | BA453 | 32 Kwords | E28000h-E2FFFFh |
| | BA452 | 32 Kwords | E20000h-E27FFFh |
| | BA451 | 32 Kwords | E18000h-E1FFFFh |
| | BA450 | 32 Kwords | E10000h-E17FFFh |
| | BA449 | 32 Kwords | E08000h-E0FFFFh |
| | BA448 | 32 Kwords | E00000h-E07FFFh |
| Bank 2 | BA447 | 32 Kwords | DF8000h-DFFFFFh |
| | BA446 | 32 Kwords | DF0000h-DF7FFFh |
| | BA445 | 32 Kwords | DE8000h-DEFFFFh |
| | BA444 | 32 Kwords | DE0000h-DE7FFFh |
| | BA443 | 32 Kwords | DD8000h-DDFFFFh |
| | BA442 | 32 Kwords | DD0000h-DD7FFFh |
| | BA441 | 32 Kwords | DC8000h-DCFFFFh |
| | BA440 | 32 Kwords | DC0000h-DC7FFFh |
| | BA439 | 32 Kwords | DB8000h-DBFFFFh |
| | BA438 | 32 Kwords | DB0000h-DB7FFFh |
| | BA437 | 32 Kwords | DA8000h-DAFFFFh |
| | BA436 | 32 Kwords | DA0000h-DA7FFFh |
| | BA435 | 32 Kwords | D98000h-D9FFFFh |
| | BA434 | 32 Kwords | D90000h-D97FFFh |
| | BA433 | 32 Kwords | D88000h-D8FFFFh |
| | BA432 | 32 Kwords | D80000h-D87FFFh |
| | BA431 | 32 Kwords | D78000h-D7FFFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 2 | BA430 | 32 Kwords | D70000h-D77FFFh |
| | BA429 | 32 Kwords | D68000h-D6FFFFh |
| | BA428 | 32 Kwords | D60000h-D67FFFh |
| | BA427 | 32 Kwords | D58000h-D5FFFFh |
| | BA426 | 32 Kwords | D50000h-D57FFFh |
| | BA425 | 32 Kwords | D48000h-D4FFFFh |
| | BA424 | 32 Kwords | D40000h-D47FFFh |
| | BA423 | 32 Kwords | D38000h-D3FFFFh |
| | BA422 | 32 Kwords | D30000h-D37FFFh |
| | BA421 | 32 Kwords | D28000h-D2FFFFh |
| | BA420 | 32 Kwords | D20000h-D27FFFh |
| | BA419 | 32 Kwords | D18000h-D1FFFFh |
| | BA418 | 32 Kwords | D10000h-D17FFFh |
| | BA417 | 32 Kwords | D08000h-D0FFFFh |
| | BA416 | 32 Kwords | D00000h-D07FFFh |
| Bank 3 | BA415 | 32 Kwords | CF8000h-CFFFFFh |
| | BA414 | 32 Kwords | CF0000h-CF7FFFh |
| | BA413 | 32 Kwords | CE8000h-CEFFFFh |
| | BA412 | 32 Kwords | CE0000h-CE7FFFh |
| | BA411 | 32 Kwords | CD8000h-CDFFFFh |
| | BA410 | 32 Kwords | CD0000h-CD7FFFh |
| | BA409 | 32 Kwords | CC8000h-CCFFFFh |
| | BA408 | 32 Kwords | CC0000h-CC7FFFh |
| | BA407 | 32 Kwords | CB8000h-CBFFFFh |
| | BA406 | 32 Kwords | CB0000h-CB7FFFh |
| | BA405 | 32 Kwords | CA8000h-CAFFFFh |
| | BA404 | 32 Kwords | CA0000h-CA7FFFh |
| | BA403 | 32 Kwords | C98000h-C9FFFFh |
| | BA402 | 32 Kwords | C90000h-C97FFFh |
| | BA401 | 32 Kwords | C88000h-C8FFFFh |
| | BA400 | 32 Kwords | C80000h-C87FFFh |
| | BA399 | 32 Kwords | C78000h-C7FFFFh |
| | BA398 | 32 Kwords | C70000h-C77FFFh |
| | BA397 | 32 Kwords | C68000h-C6FFFFh |
| | BA396 | 32 Kwords | C60000h-C67FFFh |
| | BA395 | 32 Kwords | C58000h-C5FFFFh |
| | BA394 | 32 Kwords | C50000h-C57FFFh |
| | BA393 | 32 Kwords | C48000h-C4FFFFh |
| | BA392 | 32 Kwords | C40000h-C47FFFh |
| | BA391 | 32 Kwords | C38000h-C3FFFFh |
| | BA390 | 32 Kwords | C30000h-C37FFFh |
| | BA389 | 32 Kwords | C28000h-C2FFFFh |
| | BA388 | 32 Kwords | C20000h-C27FFFh |
| | BA387 | 32 Kwords | C18000h-C1FFFFh |
| | BA386 | 32 Kwords | C10000h-C17FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 3 | BA385 | 32 Kwords | C08000h-C0FFFFh |
| | BA384 | 32 Kwords | C00000h-C07FFFh |
| Bank 4 | BA383 | 32 Kwords | BF8000h-BFFFFFh |
| | BA382 | 32 Kwords | BF0000h-BF7FFFh |
| | BA381 | 32 Kwords | BE8000h-BEFFFFh |
| | BA380 | 32 Kwords | BE0000h-BE7FFFh |
| | BA379 | 32 Kwords | BD8000h-BDFFFFh |
| | BA378 | 32 Kwords | BD0000h-BD7FFFh |
| | BA377 | 32 Kwords | BC8000h-BCFFFFh |
| | BA376 | 32 Kwords | BC0000h-BC7FFFh |
| | BA375 | 32 Kwords | BB8000h-BBFFFFh |
| | BA374 | 32 Kwords | BB0000h-BB7FFFh |
| | BA373 | 32 Kwords | BA8000h-BAFFFFh |
| | BA372 | 32 Kwords | BA0000h-BA7FFFh |
| | BA371 | 32 Kwords | B98000h-B9FFFFh |
| | BA370 | 32 Kwords | B90000h-B97FFFh |
| | BA369 | 32 Kwords | B88000h-B8FFFFh |
| | BA368 | 32 Kwords | B80000h-B87FFFh |
| | BA367 | 32 Kwords | B78000h-B7FFFFh |
| | BA366 | 32 Kwords | B70000h-B77FFFh |
| | BA365 | 32 Kwords | B68000h-B6FFFFh |
| | BA364 | 32 Kwords | B60000h-B67FFFh |
| | BA363 | 32 Kwords | B58000h-B5FFFFh |
| | BA362 | 32 Kwords | B50000h-B57FFFh |
| | BA361 | 32 Kwords | B48000h-B4FFFFh |
| | BA360 | 32 Kwords | B40000h-B47FFFh |
| | BA359 | 32 Kwords | B38000h-B3FFFFh |
| | BA358 | 32 Kwords | B30000h-B37FFFh |
| | BA357 | 32 Kwords | B28000h-B2FFFFh |
| | BA356 | 32 Kwords | B20000h-B27FFFh |
| | BA355 | 32 Kwords | B18000h-B1FFFFh |
| | BA354 | 32 Kwords | B10000h-B17FFFh |
| | BA353 | 32 Kwords | B08000h-B0FFFFh |
| | BA352 | 32 Kwords | B00000h-B07FFFh |
| Bank 5 | BA351 | 32 Kwords | AF8000h-AFFFFFh |
| | BA350 | 32 Kwords | AF0000h-AF7FFFh |
| | BA349 | 32 Kwords | AE8000h-AEFFFFh |
| | BA348 | 32 Kwords | AE0000h-AE7FFFh |
| | BA347 | 32 Kwords | AD8000h-ADFFFFh |
| | BA346 | 32 Kwords | AD0000h-AD7FFFh |
| | BA345 | 32 Kwords | AC8000h-ACFFFFh |
| | BA344 | 32 Kwords | AC0000h-AC7FFFh |
| | BA343 | 32 Kwords | AB8000h-ABFFFFh |
| | BA342 | 32 Kwords | AB0000h-AB7FFFh |
| | BA341 | 32 Kwords | AA8000h-AAFFFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 5 | BA340 | 32 Kwords | AA0000h-AA7FFFh |
| | BA339 | 32 Kwords | A98000h-A9FFFFh |
| | BA338 | 32 Kwords | A90000h-A97FFFh |
| | BA337 | 32 Kwords | A88000h-A8FFFFh |
| | BA336 | 32 Kwords | A80000h-A87FFFh |
| | BA335 | 32 Kwords | A78000h-A7FFFFh |
| | BA334 | 32 Kwords | A70000h-A77FFFh |
| | BA333 | 32 Kwords | A68000h-A6FFFFh |
| | BA332 | 32 Kwords | A60000h-A67FFFh |
| | BA331 | 32 Kwords | A58000h-A5FFFFh |
| | BA330 | 32 Kwords | A50000h-A57FFFh |
| | BA329 | 32 Kwords | A48000h-A4FFFFh |
| | BA328 | 32 Kwords | A40000h-A47FFFh |
| | BA327 | 32 Kwords | A38000h-A3FFFFh |
| | BA326 | 32 Kwords | A30000h-A37FFFh |
| | BA325 | 32 Kwords | A28000h-A2FFFFh |
| | BA324 | 32 Kwords | A20000h-A27FFFh |
| | BA323 | 32 Kwords | A18000h-A1FFFFh |
| | BA322 | 32 Kwords | A10000h-A17FFFh |
| | BA321 | 32 Kwords | A08000h-A0FFFFh |
| | BA320 | 32 Kwords | A00000h-A07FFFh |
| Bank 6 | BA319 | 32 Kwords | 9F8000h-9FFFFFh |
| | BA318 | 32 Kwords | 9F0000h-9F7FFFh |
| | BA317 | 32 Kwords | 9E8000h-9EFFFFh |
| | BA316 | 32 Kwords | 9E0000h-9E7FFFh |
| | BA315 | 32 Kwords | 9D8000h-9DFFFFh |
| | BA314 | 32 Kwords | 9D0000h-9D7FFFh |
| | BA313 | 32 Kwords | 9C8000h-9CFFFFh |
| | BA312 | 32 Kwords | 9C0000h-9C7FFFh |
| | BA311 | 32 Kwords | 9B8000h-9BFFFFh |
| | BA310 | 32 Kwords | 9B0000h-9B7FFFh |
| | BA309 | 32 Kwords | 9A8000h-9AFFFFh |
| | BA308 | 32 Kwords | 9A0000h-9A7FFFh |
| | BA307 | 32 Kwords | 998000h-99FFFFh |
| | BA306 | 32 Kwords | 990000h-997FFFh |
| | BA305 | 32 Kwords | 988000h-98FFFFh |
| | BA304 | 32 Kwords | 980000h-987FFFh |
| | BA303 | 32 Kwords | 978000h-97FFFFh |
| | BA302 | 32 Kwords | 970000h-977FFFh |
| | BA301 | 32 Kwords | 968000h-96FFFFh |
| | BA300 | 32 Kwords | 960000h-967FFFh |
| | BA299 | 32 Kwords | 958000h-95FFFFh |
| | BA298 | 32 Kwords | 950000h-957FFFh |
| | BA297 | 32 Kwords | 948000h-94FFFFh |
| | BA296 | 32 Kwords | 940000h-947FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 6 | BA295 | 32 Kwords | 938000h-93FFFFh |
| | BA294 | 32 Kwords | 930000h-937FFFh |
| | BA293 | 32 Kwords | 928000h-92FFFFh |
| | BA292 | 32 Kwords | 920000h-927FFFh |
| | BA291 | 32 Kwords | 918000h-91FFFFh |
| | BA290 | 32 Kwords | 910000h-917FFFh |
| | BA289 | 32 Kwords | 908000h-90FFFFh |
| | BA288 | 32 Kwords | 900000h-907FFFh |
| Bank 7 | BA287 | 32 Kwords | 8F8000h-8FFFFFh |
| | BA286 | 32 Kwords | 8F0000h-8F7FFFh |
| | BA285 | 32 Kwords | 8E8000h-8EFFFFh |
| | BA284 | 32 Kwords | 8E0000h-8E7FFFh |
| | BA283 | 32 Kwords | 8D8000h-8DFFFFh |
| | BA282 | 32 Kwords | 8D0000h-8D7FFFh |
| | BA281 | 32 Kwords | 8C8000h-8CFFFFh |
| | BA280 | 32 Kwords | 8C0000h-8C7FFFh |
| | BA279 | 32 Kwords | 8B8000h-8BFFFFh |
| | BA278 | 32 Kwords | 8B0000h-8B7FFFh |
| | BA277 | 32 Kwords | 8A8000h-8AFFFFh |
| | BA276 | 32 Kwords | 8A0000h-8A7FFFh |
| | BA275 | 32 Kwords | 898000h-89FFFFh |
| | BA274 | 32 Kwords | 890000h-897FFFh |
| | BA273 | 32 Kwords | 888000h-88FFFFh |
| | BA272 | 32 Kwords | 880000h-887FFFh |
| | BA271 | 32 Kwords | 878000h-87FFFFh |
| | BA270 | 32 Kwords | 870000h-877FFFh |
| | BA269 | 32 Kwords | 868000h-86FFFFh |
| | BA268 | 32 Kwords | 860000h-867FFFh |
| | BA267 | 32 Kwords | 858000h-85FFFFh |
| | BA266 | 32 Kwords | 850000h-857FFFh |
| | BA265 | 32 Kwords | 848000h-84FFFFh |
| | BA264 | 32 Kwords | 840000h-847FFFh |
| | BA263 | 32 Kwords | 838000h-83FFFFh |
| | BA262 | 32 Kwords | 830000h-837FFFh |
| | BA261 | 32 Kwords | 828000h-82FFFFh |
| | BA260 | 32 Kwords | 820000h-827FFFh |
| | BA259 | 32 Kwords | 818000h-81FFFFh |
| | BA258 | 32 Kwords | 810000h-817FFFh |
| | BA257 | 32 Kwords | 808000h-80FFFFh |
| | BA256 | 32 Kwords | 800000h-807FFFh |

**Table 3-1. Top Boot Boot Block Address Table(K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 8 | BA255 | 32 Kwords | 7F8000h-7FFFFFh |
| | BA254 | 32 Kwords | 7F0000h-7F7FFFh |
| | BA253 | 32 Kwords | 7E8000h-7EFFFFh |
| | BA252 | 32 Kwords | 7E0000h-7E7FFFh |
| | BA251 | 32 Kwords | 7D8000h-7DFFFFh |
| | BA250 | 32 Kwords | 7D0000h-7D7FFFh |
| | BA249 | 32 Kwords | 7C8000h-7CFFFFh |
| | BA248 | 32 Kwords | 7C0000h-7C7FFFh |
| | BA247 | 32 Kwords | 7B8000h-7BFFFFh |
| | BA246 | 32 Kwords | 7B0000h-7B7FFFh |
| | BA245 | 32 Kwords | 7A8000h-7AFFFFh |
| | BA244 | 32 Kwords | 7A0000h-7A7FFFh |
| | BA243 | 32 Kwords | 798000h-79FFFFh |
| | BA242 | 32 Kwords | 790000h-797FFFh |
| | BA241 | 32 Kwords | 788000h-78FFFFh |
| | BA240 | 32 Kwords | 780000h-787FFFh |
| | BA239 | 32 Kwords | 778000h-77FFFFh |
| | BA238 | 32 Kwords | 770000h-777FFFh |
| | BA237 | 32 Kwords | 768000h-76FFFFh |
| | BA236 | 32 Kwords | 760000h-767FFFh |
| | BA235 | 32 Kwords | 758000h-75FFFFh |
| | BA234 | 32 Kwords | 750000h-757FFFh |
| | BA233 | 32 Kwords | 748000h-74FFFFh |
| | BA232 | 32 Kwords | 740000h-747FFFh |
| | BA231 | 32 Kwords | 738000h-73FFFFh |
| | BA230 | 32 Kwords | 730000h-737FFFh |
| | BA229 | 32 Kwords | 728000h-72FFFFh |
| | BA228 | 32 Kwords | 720000h-727FFFh |
| | BA227 | 32 Kwords | 718000h-71FFFFh |
| | BA226 | 32 Kwords | 710000h-717FFFh |
| | BA225 | 32 Kwords | 708000h-70FFFFh |
| | BA224 | 32 kwords | 700000h-707FFFh |
| Bank 9 | BA223 | 32 Kwords | 6F8000h-6FFFFFh |
| | BA222 | 32 Kwords | 6F0000h-6F7FFFh |
| | BA221 | 32 Kwords | 6E8000h-6EFFFFh |
| | BA220 | 32 Kwords | 6E0000h-6E7FFFh |
| | BA219 | 32 Kwords | 6D8000h-6DFFFFh |
| | BA218 | 32 Kwords | 6D0000h-6D7FFFh |
| | BA217 | 32 Kwords | 6C8000h-6CFFFFh |
| | BA216 | 32 Kwords | 6C0000h-6C7FFFh |
| | BA215 | 32 Kwords | 6B8000h-6BFFFFh |
| | BA214 | 32 Kwords | 6B0000h-6B7FFFh |
| | BA213 | 32 Kwords | 6A8000h-6AFFFFh |
| | BA212 | 32 Kwords | 6A0000h-6A7FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 9 | BA211 | 32 Kwords | 698000h-69FFFFh |
| | BA210 | 32 Kwords | 690000h-697FFFh |
| | BA209 | 32 Kwords | 688000h-68FFFFh |
| | BA208 | 32 Kwords | 680000h-687FFFh |
| | BA207 | 32 Kwords | 678000h-67FFFFh |
| | BA206 | 32 Kwords | 670000h-677FFFh |
| | BA205 | 32 Kwords | 668000h-66FFFFh |
| | BA204 | 32 Kwords | 660000h-667FFFh |
| | BA203 | 32 Kwords | 658000h-65FFFFh |
| | BA202 | 32 Kwords | 650000h-657FFFh |
| | BA201 | 32 Kwords | 648000h-64FFFFh |
| | BA200 | 32 Kwords | 640000h-647FFFh |
| | BA199 | 32 Kwords | 638000h-63FFFFh |
| | BA198 | 32 Kwords | 630000h-637FFFh |
| | BA197 | 32 Kwords | 628000h-62FFFFh |
| | BA196 | 32 Kwords | 620000h-627FFFh |
| | BA195 | 32 Kwords | 618000h-61FFFFh |
| | BA194 | 32 Kwords | 610000h-617FFFh |
| | BA193 | 32 Kwords | 608000h-60FFFFh |
| | BA192 | 32 Kwords | 600000h-607FFFh |
| Bank 10 | BA191 | 32 Kwords | 5F8000h-5FFFFFh |
| | BA190 | 32 Kwords | 5F0000h-5F7FFFh |
| | BA189 | 32 Kwords | 5E8000h-5EFFFFh |
| | BA188 | 32 Kwords | 5E0000h-5E7FFFh |
| | BA187 | 32 Kwords | 5D8000h-5DFFFFh |
| | BA186 | 32 Kwords | 5D0000h-5D7FFFh |
| | BA185 | 32 Kwords | 5C8000h-5CFFFFh |
| | BA184 | 32 Kwords | 5C0000h-5C7FFFh |
| | BA183 | 32 Kwords | 5B8000h-5BFFFFh |
| | BA182 | 32 Kwords | 5B0000h-5B7FFFh |
| | BA181 | 32 Kwords | 5A8000h-5AFFFFh |
| | BA180 | 32 Kwords | 5A0000h-5A7FFFh |
| | BA179 | 32 Kwords | 598000h-59FFFFh |
| | BA178 | 32 Kwords | 590000h-597FFFh |
| | BA177 | 32 Kwords | 588000h-58FFFFh |
| | BA176 | 32 Kwords | 580000h-587FFFh |
| | BA175 | 32 Kwords | 578000h-57FFFFh |
| | BA174 | 32 Kwords | 570000h-577FFFh |
| | BA173 | 32 Kwords | 568000h-56FFFFh |
| | BA172 | 32 Kwords | 560000h-567FFFh |
| | BA171 | 32 Kwords | 558000h-55FFFFh |
| | BA170 | 32 Kwords | 550000h-557FFFh |
| | BA169 | 32 Kwords | 548000h-54FFFFh |
| | BA168 | 32 Kwords | 540000h-547FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 10 | BA167 | 32 Kwords | 538000h-53FFFFh |
| | BA166 | 32 Kwords | 530000h-537FFFh |
| | BA165 | 32 Kwords | 528000h-52FFFFh |
| | BA164 | 32 Kwords | 520000h-527FFFh |
| | BA163 | 32 Kwords | 518000h-51FFFFh |
| | BA162 | 32 Kwords | 510000h-517FFFh |
| | BA161 | 32 Kwords | 508000h-50FFFFh |
| | BA160 | 32 Kwords | 500000h-507FFFh |
| Bank 11 | BA159 | 32 Kwords | 4F8000h-4FFFFFh |
| | BA158 | 32 Kwords | 4F0000h-4F7FFFh |
| | BA157 | 32 Kwords | 4E8000h-4EFFFFh |
| | BA156 | 32 Kwords | 4E0000h-4E7FFFh |
| | BA155 | 32 Kwords | 4D8000h-4DFFFFh |
| | BA154 | 32 Kwords | 4D0000h-4D7FFFh |
| | BA153 | 32 Kwords | 4C8000h-4CFFFFh |
| | BA152 | 32 Kwords | 4C0000h-4C7FFFh |
| | BA151 | 32 Kwords | 4B8000h-4BFFFFh |
| | BA150 | 32 Kwords | 4B0000h-4B7FFFh |
| | BA149 | 32 Kwords | 4A8000h-4AFFFFh |
| | BA148 | 32 Kwords | 4A0000h-4A7FFFh |
| | BA147 | 32 Kwords | 498000h-49FFFFh |
| | BA146 | 32 Kwords | 490000h-497FFFh |
| | BA145 | 32 Kwords | 488000h-48FFFFh |
| | BA144 | 32 Kwords | 480000h-487FFFh |
| | BA143 | 32 Kwords | 478000h-47FFFFh |
| | BA142 | 32 Kwords | 470000h-477FFFh |
| | BA141 | 32 Kwords | 468000h-46FFFFh |
| | BA140 | 32 Kwords | 460000h-467FFFh |
| | BA139 | 32 Kwords | 458000h-45FFFFh |
| | BA138 | 32 Kwords | 450000h-457FFFh |
| | BA137 | 32 Kwords | 448000h-44FFFFh |
| | BA136 | 32 Kwords | 440000h-447FFFh |
| | BA135 | 32 Kwords | 438000h-43FFFFh |
| | BA134 | 32 Kwords | 430000h-437FFFh |
| | BA133 | 32 Kwords | 428000h-42FFFFh |
| | BA132 | 32 Kwords | 420000h-427FFFh |
| | BA131 | 32 Kwords | 418000h-41FFFFh |
| | BA130 | 32 Kwords | 410000h-417FFFh |
| | BA129 | 32 Kwords | 408000h-40FFFFh |
| | BA128 | 32 Kwords | 400000h-407FFFh |
| Bank 12 | BA127 | 32 Kwords | 3F8000h-3FFFFFh |
| | BA126 | 32 Kwords | 3F0000h-3F7FFFh |
| | BA125 | 32 Kwords | 3E8000h-3EFFFFh |
| | BA124 | 32 Kwords | 3E0000h-3E7FFFh |
| | BA123 | 32 Kwords | 3D8000h-3DFFFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 12 | BA122 | 32 Kwords | 3D0000h-3D7FFFh |
| | BA121 | 32 Kwords | 3C8000h-3CFFFFh |
| | BA120 | 32 Kwords | 3C0000h-3C7FFFh |
| | BA119 | 32 Kwords | 3B8000h-3BFFFFh |
| | BA118 | 32 Kwords | 3B0000h-3B7FFFh |
| | BA117 | 32 Kwords | 3A8000h-3AFFFFh |
| | BA116 | 32 Kwords | 3A0000h-3A7FFFh |
| | BA115 | 32 Kwords | 398000h-39FFFFh |
| | BA114 | 32 Kwords | 390000h-397FFFh |
| | BA113 | 32 Kwords | 388000h-38FFFFh |
| | BA112 | 32 Kwords | 380000h-387FFFh |
| | BA111 | 32 Kwords | 378000h-37FFFFh |
| | BA110 | 32 Kwords | 370000h-377FFFh |
| | BA109 | 32 Kwords | 368000h-36FFFFh |
| | BA108 | 32 Kwords | 360000h-367FFFh |
| | BA107 | 32 Kwords | 358000h-35FFFFh |
| | BA106 | 32 Kwords | 350000h-357FFFh |
| | BA105 | 32 Kwords | 348000h-34FFFFh |
| | BA104 | 32 Kwords | 340000h-347FFFh |
| | BA103 | 32 Kwords | 338000h-33FFFFh |
| | BA102 | 32 Kwords | 330000h-337FFFh |
| | BA101 | 32 Kwords | 328000h-32FFFFh |
| | BA100 | 32 Kwords | 320000h-327FFFh |
| | BA99 | 32 Kwords | 318000h-31FFFFh |
| | BA98 | 32 Kwords | 310000h-317FFFh |
| | BA97 | 32 Kwords | 308000h-30FFFFh |
| | BA96 | 32 Kwords | 300000h-307FFFh |
| Bank 13 | BA95 | 32 Kwords | 2F8000h-2FFFFFh |
| | BA94 | 32 Kwords | 2F0000h-2F7FFFh |
| | BA93 | 32 Kwords | 2E8000h-2EFFFFh |
| | BA92 | 32 Kwords | 2E0000h-2E7FFFh |
| | BA91 | 32 Kwords | 2D8000h-2DFFFFh |
| | BA90 | 32 Kwords | 2D0000h-2D7FFFh |
| | BA89 | 32 Kwords | 2C8000h-2CFFFFh |
| | BA88 | 32 Kwords | 2C0000h-2C7FFFh |
| | BA87 | 32 Kwords | 2B8000h-2BFFFFh |
| | BA86 | 32 Kwords | 2B0000h-2B7FFFh |
| | BA85 | 32 Kwords | 2A8000h-2AFFFFh |
| | BA84 | 32 Kwords | 2A0000h-2A7FFFh |
| | BA83 | 32 Kwords | 298000h-29FFFFh |
| | BA82 | 32 Kwords | 290000h-297FFFh |
| | BA81 | 32 Kwords | 288000h-28FFFFh |
| | BA80 | 32 Kwords | 280000h-287FFFh |
| | BA79 | 32 Kwords | 278000h-27FFFFh |
| | BA78 | 32 Kwords | 270000h-277FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 13 | BA77 | 32 Kwords | 268000h-26FFFFh |
| | BA76 | 32 Kwords | 260000h-267FFFh |
| | BA75 | 32 Kwords | 258000h-25FFFFh |
| | BA74 | 32 Kwords | 250000h-257FFFh |
| | BA73 | 32 Kwords | 248000h-24FFFFh |
| | BA72 | 32 Kwords | 240000h-247FFFh |
| | BA71 | 32 Kwords | 238000h-23FFFFh |
| | BA70 | 32 Kwords | 230000h-237FFFh |
| | BA69 | 32 Kwords | 228000h-22FFFFh |
| | BA68 | 32 Kwords | 220000h-227FFFh |
| | BA67 | 32 Kwords | 218000h-21FFFFh |
| | BA66 | 32 Kwords | 210000h-217FFFh |
| | BA65 | 32 Kwords | 208000h-20FFFFh |
| | BA64 | 32 Kwords | 200000h-207FFFh |
| Bank 14 | BA63 | 32 Kwords | 1F8000h-1FFFFFh |
| | BA62 | 32 Kwords | 1F0000h-1F7FFFh |
| | BA61 | 32 Kwords | 1E8000h-1EFFFFh |
| | BA60 | 32 Kwords | 1E0000h-1E7FFFh |
| | BA59 | 32 Kwords | 1D8000h-1DFFFFh |
| | BA58 | 32 Kwords | 1D0000h-1D7FFFh |
| | BA57 | 32 Kwords | 1C8000h-1CFFFFh |
| | BA56 | 32 Kwords | 1C0000h-1C7FFFh |
| | BA55 | 32 Kwords | 1B8000h-1BFFFFh |
| | BA54 | 32 Kwords | 1B0000h-1B7FFFh |
| | BA53 | 32 Kwords | 1A8000h-1AFFFFh |
| | BA52 | 32 Kwords | 1A0000h-1A7FFFh |
| | BA51 | 32 Kwords | 198000h-19FFFFh |
| | BA50 | 32 Kwords | 190000h-197FFFh |
| | BA49 | 32 Kwords | 188000h-18FFFFh |
| | BA48 | 32 Kwords | 180000h-187FFFh |
| | BA47 | 32 Kwords | 178000h-17FFFFh |
| | BA46 | 32 Kwords | 170000h-177FFFh |
| | BA45 | 32 Kwords | 168000h-16FFFFh |
| | BA44 | 32 Kwords | 160000h-167FFFh |
| | BA43 | 32 Kwords | 158000h-15FFFFh |
| | BA42 | 32 Kwords | 150000h-157FFFh |
| | BA41 | 32 Kwords | 148000h-14FFFFh |
| | BA40 | 32 Kwords | 140000h-147FFFh |
| | BA39 | 32 Kwords | 138000h-13FFFFh |
| | BA38 | 32 Kwords | 130000h-137FFFh |
| | BA37 | 32 Kwords | 128000h-12FFFFh |
| | BA36 | 32 Kwords | 120000h-127FFFh |
| | BA35 | 32 Kwords | 118000h-11FFFFh |
| | BA34 | 32 Kwords | 110000h-117FFFh |
| | BA33 | 32 Kwords | 108000h-10FFFFh |
| | BA32 | 32 Kwords | 100000h-107FFFh |

**Table 3-1. Top Boot Block Address Table (K8A5615ETA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 15 | BA31 | 32 Kwords | 0F8000h-0FFFFFh |
| | BA30 | 32 Kwords | 0F0000h-0F7FFFh |
| | BA29 | 32 Kwords | 0E8000h-0EFFFFh |
| | BA28 | 32 Kwords | 0E0000h-0E7FFFh |
| | BA27 | 32 Kwords | 0D8000h-0DFFFFh |
| | BA26 | 32 Kwords | 0D0000h-0D7FFFh |
| | BA25 | 32 Kwords | 0C8000h-0CFFFFh |
| | BA24 | 32 Kwords | 0C0000h-0C7FFFh |
| | BA23 | 32 Kwords | 0B8000h-0BFFFFh |
| | BA22 | 32 Kwords | 0B0000h-0B7FFFh |
| | BA21 | 32 Kwords | 0A8000h-0AFFFFh |
| | BA20 | 32 Kwords | 0A0000h-0A7FFFh |
| | BA19 | 32 Kwords | 098000h-09FFFFh |
| | BA18 | 32 Kwords | 090000h-097FFFh |
| | BA17 | 32 Kwords | 088000h-08FFFFh |
| | BA16 | 32 Kwords | 080000h-087FFFh |
| | BA15 | 32 Kwords | 078000h-07FFFFh |
| | BA14 | 32 Kwords | 070000h-077FFFh |
| | BA13 | 32 Kwords | 068000h-06FFFFh |
| | BA12 | 32 Kwords | 060000h-067FFFh |
| | BA11 | 32 Kwords | 058000h-05FFFFh |
| | BA10 | 32 Kwords | 050000h-057FFFh |
| | BA9 | 32 Kwords | 048000h-04FFFFh |
| | BA8 | 32 Kwords | 040000h-047FFFh |
| | BA7 | 32 Kwords | 038000h-03FFFFh |
| | BA6 | 32 Kwords | 030000h-037FFFh |
| | BA5 | 32 Kwords | 028000h-02FFFFh |
| | BA4 | 32 Kwords | 020000h-027FFFh |
| | BA3 | 32 Kwords | 018000h-01FFFFh |
| | BA2 | 32 Kwords | 010000h-017FFFh |
| | BA1 | 32 Kwords | 008000h-00FFFFh |
| | BA0 | 32 Kwords | 000000h-007FFFh |

**Table 3-1-1. Top Boot Block OTP Addresses Table (K8A5615ETA)**

| OTP | Block Address A23 ~ A8 | Block Size | (x16) Address Range |
|---|---|---|---|
| | FFFFh | 128words | FFFF80h-FFFFFFh |

**After entering OTP block, any issued addresses should be in the range of OTP block address**

**Table 3-1. Bottom Boot Block Address Table(K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 15 | BA518 | 32 Kwords | FF8000h-FFFFFFh |
| | BA517 | 32 Kwords | FF0000h-FF7FFFh |
| | BA516 | 32 Kwords | FE8000h-FEFFFFh |
| | BA515 | 32 Kwords | FE0000h-FE7FFFh |
| | BA514 | 32 Kwords | FD8000h-FDFFFFh |
| | BA513 | 32 Kwords | FD0000h-FD7FFFh |
| | BA512 | 32 Kwords | FC8000h-FCFFFFh |
| | BA511 | 32 Kwords | FC0000h-FC7FFFh |
| | BA510 | 32 Kwords | FB8000h-FBFFFFh |
| | BA509 | 32 Kwords | FB0000h-FB7FFFh |
| | BA508 | 32 Kwords | FA8000h-FAFFFFh |
| | BA507 | 32 Kwords | FA0000h-FA7FFFh |
| | BA506 | 32 Kwords | F98000h-F9FFFFh |
| | BA505 | 32 Kwords | F90000h-F97FFFh |
| | BA504 | 32 Kwords | F88000h-F8FFFFh |
| | BA503 | 32 Kwords | F80000h-F87FFFh |
| | BA502 | 32 Kwords | F78000h-F7FFFFh |
| | BA501 | 32 Kwords | F70000h-F77FFFh |
| | BA500 | 32 Kwords | F68000h-F6FFFFh |
| | BA499 | 32 Kwords | F60000h-F67FFFh |
| | BA498 | 32 Kwords | F58000h-F5FFFFh |
| | BA497 | 32 Kwords | F50000h-F57FFFh |
| | BA496 | 32 Kwords | F48000h-F4FFFFh |
| | BA495 | 32 Kwords | F40000h-F47FFFh |
| | BA494 | 32 Kwords | F38000h-F3FFFFh |
| | BA493 | 32 Kwords | F30000h-F37FFFh |
| | BA492 | 32 Kwords | F28000h-F2FFFFh |
| | BA491 | 32 Kwords | F20000h-F27FFFh |
| | BA490 | 32 Kwords | F18000h-F1FFFFh |
| | BA489 | 32 Kwords | F10000h-F17FFFh |
| | BA488 | 32 Kwords | F08000h-F0FFFFh |
| | BA487 | 32 kwords | F00000h-F07FFFh |
| Bank 14 | BA486 | 32 Kwords | EF8000h-EFFFFFh |
| | BA485 | 32 Kwords | EF0000h-EF7FFFh |
| | BA484 | 32 Kwords | EE8000h-EEFFFFh |
| | BA483 | 32 Kwords | EE0000h-EE7FFFh |
| | BA482 | 32 Kwords | ED8000h-EDFFFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 14 | BA481 | 32 Kwords | ED0000h-ED7FFFh |
| | BA480 | 32 Kwords | EC8000h-ECFFFFh |
| | BA479 | 32 Kwords | EC0000h-EC7FFFh |
| | BA478 | 32 Kwords | EB8000h-EBFFFFh |
| | BA477 | 32 Kwords | EB0000h-EB7FFFh |
| | BA476 | 32 Kwords | EA8000h-EAFFFFh |
| | BA475 | 32 Kwords | EA0000h-EA7FFFh |
| | BA474 | 32 Kwords | E98000h-E9FFFFh |
| | BA473 | 32 Kwords | E90000h-E97FFFh |
| | BA472 | 32 Kwords | E88000h-E8FFFFh |
| | BA471 | 32 Kwords | E80000h-E87FFFh |
| | BA470 | 32 Kwords | E78000h-E7FFFFh |
| | BA469 | 32 Kwords | E70000h-E77FFFh |
| | BA468 | 32 Kwords | E68000h-E6FFFFh |
| | BA467 | 32 Kwords | E60000h-E67FFFh |
| | BA466 | 32 Kwords | E58000h-E5FFFFh |
| | BA465 | 32 Kwords | E50000h-E57FFFh |
| | BA464 | 32 Kwords | E48000h-E4FFFFh |
| | BA463 | 32 Kwords | E40000h-E47FFFh |
| | BA462 | 32 Kwords | E38000h-E3FFFFh |
| | BA461 | 32 Kwords | E30000h-E37FFFh |
| | BA460 | 32 Kwords | E28000h-E2FFFFh |
| | BA459 | 32 Kwords | E20000h-E27FFFh |
| | BA458 | 32 Kwords | E18000h-E1FFFFh |
| | BA457 | 32 Kwords | E10000h-E17FFFh |
| | BA456 | 32 Kwords | E08000h-E0FFFFh |
| | BA455 | 32 Kwords | E00000h-E07FFFh |
| Bank 13 | BA454 | 32 Kwords | DF8000h-DFFFFFh |
| | BA453 | 32 Kwords | DF0000h-DF7FFFh |
| | BA452 | 32 Kwords | DE8000h-DEFFFFh |
| | BA451 | 32 Kwords | DE0000h-DE7FFFh |
| | BA450 | 32 Kwords | DD8000h-DDFFFFh |
| | BA449 | 32 Kwords | DD0000h-DD7FFFh |
| | BA448 | 32 Kwords | DC8000h-DCFFFFh |
| | BA447 | 32 Kwords | DC0000h-DC7FFFh |
| | BA446 | 32 Kwords | DB8000h-DBFFFFh |
| | BA445 | 32 Kwords | DB0000h-DB7FFFh |
| | BA444 | 32 Kwords | DA8000h-DAFFFFh |
| | BA443 | 32 Kwords | DA0000h-DA7FFFh |
| | BA442 | 32 Kwords | D98000h-D9FFFFh |
| | BA441 | 32 Kwords | D90000h-D97FFFh |
| | BA440 | 32 Kwords | D88000h-D8FFFFh |
| | BA439 | 32 Kwords | D80000h-D87FFFh |
| | BA438 | 32 Kwords | D78000h-D7FFFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 13 | BA437 | 32 Kwords | D70000h-D77FFFh |
| | BA436 | 32 Kwords | D68000h-D6FFFFh |
| | BA435 | 32 Kwords | D60000h-D67FFFh |
| | BA434 | 32 Kwords | D58000h-D5FFFFh |
| | BA433 | 32 Kwords | D50000h-D57FFFh |
| | BA432 | 32 Kwords | D48000h-D4FFFFh |
| | BA431 | 32 Kwords | D40000h-D47FFFh |
| | BA430 | 32 Kwords | D38000h-D3FFFFh |
| | BA429 | 32 Kwords | D30000h-D37FFFh |
| | BA428 | 32 Kwords | D28000h-D2FFFFh |
| | BA427 | 32 Kwords | D20000h-D27FFFh |
| | BA426 | 32 Kwords | D18000h-D1FFFFh |
| | BA425 | 32 Kwords | D10000h-D17FFFh |
| | BA424 | 32 Kwords | D08000h-D0FFFFh |
| | BA423 | 32 Kwords | D00000h-D07FFFh |
| Bank 12 | BA422 | 32 Kwords | CF8000h-CFFFFFh |
| | BA421 | 32 Kwords | CF0000h-CF7FFFh |
| | BA420 | 32 Kwords | CE8000h-CEFFFFh |
| | BA419 | 32 Kwords | CE0000h-CE7FFFh |
| | BA418 | 32 Kwords | CD8000h-CDFFFFh |
| | BA417 | 32 Kwords | CD0000h-CD7FFFh |
| | BA416 | 32 Kwords | CC8000h-CCFFFFh |
| | BA415 | 32 Kwords | CC0000h-CC7FFFh |
| | BA414 | 32 Kwords | CB8000h-CBFFFFh |
| | BA413 | 32 Kwords | CB0000h-CB7FFFh |
| | BA412 | 32 Kwords | CA8000h-CAFFFFh |
| | BA411 | 32 Kwords | CA0000h-CA7FFFh |
| | BA410 | 32 Kwords | C98000h-C9FFFFh |
| | BA409 | 32 Kwords | C90000h-C97FFFh |
| | BA408 | 32 Kwords | C88000h-C8FFFFh |
| | BA407 | 32 Kwords | C80000h-C87FFFh |
| | BA406 | 32 Kwords | C78000h-C7FFFFh |
| | BA405 | 32 Kwords | C70000h-C77FFFh |
| | BA404 | 32 Kwords | C68000h-C6FFFFh |
| | BA403 | 32 Kwords | C60000h-C67FFFh |
| | BA402 | 32 Kwords | C58000h-C5FFFFh |
| | BA401 | 32 Kwords | C50000h-C57FFFh |
| | BA400 | 32 Kwords | C48000h-C4FFFFh |
| | BA399 | 32 Kwords | C40000h-C47FFFh |
| | BA398 | 32 Kwords | C38000h-C3FFFFh |
| | BA397 | 32 Kwords | C30000h-C37FFFh |
| | BA396 | 32 Kwords | C28000h-C2FFFFh |
| | BA395 | 32 Kwords | C20000h-C27FFFh |
| | BA394 | 32 Kwords | C18000h-C1FFFFh |
| | BA393 | 32 Kwords | C10000h-C17FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 12 | BA392 | 32 Kwords | C08000h-C0FFFFh |
| | BA391 | 32 Kwords | C00000h-C07FFFh |
| Bank 11 | BA390 | 32 Kwords | BF8000h-BFFFFFh |
| | BA389 | 32 Kwords | BF0000h-BF7FFFh |
| | BA388 | 32 Kwords | BE8000h-BEFFFFh |
| | BA387 | 32 Kwords | BE0000h-BE7FFFh |
| | BA386 | 32 Kwords | BD8000h-BDFFFFh |
| | BA385 | 32 Kwords | BD0000h-BD7FFFh |
| | BA384 | 32 Kwords | BC8000h-BCFFFFh |
| | BA383 | 32 Kwords | BC0000h-BC7FFFh |
| | BA382 | 32 Kwords | BB8000h-BBFFFFh |
| | BA381 | 32 Kwords | BB0000h-BB7FFFh |
| | BA380 | 32 Kwords | BA8000h-BAFFFFh |
| | BA379 | 32 Kwords | BA0000h-BA7FFFh |
| | BA378 | 32 Kwords | B98000h-B9FFFFh |
| | BA377 | 32 Kwords | B90000h-B97FFFh |
| | BA376 | 32 Kwords | B88000h-B8FFFFh |
| | BA375 | 32 Kwords | B80000h-B87FFFh |
| | BA374 | 32 Kwords | B78000h-B7FFFFh |
| | BA373 | 32 Kwords | B70000h-B77FFFh |
| | BA372 | 32 Kwords | B68000h-B6FFFFh |
| | BA371 | 32 Kwords | B60000h-B67FFFh |
| | BA370 | 32 Kwords | B58000h-B5FFFFh |
| | BA369 | 32 Kwords | B50000h-B57FFFh |
| | BA368 | 32 Kwords | B48000h-B4FFFFh |
| | BA367 | 32 Kwords | B40000h-B47FFFh |
| | BA366 | 32 Kwords | B38000h-B3FFFFh |
| | BA365 | 32 Kwords | B30000h-B37FFFh |
| | BA364 | 32 Kwords | B28000h-B2FFFFh |
| | BA363 | 32 Kwords | B20000h-B27FFFh |
| | BA362 | 32 Kwords | B18000h-B1FFFFh |
| | BA361 | 32 Kwords | B10000h-B17FFFh |
| | BA360 | 32 Kwords | B08000h-B0FFFFh |
| | BA359 | 32 Kwords | B00000h-B07FFFh |
| Bank 10 | BA358 | 32 Kwords | AF8000h-AFFFFFh |
| | BA357 | 32 Kwords | AF0000h-AF7FFFh |
| | BA356 | 32 Kwords | AE8000h-AEFFFFh |
| | BA355 | 32 Kwords | AE0000h-AE7FFFh |
| | BA354 | 32 Kwords | AD8000h-ADFFFFh |
| | BA353 | 32 Kwords | AD0000h-AD7FFFh |
| | BA352 | 32 Kwords | AC8000h-ACFFFFh |
| | BA351 | 32 Kwords | AC0000h-AC7FFFh |
| | BA350 | 32 Kwords | AB8000h-ABFFFFh |
| | BA349 | 32 Kwords | AB0000h-AB7FFFh |
| | BA348 | 32 Kwords | AA8000h-AAFFFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 10 | BA347 | 32 Kwords | AA0000h-AA7FFFh |
| | BA346 | 32 Kwords | A98000h-A9FFFFh |
| | BA345 | 32 Kwords | A90000h-A97FFFh |
| | BA344 | 32 Kwords | A88000h-A8FFFFh |
| | BA343 | 32 Kwords | A80000h-A87FFFh |
| | BA342 | 32 Kwords | A78000h-A7FFFFh |
| | BA341 | 32 Kwords | A70000h-A77FFFh |
| | BA340 | 32 Kwords | A68000h-A6FFFFh |
| | BA339 | 32 Kwords | A60000h-A67FFFh |
| | BA338 | 32 Kwords | A58000h-A5FFFFh |
| | BA337 | 32 Kwords | A50000h-A57FFFh |
| | BA336 | 32 Kwords | A48000h-A4FFFFh |
| | BA335 | 32 Kwords | A40000h-A47FFFh |
| | BA334 | 32 Kwords | A38000h-A3FFFFh |
| | BA333 | 32 Kwords | A30000h-A37FFFh |
| | BA332 | 32 Kwords | A28000h-A2FFFFh |
| | BA331 | 32 Kwords | A20000h-A27FFFh |
| | BA330 | 32 Kwords | A18000h-A1FFFFh |
| | BA329 | 32 Kwords | A10000h-A17FFFh |
| | BA328 | 32 Kwords | A08000h-A0FFFFh |
| | BA327 | 32 Kwords | A00000h-A07FFFh |
| Bank 9 | BA326 | 32 Kwords | 9F8000h-9FFFFFh |
| | BA325 | 32 Kwords | 9F0000h-9F7FFFh |
| | BA324 | 32 Kwords | 9E8000h-9EFFFFh |
| | BA323 | 32 Kwords | 9E0000h-9E7FFFh |
| | BA322 | 32 Kwords | 9D8000h-9DFFFFh |
| | BA321 | 32 Kwords | 9D0000h-9D7FFFh |
| | BA320 | 32 Kwords | 9C8000h-9CFFFFh |
| | BA319 | 32 Kwords | 9C0000h-9C7FFFh |
| | BA318 | 32 Kwords | 9B8000h-9BFFFFh |
| | BA317 | 32 Kwords | 9B0000h-9B7FFFh |
| | BA316 | 32 Kwords | 9A8000h-9AFFFFh |
| | BA315 | 32 Kwords | 9A0000h-9A7FFFh |
| | BA314 | 32 Kwords | 998000h-99FFFFh |
| | BA313 | 32 Kwords | 990000h-997FFFh |
| | BA312 | 32 Kwords | 988000h-98FFFFh |
| | BA311 | 32 Kwords | 980000h-987FFFh |
| | BA310 | 32 Kwords | 978000h-97FFFFh |
| | BA309 | 32 Kwords | 970000h-977FFFh |
| | BA308 | 32 Kwords | 968000h-96FFFFh |
| | BA307 | 32 Kwords | 960000h-967FFFh |
| | BA306 | 32 Kwords | 958000h-95FFFFh |
| | BA305 | 32 Kwords | 950000h-957FFFh |
| | BA304 | 32 Kwords | 948000h-94FFFFh |
| | BA303 | 32 Kwords | 940000h-947FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 9 | BA302 | 32 Kwords | 938000h-93FFFFh |
| | BA301 | 32 Kwords | 930000h-937FFFh |
| | BA300 | 32 Kwords | 928000h-92FFFFh |
| | BA299 | 32 Kwords | 920000h-927FFFh |
| | BA298 | 32 Kwords | 918000h-91FFFFh |
| | BA297 | 32 Kwords | 910000h-917FFFh |
| | BA296 | 32 Kwords | 908000h-90FFFFh |
| | BA295 | 32 Kwords | 900000h-907FFFh |
| Bank 8 | BA294 | 32 Kwords | 8F8000h-8FFFFFh |
| | BA293 | 32 Kwords | 8F0000h-8F7FFFh |
| | BA292 | 32 Kwords | 8E8000h-8EFFFFh |
| | BA291 | 32 Kwords | 8E0000h-8E7FFFh |
| | BA290 | 32 Kwords | 8D8000h-8DFFFFh |
| | BA289 | 32 Kwords | 8D0000h-8D7FFFh |
| | BA288 | 32 Kwords | 8C8000h-8CFFFFh |
| | BA287 | 32 Kwords | 8C0000h-8C7FFFh |
| | BA286 | 32 Kwords | 8B8000h-8BFFFFh |
| | BA285 | 32 Kwords | 8B0000h-8B7FFFh |
| | BA284 | 32 Kwords | 8A8000h-8AFFFFh |
| | BA283 | 32 Kwords | 8A0000h-8A7FFFh |
| | BA282 | 32 Kwords | 898000h-89FFFFh |
| | BA281 | 32 Kwords | 890000h-897FFFh |
| | BA280 | 32 Kwords | 888000h-88FFFFh |
| | BA279 | 32 Kwords | 880000h-887FFFh |
| | BA278 | 32 Kwords | 878000h-87FFFFh |
| | BA277 | 32 Kwords | 870000h-877FFFh |
| | BA276 | 32 Kwords | 868000h-86FFFFh |
| | BA275 | 32 Kwords | 860000h-867FFFh |
| | BA274 | 32 Kwords | 858000h-85FFFFh |
| | BA273 | 32 Kwords | 850000h-857FFFh |
| | BA272 | 32 Kwords | 848000h-84FFFFh |
| | BA271 | 32 Kwords | 840000h-847FFFh |
| | BA270 | 32 Kwords | 838000h-83FFFFh |
| | BA269 | 32 Kwords | 830000h-837FFFh |
| | BA268 | 32 Kwords | 828000h-82FFFFh |
| | BA267 | 32 Kwords | 820000h-827FFFh |
| | BA266 | 32 Kwords | 818000h-81FFFFh |
| | BA265 | 32 Kwords | 810000h-817FFFh |
| | BA264 | 32 Kwords | 808000h-80FFFFh |
| | BA263 | 32 Kwords | 800000h-807FFFh |

**Table 3-1. Bottom Boot Boot Block Address Table(K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 7 | BA262 | 32 Kwords | 7F8000h-7FFFFFh |
| | BA261 | 32 Kwords | 7F0000h-7F7FFFh |
| | BA260 | 32 Kwords | 7E8000h-7EFFFFh |
| | BA259 | 32 Kwords | 7E0000h-7E7FFFh |
| | BA258 | 32 Kwords | 7D8000h-7DFFFFh |
| | BA257 | 32 Kwords | 7D0000h-7D7FFFh |
| | BA256 | 32 Kwords | 7C8000h-7CFFFFh |
| | BA255 | 32 Kwords | 7C0000h-7C7FFFh |
| | BA254 | 32 Kwords | 7B8000h-7BFFFFh |
| | BA253 | 32 Kwords | 7B0000h-7B7FFFh |
| | BA252 | 32 Kwords | 7A8000h-7AFFFFh |
| | BA251 | 32 Kwords | 7A0000h-7A7FFFh |
| | BA250 | 32 Kwords | 798000h-79FFFFh |
| | BA249 | 32 Kwords | 790000h-797FFFh |
| | BA248 | 32 Kwords | 788000h-78FFFFh |
| | BA247 | 32 Kwords | 780000h-787FFFh |
| | BA246 | 32 Kwords | 778000h-77FFFFh |
| | BA245 | 32 Kwords | 770000h-777FFFh |
| | BA244 | 32 Kwords | 768000h-76FFFFh |
| | BA243 | 32 Kwords | 760000h-767FFFh |
| | BA242 | 32 Kwords | 758000h-75FFFFh |
| | BA241 | 32 Kwords | 750000h-757FFFh |
| | BA240 | 32 Kwords | 748000h-74FFFFh |
| | BA239 | 32 Kwords | 740000h-747FFFh |
| | BA238 | 32 Kwords | 738000h-73FFFFh |
| | BA237 | 32 Kwords | 730000h-737FFFh |
| | BA236 | 32 Kwords | 728000h-72FFFFh |
| | BA235 | 32 Kwords | 720000h-727FFFh |
| | BA234 | 32 Kwords | 718000h-71FFFFh |
| | BA233 | 32 Kwords | 710000h-717FFFh |
| | BA232 | 32 Kwords | 708000h-70FFFFh |
| | BA231 | 32 kwords | 700000h-707FFFh |
| Bank 6 | BA230 | 32 Kwords | 6F8000h-6FFFFFh |
| | BA229 | 32 Kwords | 6F0000h-6F7FFFh |
| | BA228 | 32 Kwords | 6E8000h-6EFFFFh |
| | BA227 | 32 Kwords | 6E0000h-6E7FFFh |
| | BA226 | 32 Kwords | 6D8000h-6DFFFFh |
| | BA225 | 32 Kwords | 6D0000h-6D7FFFh |
| | BA224 | 32 Kwords | 6C8000h-6CFFFFh |
| | BA223 | 32 Kwords | 6C0000h-6C7FFFh |
| | BA222 | 32 Kwords | 6B8000h-6BFFFFh |
| | BA221 | 32 Kwords | 6B0000h-6B7FFFh |
| | BA220 | 32 Kwords | 6A8000h-6AFFFFh |
| | BA219 | 32 Kwords | 6A0000h-6A7FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 6 | BA218 | 32 Kwords | 698000h-69FFFFh |
| | BA217 | 32 Kwords | 690000h-697FFFh |
| | BA216 | 32 Kwords | 688000h-68FFFFh |
| | BA215 | 32 Kwords | 680000h-687FFFh |
| | BA214 | 32 Kwords | 678000h-67FFFFh |
| | BA213 | 32 Kwords | 670000h-677FFFh |
| | BA212 | 32 Kwords | 668000h-66FFFFh |
| | BA211 | 32 Kwords | 660000h-667FFFh |
| | BA210 | 32 Kwords | 658000h-65FFFFh |
| | BA209 | 32 Kwords | 650000h-657FFFh |
| | BA208 | 32 Kwords | 648000h-64FFFFh |
| | BA207 | 32 Kwords | 640000h-647FFFh |
| | BA206 | 32 Kwords | 638000h-63FFFFh |
| | BA205 | 32 Kwords | 630000h-637FFFh |
| | BA204 | 32 Kwords | 628000h-62FFFFh |
| | BA203 | 32 Kwords | 620000h-627FFFh |
| | BA202 | 32 Kwords | 618000h-61FFFFh |
| | BA201 | 32 Kwords | 610000h-617FFFh |
| | BA200 | 32 Kwords | 608000h-60FFFFh |
| | BA199 | 32 Kwords | 600000h-607FFFh |
| Bank 5 | BA198 | 32 Kwords | 5F8000h-5FFFFFh |
| | BA197 | 32 Kwords | 5F0000h-5F7FFFh |
| | BA196 | 32 Kwords | 5E8000h-5EFFFFh |
| | BA195 | 32 Kwords | 5E0000h-5E7FFFh |
| | BA194 | 32 Kwords | 5D8000h-5DFFFFh |
| | BA193 | 32 Kwords | 5D0000h-5D7FFFh |
| | BA192 | 32 Kwords | 5C8000h-5CFFFFh |
| | BA191 | 32 Kwords | 5C0000h-5C7FFFh |
| | BA190 | 32 Kwords | 5B8000h-5BFFFFh |
| | BA189 | 32 Kwords | 5B0000h-5B7FFFh |
| | BA188 | 32 Kwords | 5A8000h-5AFFFFh |
| | BA187 | 32 Kwords | 5A0000h-5A7FFFh |
| | BA186 | 32 Kwords | 598000h-59FFFFh |
| | BA185 | 32 Kwords | 590000h-597FFFh |
| | BA184 | 32 Kwords | 588000h-58FFFFh |
| | BA183 | 32 Kwords | 580000h-587FFFh |
| | BA182 | 32 Kwords | 578000h-57FFFFh |
| | BA181 | 32 Kwords | 570000h-577FFFh |
| | BA180 | 32 Kwords | 568000h-56FFFFh |
| | BA179 | 32 Kwords | 560000h-567FFFh |
| | BA178 | 32 Kwords | 558000h-55FFFFh |
| | BA177 | 32 Kwords | 550000h-557FFFh |
| | BA176 | 32 Kwords | 548000h-54FFFFh |
| | BA175 | 32 Kwords | 540000h-547FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 5 | BA174 | 32 Kwords | 538000h-53FFFFh |
| | BA173 | 32 Kwords | 530000h-537FFFh |
| | BA172 | 32 Kwords | 528000h-52FFFFh |
| | BA171 | 32 Kwords | 520000h-527FFFh |
| | BA170 | 32 Kwords | 518000h-51FFFFh |
| | BA169 | 32 Kwords | 510000h-517FFFh |
| | BA168 | 32 Kwords | 508000h-50FFFFh |
| | BA167 | 32 Kwords | 500000h-507FFFh |
| Bank 4 | BA166 | 32 Kwords | 4F8000h-4FFFFFh |
| | BA165 | 32 Kwords | 4F0000h-4F7FFFh |
| | BA164 | 32 Kwords | 4E8000h-4EFFFFh |
| | BA163 | 32 Kwords | 4E0000h-4E7FFFh |
| | BA162 | 32 Kwords | 4D8000h-4DFFFFh |
| | BA161 | 32 Kwords | 4D0000h-4D7FFFh |
| | BA160 | 32 Kwords | 4C8000h-4CFFFFh |
| | BA159 | 32 Kwords | 4C0000h-4C7FFFh |
| | BA158 | 32 Kwords | 4B8000h-4BFFFFh |
| | BA157 | 32 Kwords | 4B0000h-4B7FFFh |
| | BA156 | 32 Kwords | 4A8000h-4AFFFFh |
| | BA155 | 32 Kwords | 4A0000h-4A7FFFh |
| | BA154 | 32 Kwords | 498000h-49FFFFh |
| | BA153 | 32 Kwords | 490000h-497FFFh |
| | BA152 | 32 Kwords | 488000h-48FFFFh |
| | BA151 | 32 Kwords | 480000h-487FFFh |
| | BA150 | 32 Kwords | 478000h-47FFFFh |
| | BA149 | 32 Kwords | 470000h-477FFFh |
| | BA148 | 32 Kwords | 468000h-46FFFFh |
| | BA147 | 32 Kwords | 460000h-467FFFh |
| | BA146 | 32 Kwords | 458000h-45FFFFh |
| | BA145 | 32 Kwords | 450000h-457FFFh |
| | BA144 | 32 Kwords | 448000h-44FFFFh |
| | BA143 | 32 Kwords | 440000h-447FFFh |
| | BA142 | 32 Kwords | 438000h-43FFFFh |
| | BA141 | 32 Kwords | 430000h-437FFFh |
| | BA140 | 32 Kwords | 428000h-42FFFFh |
| | BA139 | 32 Kwords | 420000h-427FFFh |
| | BA138 | 32 Kwords | 418000h-41FFFFh |
| | BA137 | 32 Kwords | 410000h-417FFFh |
| | BA136 | 32 Kwords | 408000h-40FFFFh |
| | BA135 | 32 Kwords | 400000h-407FFFh |
| Bank 3 | BA134 | 32 Kwords | 3F8000h-3FFFFFh |
| | BA133 | 32 Kwords | 3F0000h-3F7FFFh |
| | BA132 | 32 Kwords | 3E8000h-3EFFFFh |
| | BA131 | 32 Kwords | 3E0000h-3E7FFFh |
| | BA130 | 32 Kwords | 3D8000h-3DFFFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 3 | BA129 | 32 Kwords | 3D0000h-3D7FFFh |
| | BA128 | 32 Kwords | 3C8000h-3CFFFFh |
| | BA127 | 32 Kwords | 3C0000h-3C7FFFh |
| | BA126 | 32 Kwords | 3B8000h-3BFFFFh |
| | BA125 | 32 Kwords | 3B0000h-3B7FFFh |
| | BA124 | 32 Kwords | 3A8000h-3AFFFFh |
| | BA123 | 32 Kwords | 3A0000h-3A7FFFh |
| | BA122 | 32 Kwords | 398000h-39FFFFh |
| | BA121 | 32 Kwords | 390000h-397FFFh |
| | BA120 | 32 Kwords | 388000h-38FFFFh |
| | BA119 | 32 Kwords | 380000h-387FFFh |
| | BA118 | 32 Kwords | 378000h-37FFFFh |
| | BA117 | 32 Kwords | 370000h-377FFFh |
| | BA116 | 32 Kwords | 368000h-36FFFFh |
| | BA115 | 32 Kwords | 360000h-367FFFh |
| | BA114 | 32 Kwords | 358000h-35FFFFh |
| | BA113 | 32 Kwords | 350000h-357FFFh |
| | BA112 | 32 Kwords | 348000h-34FFFFh |
| | BA111 | 32 Kwords | 340000h-347FFFh |
| | BA110 | 32 Kwords | 338000h-33FFFFh |
| | BA109 | 32 Kwords | 330000h-337FFFh |
| | BA108 | 32 Kwords | 328000h-32FFFFh |
| | BA107 | 32 Kwords | 320000h-327FFFh |
| | BA106 | 32 Kwords | 318000h-31FFFFh |
| | BA105 | 32 Kwords | 310000h-317FFFh |
| | BA104 | 32 Kwords | 308000h-30FFFFh |
| | BA103 | 32 Kwords | 300000h-307FFFh |
| Bank 2 | BA102 | 32 Kwords | 2F8000h-2FFFFFh |
| | BA101 | 32 Kwords | 2F0000h-2F7FFFh |
| | BA100 | 32 Kwords | 2E8000h-2EFFFFh |
| | BA99 | 32 Kwords | 2E0000h-2E7FFFh |
| | BA98 | 32 Kwords | 2D8000h-2DFFFFh |
| | BA97 | 32 Kwords | 2D0000h-2D7FFFh |
| | BA96 | 32 Kwords | 2C8000h-2CFFFFh |
| | BA95 | 32 Kwords | 2C0000h-2C7FFFh |
| | BA94 | 32 Kwords | 2B8000h-2BFFFFh |
| | BA93 | 32 Kwords | 2B0000h-2B7FFFh |
| | BA92 | 32 Kwords | 2A8000h-2AFFFFh |
| | BA91 | 32 Kwords | 2A0000h-2A7FFFh |
| | BA90 | 32 Kwords | 298000h-29FFFFh |
| | BA89 | 32 Kwords | 290000h-297FFFh |
| | BA88 | 32 Kwords | 288000h-28FFFFh |
| | BA87 | 32 Kwords | 280000h-287FFFh |
| | BA86 | 32 Kwords | 278000h-27FFFFh |
| | BA85 | 32 Kwords | 270000h-277FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 2 | BA84 | 32 Kwords | 268000h-26FFFFh |
| | BA83 | 32 Kwords | 260000h-267FFFh |
| | BA82 | 32 Kwords | 258000h-25FFFFh |
| | BA81 | 32 Kwords | 250000h-257FFFh |
| | BA80 | 32 Kwords | 248000h-24FFFFh |
| | BA79 | 32 Kwords | 240000h-247FFFh |
| | BA78 | 32 Kwords | 238000h-23FFFFh |
| | BA77 | 32 Kwords | 230000h-237FFFh |
| | BA76 | 32 Kwords | 228000h-22FFFFh |
| | BA75 | 32 Kwords | 220000h-227FFFh |
| | BA74 | 32 Kwords | 218000h-21FFFFh |
| | BA73 | 32 Kwords | 210000h-217FFFh |
| | BA72 | 32 Kwords | 208000h-20FFFFh |
| | BA71 | 32 Kwords | 200000h-207FFFh |
| Bank 1 | BA70 | 32 Kwords | 1F8000h-1FFFFFh |
| | BA69 | 32 Kwords | 1F0000h-1F7FFFh |
| | BA68 | 32 Kwords | 1E8000h-1EFFFFh |
| | BA67 | 32 Kwords | 1E0000h-1E7FFFh |
| | BA66 | 32 Kwords | 1D8000h-1DFFFFh |
| | BA65 | 32 Kwords | 1D0000h-1D7FFFh |
| | BA64 | 32 Kwords | 1C8000h-1CFFFFh |
| | BA63 | 32 Kwords | 1C0000h-1C7FFFh |
| | BA62 | 32 Kwords | 1B8000h-1BFFFFh |
| | BA61 | 32 Kwords | 1B0000h-1B7FFFh |
| | BA60 | 32 Kwords | 1A8000h-1AFFFFh |
| | BA59 | 32 Kwords | 1A0000h-1A7FFFh |
| | BA58 | 32 Kwords | 198000h-19FFFFh |
| | BA57 | 32 Kwords | 190000h-197FFFh |
| | BA56 | 32 Kwords | 188000h-18FFFFh |
| | BA55 | 32 Kwords | 180000h-187FFFh |
| | BA54 | 32 Kwords | 178000h-17FFFFh |
| | BA53 | 32 Kwords | 170000h-177FFFh |
| | BA52 | 32 Kwords | 168000h-16FFFFh |
| | BA51 | 32 Kwords | 160000h-167FFFh |
| | BA50 | 32 Kwords | 158000h-15FFFFh |
| | BA49 | 32 Kwords | 150000h-157FFFh |
| | BA48 | 32 Kwords | 148000h-14FFFFh |
| | BA47 | 32 Kwords | 140000h-147FFFh |
| | BA46 | 32 Kwords | 138000h-13FFFFh |
| | BA45 | 32 Kwords | 130000h-137FFFh |
| | BA44 | 32 Kwords | 128000h-12FFFFh |
| | BA43 | 32 Kwords | 120000h-127FFFh |
| | BA42 | 32 Kwords | 118000h-11FFFFh |
| | BA41 | 32 Kwords | 110000h-117FFFh |
| | BA40 | 32 Kwords | 108000h-10FFFFh |
| | BA39 | 32 Kwords | 100000h-107FFFh |

**Table 3-1. Bottom Boot Block Address Table (K8A5615EBA)**

| Bank | Block | Block Size | (x16) Address Range |
|---|---|---|---|
| Bank 0 | BA38 | 32 Kwords | 0F8000h-0FFFFFh |
| | BA37 | 32 Kwords | 0F0000h-0F7FFFh |
| | BA36 | 32 Kwords | 0E8000h-0EFFFFh |
| | BA35 | 32 Kwords | 0E0000h-0E7FFFh |
| | BA34 | 32 Kwords | 0D8000h-0DFFFFh |
| | BA33 | 32 Kwords | 0D0000h-0D7FFFh |
| | BA32 | 32 Kwords | 0C8000h-0CFFFFh |
| | BA31 | 32 Kwords | 0C0000h-0C7FFFh |
| | BA30 | 32 Kwords | 0B8000h-0BFFFFh |
| | BA29 | 32 Kwords | 0B0000h-0B7FFFh |
| | BA28 | 32 Kwords | 0A8000h-0AFFFFh |
| | BA27 | 32 Kwords | 0A0000h-0A7FFFh |
| | BA26 | 32 Kwords | 098000h-09FFFFh |
| | BA25 | 32 Kwords | 090000h-097FFFh |
| | BA24 | 32 Kwords | 088000h-08FFFFh |
| | BA23 | 32 Kwords | 080000h-087FFFh |
| | BA22 | 32 Kwords | 078000h-07FFFFh |
| | BA21 | 32 Kwords | 070000h-077FFFh |
| | BA20 | 32 Kwords | 068000h-06FFFFh |
| | BA19 | 32 Kwords | 060000h-067FFFh |
| | BA18 | 32 Kwords | 058000h-05FFFFh |
| | BA17 | 32 Kwords | 050000h-057FFFh |
| | BA16 | 32 Kwords | 048000h-04FFFFh |
| | BA15 | 32 Kwords | 040000h-047FFFh |
| | BA14 | 32 Kwords | 038000h-03FFFFh |
| | BA13 | 32 Kwords | 030000h-037FFFh |
| | BA12 | 32 Kwords | 028000h-02FFFFh |
| | BA11 | 32 Kwords | 020000h-027FFFh |
| | BA10 | 32 Kwords | 018000h-01FFFFh |
| | BA9 | 32 Kwords | 010000h-017FFFh |
| | BA8 | 32 Kwords | 008000h-00FFFFh |
| | BA7 | 4 Kwords | 007000h-007FFFh |
| | BA6 | 4 Kwords | 006000h-006FFFh |
| | BA5 | 4 Kwords | 005000h-005FFFh |
| | BA4 | 4 Kwords | 004000h-004FFFh |
| | BA3 | 4 Kwords | 003000h-003FFFh |
| | BA2 | 4 Kwords | 002000h-002FFFh |
| | BA1 | 4 Kwords | 001000h-001FFFh |
| | BA0 | 4 Kwords | 000000h-000FFFh |

**Table 3-1-2. Bottom Boot Block OTP Block Addresses**

| OTP | Block Address A23 ~ A8 | Block Size | (x16) Address Range |
|---|---|---|---|
| | 0000h | 128words | 000000h-00007Fh |

**After entering OTP block, any issued addresses should be in the range of OTP block address**

## PRODUCT INTRODUCTION

The K8A5615E is a 256Mbit (268,435,456 bits) NOR-type Burst Flash memory. The device features 1.8V single voltage power supply operating within the range of 1.7V to 1.95V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adopts a block memory architecture that divides its memory array into 519 blocks (32-Kword x 511 , 4-Kword x 8, ). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 519 memory blocks can be hardware protected. Regarding read access time, at 54MHz, the K8A5615E provides a burst access of 14.5ns with initial access times of 88.5ns at 30pF. At 66MHz, the K8A5615E provides a burst access of 11ns with initial access times of 70ns at 30pF. The command set of K8A5615E is compatible with standard Flash devices. The device uses Chip Enable ($\overline{CE}$), Write Enable ($\overline{WE}$), Address Valid($\overline{AVD}$) and Output Enable ($\overline{OE}$) to control asynchronous read and write operation. For burst operations, the device additionally requires Ready (RDY) and Clock (CLK). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8A5615E is implemented with Internal Program/Erase Routines to execute the program/erase operations. The Internal Program/Erase Routines are invoked by program/erase command sequences. The Internal Program Routine automatically programs and verifies data at specified addresses. The Internal Erase Routine automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8A5615E has means to indicate the status of completion of program/erase operations. The status can be indicated via Data polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The device requires only 30mA as burst and asynchronous mode read current and 15 mA for program/erase operations.

**Table 4. Device Bus Operations**

| Operation | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0-23 | DQ0-15 | $\overline{RESET}$ | CLK | $\overline{AVD}$ |
|---|---|---|---|---|---|---|---|---|
| Asynchronous Read Operation | L | L | H | Add In | I/O | H | L | L |
| Write | L | H |  | Add In | I/O | H | L | X |
| Standby | H | X | X | X | High-Z | H | X | X |
| Hardware Reset | X | X | X | X | High-Z | L | X | X |
| Load Initial Burst Address | L | H | H | Add In | X | H |  |  |
| Burst Read Operation | L | L | H | X | Burst $D_{OUT}$ | H |  | H |
| Terminate Burst Read Cycle | H | X | X | X | High-Z | H | X | X |
| Terminate Burst Read Cycle via $\overline{RESET}$ | X | X | X | X | High-Z | L | X | X |
| Terminate Current Burst Read Cycle and Start New Burst Read Cycle | L | H | H | Add In | I/O | H |  |  |

Note : L=$V_{IL}$ (Low), H=$V_{IH}$ (High), X=Don't Care.

## COMMAND DEFINITIONS

The K8A5615E operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5.

**Table 5. Command Sequences**

| Command Definitions | | Cycle | 1st Cycle | 2nd Cycle | 3rd Cycle | 4th Cycle | 5th Cycle | 6th Cycle |
|---|---|---|---|---|---|---|---|---|
| Asynchronous Read | Add | 1 | RA | | | | | |
| | Data | | RD | | | | | |
| Reset(Note 5) | Add | 1 | XXXH | | | | | |
| | Data | | F0H | | | | | |
| Autoselect Manufacturer ID(Note 6) | Add | 4 | 555H | 2AAH | (DA)555H | (DA)X00H | | |
| | Data | | AAH | 55H | 90H | ECH | | |
| Autoselect Device ID(Note 6) | Add | 4 | 555H | 2AAH | (DA)555H | (DA)X01H | | |
| | Data | | AAH | 55H | 90H | Note6 | | |
| Autoselect Block Protection Verify(Note 7) | Add | 4 | 555H | 2AAH | (BA)555H | (BA)X02H | | |
| | Data | | AAH | 55H | 90H | 00H/01H | | |
| Autoselect Handshaking(Note 6, 8) | Add | 4 | 555H | 2AAH | (DA)555H | (DA)X03H | | |
| | Data | | AAH | 55H | 90H | 0H/1H | | |
| Program | Add | 4 | 555H | 2AAH | 555H | PA | | |
| | Data | | AAH | 55H | A0H | PD | | |
| Unlock Bypass | Add | 3 | 555H | 2AAH | 555H | | | |
| | Data | | AAH | 55H | 20H | | | |
| Unlock Bypass Program(Note 9) | Add | 2 | XXX | PA | | | | |
| | Data | | A0H | PD | | | | |
| Unlock Bypass Block Erase(Note 9) | Add | 2 | XXX | BA | | | | |
| | Data | | 80H | 30H | | | | |
| Unlock Bypass Chip Erase(Note 9) | Add | 2 | XXXH | XXXH | | | | |
| | Data | | 80H | 10H | | | | |
| Unlock Bypass Reset | Add | 2 | XXXH | XXXH | | | | |
| | Data | | 90H | 00H | | | | |
| Quadruple word Accelerated Program(Note 10) | Add | 5 | XXX | PA1 | PA2 | PA3 | PA4 | |
| | Data | | A5H | PD1 | PD2 | PD3 | PD4 | |
| Chip Erase | Add | 6 | 555H | 2AAH | 555H | 555H | 2AAH | 555H |
| | Data | | AAH | 55H | 80H | AAH | 55H | 10H |
| Block Erase | Add | 6 | 555H | 2AAH | 555H | 555H | 2AAH | BA |
| | Data | | AAH | 55H | 80H | AAH | 55H | 30H |
| Erase Suspend (Note 11) | Add | 1 | (DA)XXXH | | | | | |
| | Data | | B0H | | | | | |
| Erase Resume (Note 12) | Add | 1 | (DA)XXXH | | | | | |
| | Data | | 30H | | | | | |
| Program Suspend (Note13) | Add | 1 | (DA)XXXH | | | | | |
| | Data | | B0H | | | | | |
| Program Resume (Note12) | Add | 1 | (DA)XXXH | | | | | |
| | Data | | 30H | | | | | |

**Table 5. Command Sequences (Continued)**

| Command Definitions | | Cycle | 1st Cycle | 2nd Cycle | 3rd Cycle | 4th Cycle | 5th Cycle | 6th Cycle |
|---|---|---|---|---|---|---|---|---|
| Block Protection/Unprotection (Note 14) | Add | 3 | XXX | XXX | ABP | | | |
| | Data | | 60H | 60H | 60H | | | |
| CFI Query (Note 15) | Add | 1 | (DA)X55H | | | | | |
| | Data | | 98H | | | | | |
| Set Burst Mode Configuration Register (Note 16) | Add | 3 | 555H | 2AAH | (CR)555H | | | |
| | Data | | AAH | 55H | C0H | | | |
| Enter OTP Block Region | Addr | 3 | 555H | 2AAH | 555H | | | |
| | Data | | AAH | 55H | 70H | | | |
| Exit OTP Block Region | Addr | 4 | 555H | 2AAH | 555H | XXX | | |
| | Data | | AAH | 55H | 75H | 00H | | |

**Notes:**

1. RA : Read Address , PA : Program Address, RD : Read Data, PD : Program Data , BA : Block Address (A23 ~ A12)
   DA : Bank Address (A23 ~ A20) , ABP : Address of the block to be protected or unprotected, CR : Configuration Register Setting
2. The 4th cycle data of autoselect mode and RD are output data. The others are input data.
3. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD and Device ID.
4. Unless otherwise noted, address bits A23–A11 are don't cares.
5. The reset command is required to return to read mode.
   If a bank entered the autoselect mode during the erase suspend mode, writing the reset command returns that bank to the erase suspend mode.
   If a bank entered the autoselect mode during the program suspend mode, writing the reset command returns that bank to the program suspend mode.
   If DQ5 goes high during the program or erase operation, writing the reset command returns that bank to read mode or erase suspend mode if that bank was in erase suspend mode.
6. The 3rd and 4th cycle bank address of autoselect mode must be same.
   Device ID Data : "22FCH" for Top Boot Block Device, "22FDH" for Bottom Boot Block Device
7. 00H for an unprotected block and 01H for a protected block.
8. 0H for handshaking, 1H for non-handshaking
9. The unlock bypass command sequence is required prior to this command sequence.
10. Quadruple word accelerated program is invoked only at Vpp=$V_{ID}$ ,Vpp setup is required prior to this command sequence.
    PA1, PA2, PA3, PA4 have the same A23~A2 address.
11. The system may read and program in non-erasing blocks when in the erase suspend mode.
    The system may enter the autoselect mode when in the erase suspend mode.
    The erase suspend command is valid only during a block erase operation, and requires the bank address.
12. The erase/program resume command is valid only during the erase/program suspend mode, and requires the bank address.
13. This mode is used only to enable Data Read by suspending the Program operation.
14. Set block address(BA) as either A6 = $V_{IH}$, A1 = $V_{IH}$ and A0 = $V_{IL}$ for unprotected or A6 = $V_{IL}$, A1 = $V_{IH}$ and A0 = $V_{IL}$ for protected.
15. Command is valid when the device is in Read mode or Autoselect mode.
16. See "Set Burst Mode Congiguration Register" for details.

## DEVICE OPERATION

To write a command or command sequence (which includes programming data to the device and erasing blocks of memory), the system must drive CLK, $\overline{WE}$ and $\overline{CE}$ to $V_{IL}$ and $\overline{OE}$ to $V_{IH}$ when providing address or data. The device provide the unlock bypass mode to save its program time for program operation. Unlike the standard program command sequence which is comprised of four bus cycles, only two program cycles are required to program a word in the unlock bypass mode. One block, multiple blocks, or the entire device can be erased. Table 3 indicates the address space that each block occupies. The device's address space is divided into sixteen banks: Bank 0 contains the boot/parameter blocks, and the other banks(from Bank 1 to 15) consist of uniform blocks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "block address" is the address bits required to uniquely select a block. $I_{CC2}$ in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

### Read Mode

The device automatically enters to asynchronous read mode after device power-up. No commands are required to retrieve data in asynchronous mode. After completing an Internal Program/Erase Routine, each bank is ready to read array data. The reset command is required to return a bank to the read(or erase-suspend-read)mode if DQ5 goes high during an active program/erase operation, or if the bank is in the autoselect mode.

The synchronous(burst) mode will ***automatically*** be enabled on the first rising edge on the CLK input while $\overline{AVD}$ is held low. That means device enters burst read mode from asynchronous read mode to burst read mode using CLK and $\overline{AVD}$ signal. When the burst read is finished(or terminated), the device return to asynchronous read mode automatically.

#### Asynchronous Read Mode

For the asynchronous read mode a valid address should be asserted on A0-A23, while driving $\overline{AVD}$ and $\overline{CE}$ to $V_{IL}$. $\overline{WE}$ should remain at $V_{IH}$ . The data will appear on DQ0-DQ15. Since the memory array is divided into sixteen banks, each bank remains enabled for read access until the command register contents are altered.

Address access time ($t_{AA}$) is equal to the delay from valid addresses to valid output data. The chip enable access time($t_{CE}$) is the delay from the falling edge of $\overline{CE}$ to valid data at the outputs. The output enable access time($t_{OE}$) is the delay from the falling edge of $\overline{OE}$ to valid data at the output. To prevent the memory content from spurious altering during power transition, the initial state machine is set for reading array data upon device power-up, or after a hardware reset.

#### Synchronous (Burst) Read Mode

The device is capable of continuous linear burst operation and linear burst operation of a preset length. For the burst mode, the system should determine how many clock cycles are desired for the initial word($t_{IACC}$) of each burst access and what mode of burst operation is desired using "Burst Mode Configuration Register" command sequences. See "Set Burst Mode Configuration" for further details. The status data also can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation.

##### Continuous Linear Burst Read

The synchronous(burst) mode will *automatically* be enabled on the first rising edge on the CLK input while $\overline{AVD}$ is held low. Note that the device is enabled for asynchronous mode when it first powers up. The initial word is output $t_{IAA}$ after the rising edge of the first CLK cycle. Subsequent words are output $t_{BA}$ after the rising edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has internal address boundary that occurs every 16 words. When the device is crossing the first word boundary, additional clock cycles are needed before data appears for the next address. The number of addtional clock cycle can varies from zero to three cycles, and the exact number of additional clock cycle depends on the starting address of burst read.(Refer to Figure 13) The RDY output indicates this condition to the system by pulsing low. The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location until the system asserts $\overline{CE}$ high, $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address.(See Table 4.) The reset command does not terminate the burst read operation.

If the host system crosses the bank boundary while reading in burst mode, and the accessed bank is not programming or erasing, a additional clock cycles are needed as previously mentioned. If the host system crosses the bank boundary while the accessed bank is programming or erasing, that is busy bank, the synchronous read will be terminated.

**8-,16-Word Linear Burst Read**

As well as the Continuous Linear Burst Mode, there are two(8 & 16 word) linear wrap & no-wrap mode, in which a fixed number of words are read from consecutive addresses. In these modes, the addresses for burst read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode.(See Table. 6)

**Table 6. Burst Address Groups(Wrap mode only)**

| Burst Mode | Group Size | Group Address Ranges |
|---|---|---|
| 8 word | 8 words | 0-7h, 8-Fh, 10-17h, .... |
| 16 word | 16words | 0-Fh, 10-1Fh, 20-2Fh, .... |

As an example:

In wrap mode case, if the starting address in the 8-word mode is 2h, the address range to be read would be 0-7h, and the wrap burst sequence would be 2-3-4-5-6-7-0-1h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar manner, 16-word wrap mode begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group.

In no-wrap mode case, if the starting address in the 8-word mode is 2h, the no-wrap burst sequence would be 2-3-4-5-6-7-8-9h. The burst sequence begins with the starting address written to the device, and continue to the 8th address from starting address. In a similar manner, 16-word no-wrap mode begin their burst sequence on the starting address written to the device, and continue to the 16th address from starting address. Also, when the address cross the word boundary in no-wrap mode, same number of additional clock cycles as continuous linear mode is needed.

## Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after $\overline{AVD}$ is driven active for burst read mode. Upon power up, the number of total initial access cycles defaults to seven.

### Handshaking

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. To set the number of initial cycle for optimal burst mode, the host should use the programmable wait state configuration.(See "Set Burst Mode Configuration Register" for details.) The rising edge of RDY after $\overline{OE}$ goes low indicates the initial word of valid burst data. Using the autoselect command sequence the handshaking feature may be verified in the device.

## Set Burst Mode Configuration Register

The device uses a configuration register to set the various burst parameters : the number of initial cycles for burst and burst read mode. The burst mode configuration register must be set before the device enter burst mode.

The burst mode configuration register is loaded with a three-cycle command sequences. On the third cycle, the data should be C0h, address bits A11-A0 should be 555h, and address bits A18-A12 set the code to be latched. The device will power up or after a hardware reset with the default setting.

**Table 7. Burst Mode Configuration Register Table**

| Address Bit | Function | Settings(Binary) |
|---|---|---|
| A18 | RDY Active | 1 = RDY active one clock cycle before data<br>0 = RDY active with data(default) |
| A17 | Burst Read Mode | 000 = Continuous(default)<br>001 = 8-word linear with wrap<br>010 = 16-word linear with wrap<br>011 = 8-word linear with no-wrap<br>100 = 16-word linear with no-wrap<br>101 ~ 111 = Reserve |
| A16 | | |
| A15 | | |
| A14 | Programmable Wait State | 000 = Data is valid on the 4th active CLK edge after AVD transition to $V_{IH}$<br>001 = Data is valid on the 5th active CLK edge after AVD transition to $V_{IH}$<br>010 = Data is valid on the 6th active CLK edge after AVD transition to $V_{IH}$<br>011 = Data is valid on the 7th active CLK edge after AVD transition to $V_{IH}$ (default)<br>100 = Reserve<br>101 = Reserve<br>110 = Reserve<br>111 = Reserve |
| A13 | | |
| A12 | | |

### Programmable Wait State Configuration

This feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14-A12 determine the setting. (See Burst Mode Configuration Register Table)

The Programmable wait state setting instructs the device to set a particular number of clock cycles for the initial access in burst mode. Note that hardware reset will set the wait state to the default setting, that is 7 initial cycles.

### Burst Read Mode Setting

The device supports five different burst read modes : continuous linear mode, 8 and 16 word linear burst modes with wrap and 8 and 16 word linear burst modes with no-wrap.

### RDY Configuration

By default, the RDY pin will be high whenever there is valid data on the output. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determine this setting. Note that RDY always go high with valid data in case of word boundary crossing.

**Table 8. Burst Address Sequences**

| | Start Addr. | Burst Address Sequence(Decimal) | | |
|---|---|---|---|---|
| | | Continuous Burst | 8-word Burst | 16-word Burst |
| Wrap | 0 | 0-1-2-3-4-5-6... | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-....-13-14-15 |
| | 1 | 1-2-3-4-5-6-7... | 1-2-3-4-5-6-7-0 | 1-2-3-4-5-....-14-15-0 |
| | 2 | 2-3-4-5-6-7-8... | 2-3-4-5-6-7-0-1 | 2-3-4-5-6-....-15-0-1 |
| | . . | . . | . . | . . |
| No-wrap | 0 | 0-1-2-3-4-5-6... | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-....-13-14-15 |
| | 1 | 1-2-3-4-5-6-7... | 1-2-3-4-5-6-7-8 | 1-2-3-4-5-....-14-15-16 |
| | 2 | 2-3-4-5-6-7-8... | 2-3-4-5-6-7-8-9 | 2-3-4-5-6-....-15-16-17 |
| | . . | . . | . . | . . |

## Autoselect Mode

By writing the autoselect command sequences to the system, the device enters the autoselect mode. This mode can be read only by asynchronous read mode. The system can then read autoselect codes from the internal register(which is separate from the memory array). Standard asynchronous read cycle timings apply in this mode. The device offers the Autoselect mode to identify manufacturer and device type by reading a binary code. In addition, this mode allows the host system to verify the block protection or unprotection. Table 5 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is in the read mode, erase-suspend-read mode or program-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the device. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the address and the autoselect command. Note that the block address is needed for the verification of block protection. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. And the burst read should be prohibited during Autoselect Mode. To terminate the autoselect operation, write Reset command(F0H) into the command register.

**Table 9. Autoselct Mode Description**

| Description | Address | Read Data |
|---|---|---|
| Manufacturer ID | (DA) + 00H | ECH |
| Device ID | (DA) + 01H | 22FCH(Top Boot Block), 22FDH(Bottom Boot Block) |
| Block Protection/Unprotection | (BA) + 02H | 01H (protected), 00H (unprotected) |
| Handshaking | (DA) + 03H | 0H : handshaking, 1H : non-handshaking |

## Standby Mode

When the $\overline{CE}$ and $\overline{RESET}$ inputs are both held at $V_{CC} \pm 0.2V$ or the system is not reading or writing, the device enters Stand-by mode to minimize the power consumption. In this mode, the device outputs are placed in the high impedence state, independent of the $\overline{OE}$ input. When the device is in either of these standby modes, the device requires standard access time ($t_{CE}$ ) for read access before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. $I_{CC5}$ in the DC Characteristics table represents the standby current specification.

## Automatic Sleep Mode

The device features Automatic Sleep Mode to minimize the device power consumption during both asynchronous and burst mode. When addresses remain stable for $t_{AA}$+60ns, the device automatically enables this mode. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. In a sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time. Automatic sleep mode current is equal to standby mode current.

## Output Disable Mode

When the $\overline{OE}$ input is at $V_{IH}$ , output from the device is disabled. The outputs are placed in the high impedance state.

## Block Protection & Unprotection

To protect the block from accidental writes, the block protection/unprotection command sequence is used. On power up, all blocks in the device are protected. To unprotect a block, the system must write the block protection/unprotection command sequence. The first two cycles are written: addresses are don't care and data is 60h. Using the third cycle, the block address (ABP) and command (60h) is written, while specifying with addresses A6, A1 and A0 whether that block should be protected (A6 = $V_{IL}$, A1 = $V_{IH}$, A0 = $V_{IL}$) or unprotected (A6 = $V_{IH}$, A1 = $V_{IH}$, A0 = $V_{IL}$). After the third cycle, the system can continue to protect or unprotect additional cycles, or exit the sequence by writing F0h (reset command).

The device offers three types of data protection at the block level:

- The block protection/unprotection command sequence disables or re-enables both program and erase operations in any block.
- When $\overline{WP}$ is at $V_{IL}$, the two outermost blocks are protected.
- When $V_{PP}$ is at $V_{IL}$, all blocks are protected.

**Note that user never float the Vpp and $\overline{WP}$, that is, Vpp is always connected with $V_{IH}$, $V_{IL}$ or $V_{ID}$ and $\overline{WP}$ is $V_{IH}$ or $V_{IL}$.**

## Hardware Reset

The device features a hardware method of resetting the device by the $\overline{RESET}$ input. When the $\overline{RESET}$ pin is held low($V_{IL}$) for at least a period of tRP, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to asynchronous read mode. To ensure data integrity, the interrupted operation should be reinitiated once the device is ready to accept another command sequence. As previously noted, when $\overline{RESET}$ is held at $V_{SS} \pm 0.2V$, the device enters standby mode. The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program or Erase Routine, the device will be automatically reset to the asynchronous read mode; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory. If $\overline{RESET}$ is asserted during a program or erase operation, the device requires a time of tREADY (during Internal Routines) before the device is ready to read data again. If $\overline{RESET}$ is asserted when a program or erase operation is not executing, the reset operation is completed within a time of tREADY (not during Internal Routines). tRH is needed to read data after $\overline{RESET}$ returns to $V_{IH}$. Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and to Figure 6 for the timing diagram.

## Software Reset

The reset command provides that the bank is reseted to read mode, erase-suspend-read mode or program-suspend-read mode. The addresses are in Don't Care state. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. If the device begins erasure or programming, the reset command is ignored until the operation is completed. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. The reset command is valid between the sequence cycles in an autoselect command sequence. In an autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Also, if a bank entered the autoselect mode while in the Program Suspend mode, writing the reset command returns that bank to the program-suspend-read mode. If DQ5 goes high during a program or an erase operation, writing the reset command returns the banks to the read mode. (or erase-suspend-read mode if the bank was in Erase Suspend)

## Program

The K8A5615E can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings. During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

## Accelerated Program Operation

The device provides Single/Quadruple word accelerated program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When $V_{ID}$ is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. By removing $V_{ID}$ returns the device to normal operation mode.

**Note that Read while Accelerated Program and Program suspend mode are not guaranteed**

**Single word accelerated program operation**

The system would use two-cycle program sequence (One-cycle (XXX - A0H) is for single word program command, and Next one-cycle (PA - PD) is for program address and data ).

**Quadruple word accelerated program operation**

As well as Single word accelerated program, the system would use five-cycle program sequence (One-cycle (XXX - A5H) is for quadruple word program command, and four cycles are for program address and data).

- Only four words programming is possible
- Each program address must have the same A23~A2 address
- The device automatically generates adequate program pulses and ignores other command after program command
- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Read while Write mode is not guaranteed

**Requirements : Ambient temperature : $T_A$=25°C±5°C**

## Unlock Bypass

The K8A5615E provides the unlock bypass mode to save its operation time. This mode is possible for program, block erase and chip erase operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence or the assertion of $V_{ID}$ on $V_{PP}$ pin. Unlike the standard program/erase command sequence that contains four/six bus cycles, the unlock bypass program/erase command sequence needs only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

To enter the unlock bypass mode in hardware level, the $V_{ID}$ also can be used. By assertion $V_{ID}$ on the $V_{PP}$ pin, the device enters the unlock bypass mode. Also, the all blocks are temporarily unprotected when the device using the $V_{ID}$ for unlock bypass mode. To exit the unlock bypass mode, just remove the asserted $V_{ID}$ from the $V_{PP}$ pin.(Note that user never float the Vpp, that is, Vpp is always connected with $V_{IH}$, $V_{IL}$ or $V_{ID}$.).

## Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

## Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 5. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. Multiple blocks can be erased sequentially by writing the sixth bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. For the Multi-Block Erase, only sixth cycle(block address and 30H) is needed.(Similarly, only second cycle is needed in unlock bypass block erase.) An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command during Block Erase operation.

The device provides accelerated erase operations through the Vpp input. When $V_{ID}$ is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for erase. By removing $V_{ID}$ returns the device to normal operation mode.

## Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. Also, it is possible to protect or unprotect of the block that is not being erased in erase suspend mode. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50 us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running. When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20 us(recovery time) to suspend the erase operation. Therefore system must wait for 20us(recovery time) to read the data from the bank which include the block being erased. Otherwise, system can read the data immediately from a bank which don't include the block being erased without recovery time(max. 20us) after Erase Suspend command. And, after the maximum 20us recovery time, the device is availble for programming data in a block that is not being erased. But, when the Erase Suspend command is written during the block erase time window (50 us) , the device immediately terminates the block erase time window and suspends the erase operation. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state.

## Program Suspend / Resume

The device provides the Program Suspend/Resume mode. This mode is used to enable Data Read by suspending the Program operation. The device accepts a Program Suspend command in Program mode(including Program operations performed during Erase Suspend) but other commands are ignored. After input of the Program Suspend command, 2us is needed to enter the Program Suspend Read mode. Therefore system must wait for 2us(recovery time) to read the data from the bank which include the block being programmed. Othwewise, system can read the data immediately from a bank which don't include block being programmed without ecovery time(max. 2us) after Program Suspend command. Like an Erase Suspend mode, the device can be returned to Program mode by using a Program Resume command.

## Read While Write Operation

The device is capable of reading data from one bank while writing in the other banks. This is so called the Read While Write operation. An erase operation may also be suspended to read from or program to another location within the same bank(except the block being erased). The Read While Write operation is prohibited during the chip erase operation. Figure 12 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-write current specifications.

## OTP Block Region

The OTP Block feature provides a 256-byte Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. The customer-lockable OTP Block has the Protection Verify Bit (DQ0) set to a "0" for Unlocked state or a "1" for Locked state.

The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table8). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses normally and may check the Protection Verify Bit (DQ0) by using the "Autoselect Block Protection Verify" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

**Customer Lockable**

In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Note that the Accelerated programming and Unlock bypass functions are not available when programming the OTP Block. Locking operation to the OTP Block is started by writing the "Enter OTP Block" Command sequence, and then the "Block Protection" Command sqeunce (Table 8) with an OTP Block address. Hardware reset terminates Locking operation, and then makes exiting from OTP Block. The Locking operation has to be above 100us.

***The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.***

## Low $V_{CC}$ Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than $V_{LKO}$. If the Vcc < $V_{LKO}$ (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode.Subsequent writes will be ignored until the Vcc level is greater than $V_{LKO}$. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above $V_{LKO}$.

## Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$, $\overline{AVD}$ or $\overline{WE}$ do not initiate a write cycle.

## Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = $V_{IL}$ , $\overline{CE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

## Power-up Protection

To avoid initiation of a write cycle during $V_{CC}$ power-up, $\overline{RESET}$ low must be asserted during Power-up. After $\overline{RESET}$ goes high. the device is reset to the read mode.

## FLASH MEMORY STATUS FLAGS

The K8A5615E has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being executed internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins. This status read is supported in burst mode and asynchronous mode. The status data can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. That means status read is supported in synchronous mode. If status read is performed, the data provided in the burst read is identical to the data in the initial access. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3 and DQ2.

**Table 10. Hardware Sequence Flags**

| | Status | | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 |
|---|---|---|---|---|---|---|---|
| In Progress | Programming | | $\overline{DQ7}$ | Toggle | 0 | 0 | 1 |
| | Block Erase or Chip Erase | | 0 | Toggle | 0 | 1 | Toggle |
| | Erase Suspend Read | Erase Suspended Block | 1 | 1 | 0 | 0 | Toggle (Note 1) |
| | Erase Suspend Read | Non-Erase Suspended Block | Data | Data | Data | Data | Data |
| | Erase Suspend Program | Non-Erase Suspended Block | $\overline{DQ7}$ | Toggle | 0 | 0 | 1 |
| | Program Suspend Read | Program Suspended Block | DQ7 | 1 | 0 | 0 | Toggle (Note 1) |
| | Program Suspend Read | Non- program Suspended Block | Data | Data | Data | Data | Data |
| Exceeded Time Limits | Programming | | $\overline{DQ7}$ | Toggle | 1 | 0 | No Toggle |
| | Block Erase or Chip Erase | | 0 | Toggle | 1 | 1 | (Note 2) |
| | Erase Suspend Program | | $\overline{DQ7}$ | Toggle | 1 | 0 | No Toggle |

**Notes :**
1. DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

## DQ7 : $\overline{Data}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

### DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

### DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

### DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

### DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode.

### RDY: Ready

Normally the RDY signal is used to indicate if new burst data is available at the rising edge of the clock cycle or not. If RDY is low state, data is not valid at expected time, and if high state, data is valid. Note that, if $\overline{CE}$ is low and $\overline{OE}$ is high, the RDY is high state.

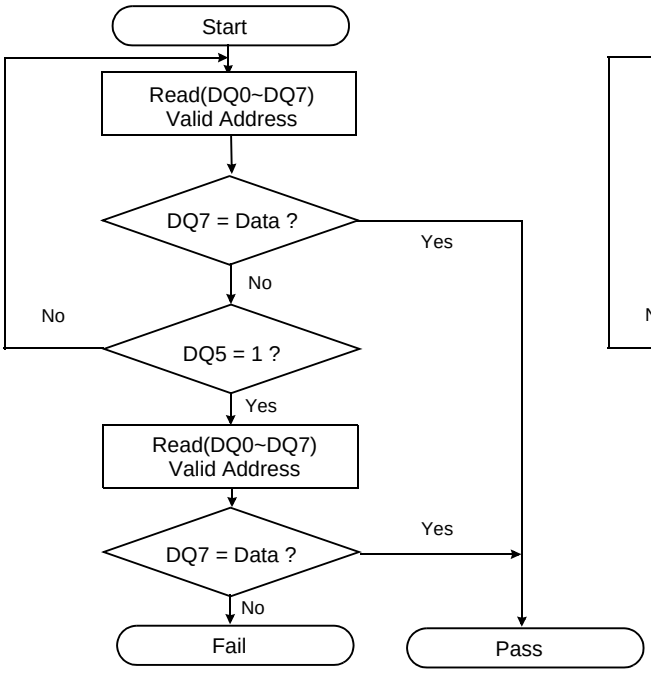



**Figure 1. Data Polling Algorithms**

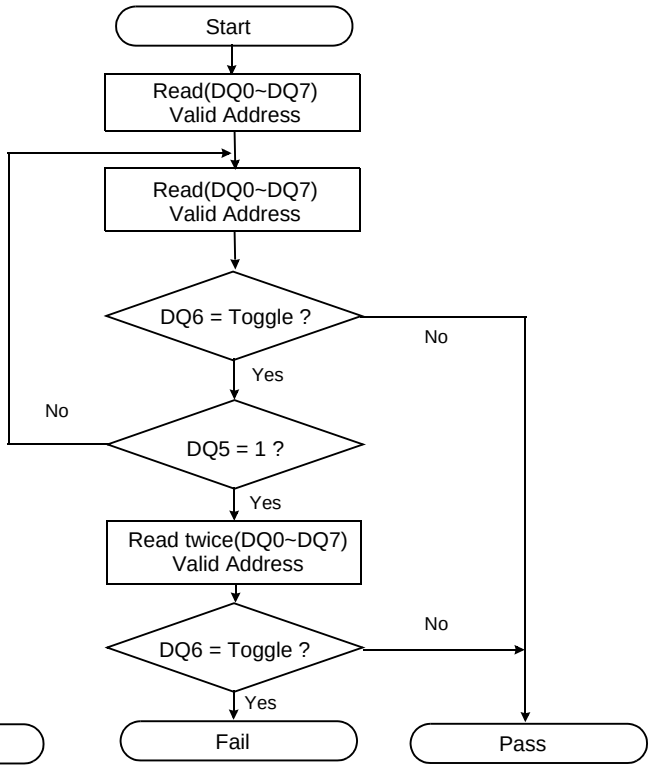



**Figure 2. Toggle Bit Algorithms**

## Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H , the device enters the CFI mode. And then if the system writes the address shown in Table 11, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

**Table 11. Common Flash Memory Interface Code**

| Description | Addresses (Word Mode) | Data |
|---|---|---|
| Query Unique ASCII string "QRY" | 10H<br>11H<br>12H | 0051H<br>0052H<br>0059H |
| Primary OEM Command Set | 13H<br>14H | 0002H<br>0000H |
| Address for Primary Extended Table | 15H<br>16H | 0040H<br>0000H |
| Alternate OEM Command Set (00h = none exists) | 17H<br>18H | 0000H<br>0000H |
| Address for Alternate OEM Extended Table (00h = none exists) | 19H<br>1AH | 0000H<br>0000H |
| Vcc Min. (write/erase)<br>D7-D4: volt, D3-D0: 100 millivolt | 1BH | 0017H |
| Vcc Max. (write/erase)<br>D7-D4: volt, D3-D0: 100 millivolt | 1CH | 0019H |
| Vpp(Acceleration Program) Supply Minimum<br>00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV | 1DH | 0085H |
| Vpp(Acceleration Program) Supply Maximum<br>00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV | 1EH | 0095H |
| Typical timeout per single word write $2^N$ us | 1FH | 0004H |
| Typical timeout for Min. size buffer write $2^N$ us(00H = not supported) | 20H | 0000H |
| Typical timeout per individual block erase $2^N$ ms | 21H | 000AH |
| Typical timeout for full chip erase $2^N$ ms(00H = not supported) | 22H | 0013H |
| Max. timeout for word write $2^N$ times typical | 23H | 0005H |
| Max. timeout for buffer write $2^N$ times typical | 24H | 0000H |
| Max. timeout per individual block erase $2^N$ times typical | 25H | 0004H |
| Max. timeout for full chip erase $2^N$ times typical(00H = not supported) | 26H | 0000H |
| Device Size = $2^N$ byte | 27H | 0019H |
| Flash Device Interface description | 28H<br>29H | 0000H<br>0000H |
| Max. number of byte in multi-byte write = $2^N$ | 2AH<br>2BH | 0000H<br>0000H |
| Number of Erase Block Regions within device | 2CH | 0002H |

**Table 11. Common Flash Memory Interface Code (Continued)**

| Description | Addresses (Word Mode) | Data |
|---|---|---|
| Erase Block Region 1 Information<br>Bits 0~15: y+1=block number<br>Bits 16~31: block size= z x 256bytes | 2DH<br>2EH<br>2FH<br>30H | 0007H<br>0000H<br>0020H<br>0000H |
| Erase Block Region 2 Information | 31H<br>32H<br>33H<br>34H | 00FEH<br>0001H<br>0000H<br>0001H |
| Erase Block Region 3 Information | 35H<br>36H<br>37H<br>38H | 0000H<br>0000H<br>0000H<br>0000H |
| Erase Block Region 4 Information | 39H<br>3AH<br>3BH<br>3CH | 0000H<br>0000H<br>0000H<br>0000H |
| Query-unique ASCII string "PRI" | 40H<br>41H<br>42H | 0050H<br>0052H<br>0049H |
| Major version number, ASCII | 43H | 0031H |
| Minor version number, ASCII | 44H | 0030H |
| Address Sensitive Unlock(Bits 1-0)<br>0 = Required, 1= Not Required<br>Silcon Revision Number(Bits 7-2) | 45H | 0000H |
| Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write | 46H | 0002H |
| Block Protect<br>00 = Not Supported, 01 = Supported | 47H | 0001H |
| Block Temporary Unprotect 00 = Not Supported, 01 = Supported | 48H | 0000H |
| Block Protect/Unprotect scheme 00 = Not Supported, 01 = Supported | 49H | 0001H |
| Simultaneous Operation<br>00 = Not Supported, 01 = Supported | 4AH | 0001H |
| Burst Mode Type 00 = Not Supported, 01 = Supported | 4BH | 0001H |
| Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page | 4CH | 0000H |
| Max. Operating Clock Frequency (MHz ) | 4EH | 0042H |
| RWW(Read While Write) Functionality Restriction (00H = non exists , 01H = exists) | 4FH | 0000H |
| Handshaking<br>00 = Not Supported at both mode, 01 = Supported at Sync. Mode<br>10 = Supported at Async. Mode, 11 = Supported at both Mode | 50H | 0001H |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{CC}$ | $V_{CC}$ | -0.5 to +2.5 | V |
| | $V_{PP}$ | $V_{IN}$ | -0.5 to +9.5 | |
| | All Other Pins | | -0.5 to +2.5 | |
| Temperature Under Bias | Commercial | $T_{bias}$ | -10 to +125 | °C |
| | Extended | | -25 to +125 | |
| Storage Temperature | | $T_{stg}$ | -65 to +150 | °C |
| Short Circuit Output Current | | $I_{OS}$ | 5 | mA |
| Operating Temperature | | $T_A$ (Commercial Temp.) | 0 to +70 | °C |
| | | $T_A$ (Extended Temp.) | -25 to + 85 | °C |

**Notes** :

1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -1.5V for periods <20ns.
   Maximum DC voltage is $V_{CC}$+0.6V on input / output pins which, during transitions, may overshoot to $V_{CC}$+1.5V for periods <20ns.
2. Minimum DC input voltage is -0.5V on $V_{PP}$ . During transitions, this level may fall to -1.5V for periods <20ns.
   Maximum DC input voltage is +9.5V on $V_{PP}$ which, during transitions, may overshoot to +11.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS ( Voltage reference to GND )

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 1.7 | 1.8 | 1.95 | V |
| Supply Voltage | $V_{SS}$ | 0 | 0 | 0 | V |

## DC CHARACTERISTICS

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=$V_{SS}$ to $V_{CC}$, $V_{CC}$=$V_{CCmax}$ | | - 1.0 | - | + 1.0 | µA |
| VPP Leakage Current | $I_{LIP}$ | $V_{CC}$=$V_{CCmax}$ , $V_{PP}$=9.5V | | - | - | 35 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$=$V_{SS}$ to $V_{CC}$, $V_{CC}$=$V_{CCmax}$, $\overline{OE}$=$V_{IH}$ | | - 1.0 | - | + 1.0 | µA |
| Active Burst Read Current | $I_{CCB1}$ | $\overline{CE}$=$V_{IL}$, $\overline{OE}$=$V_{IH}$ | | - | 30 | 45 | mA |
| Active Asynchronous Read Current | $I_{CC1}$ | $\overline{CE}$=$V_{IL}$, $\overline{OE}$=$V_{IH}$ | 10MHz | - | 30 | 45 | mA |
| | | | 1MHz | - | 3 | 5 | mA |
| Active Write Current (Note 2) | $I_{CC2}$ | $\overline{CE}$=$V_{IL}$, $\overline{OE}$=$V_{IH}$, $\overline{WE}$=$V_{IL}$, $V_{PP}$=$V_{IH}$ | | - | 15 | 30 | mA |
| Read While Write Current | $I_{CC3}$ | $\overline{CE}$=$V_{IL}$, $\overline{OE}$=$V_{IH}$ | | - | 40 | 70 | mA |
| Accelerated Program Current | $I_{CC4}$ | $\overline{CE}$=$V_{IL}$, $\overline{OE}$=$V_{IH}$ , $V_{PP}$=9.5V | | - | 15 | 30 | mA |
| Standby Current | $I_{CC5}$ | $\overline{CE}$= $\overline{RESET}$=$V_{CC}$ ± 0.2V | | - | 25 | 70 | µA |
| Standby Current During Reset | $I_{CC6}$ | $\overline{RESET}$ = $V_{SS}$ ± 0.2V | | - | 25 | 70 | µA |
| Automatic Sleep Mode(Note 3) | $I_{CC7}$ | $\overline{CE}$=$V_{SS}$ ± 0.2V, Other Pins=$V_{IL}$ or $V_{IH}$<br>$V_{IL}$ = $V_{SS}$ ± 0.2V, $V_{IH}$ = $V_{CC}$ ± 0.2V | | - | 25 | 70 | µA |
| Input Low Voltage | $V_{IL}$ | | | -0.5 | - | 0.4 | V |
| Input High Voltage | $V_{IH}$ | | | $V_{CC}$-0.4 | - | $V_{CC}$+0.4 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100 µA , $V_{CC}$=$V_{CCmin}$ | | - | - | 0.1 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -100 µA , $V_{CC}$=$V_{CCmin}$ | | $V_{CC}$-0.1 | - | - | V |
| Voltage for Accelerated Program | $V_{ID}$ | | | 8.5 | 9.0 | 9.5 | V |
| Low $V_{CC}$ Lock-out Voltage | $V_{LKO}$ | | | 1.0 | - | 1.3 | V |

**Notes:**

1. Maximum $I_{CC}$ specifications are tested with $V_{CC}$ = $V_{CCmax}$.
2. $I_{CC}$ active while Internal Erase or Internal Program is in progress.
3. Device enters automatic sleep mode when addresses are stable for $t_{AA}$ + 60ns.

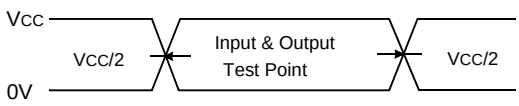
## CAPACITANCE($T_A$ = 25 °C, $V_{CC}$ = 1.8V, f = 1.0MHz)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 10 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | - | 10 | pF |
| Control Pin Capacitance | $C_{IN2}$ | $V_{IN}$=0V | - | 10 | pF |

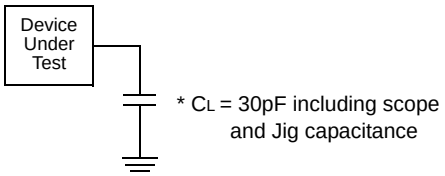
**Note** : Capacitance is periodically sampled and not 100% tested.

## AC TEST CONDITION

| Parameter | Value |
|---|---|
| Input Pulse Levels | 0V to $V_{CC}$ |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | $V_{CC}$/2 |
| Output Load | $C_L$ = 30pF |




**Input Pulse and Test Point**




**Output Load**

## AC CHARACTERISTICS

### Synchronous/Burst Read

| Parameter | Symbol | 7B (54 MHz) | | 7C (66 MHz) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Initial Access Time | $t_{IAA}$ | - | 88.5 | - | 70 | ns |
| Burst Access Time Valid Clock to Output Delay | $t_{BA}$ | - | 14.5 | - | 11 | ns |
| $\overline{AVD}$ Setup Time to CLK | $t_{AVDS}$ | 5 | - | 5 | - | ns |
| $\overline{AVD}$ Hold Time from CLK | $t_{AVDH}$ | 7 | - | 6 | - | ns |
| Address Setup Time to CLK | $t_{ACS}$ | 5 | - | 5 | - | ns |
| Address Hold Time from CLK | $t_{ACH}$ | 7 | - | 6 | - | ns |
| Data Hold Time from Next Clock Cycle | $t_{BDH}$ | 4 | - | 4 | - | ns |
| Output Enable to Data | $t_{OE}$ | - | 20 | - | 20 | ns |
| Output Enable to RDY valid | $t_{OER}$ | - | 14.5 | - | 11 | ns |
| $\overline{CE}$ Disable to High Z | $t_{CEZ}$ | - | 20 | - | 20 | ns |
| $\overline{OE}$ Disable to High Z | $t_{OEZ}$ | - | 15 | - | 15 | ns |
| $\overline{CE}$ Setup Time to CLK | $t_{CES}$ | 7 | - | 6 | - | ns |
| CLK to RDY Setup Time | $t_{RDYA}$ | - | 14.5 | - | 11 | ns |
| RDY Setup Time to CLK | $t_{RDYS}$ | 4 | - | 4 | - | ns |
| CLK High or Low Time | $t_{CLKH/L}$ | 4.5 | - | 3.5 | - | ns |
| CLK Fall or Rise Time | $t_{CLKHCL}$ | - | 3 | - | 3 | ns |

## SWITCHING WAVEFORMS

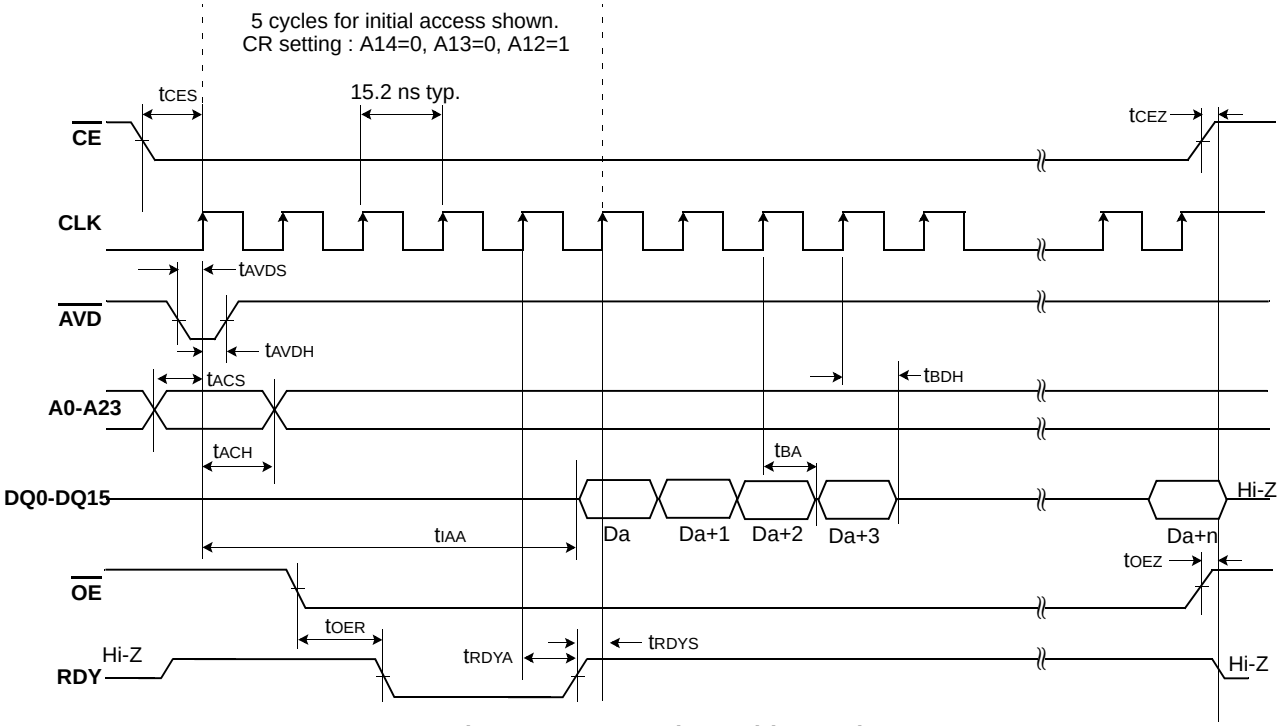



**Figure 3. Burst Mode Read (66 MHz)**

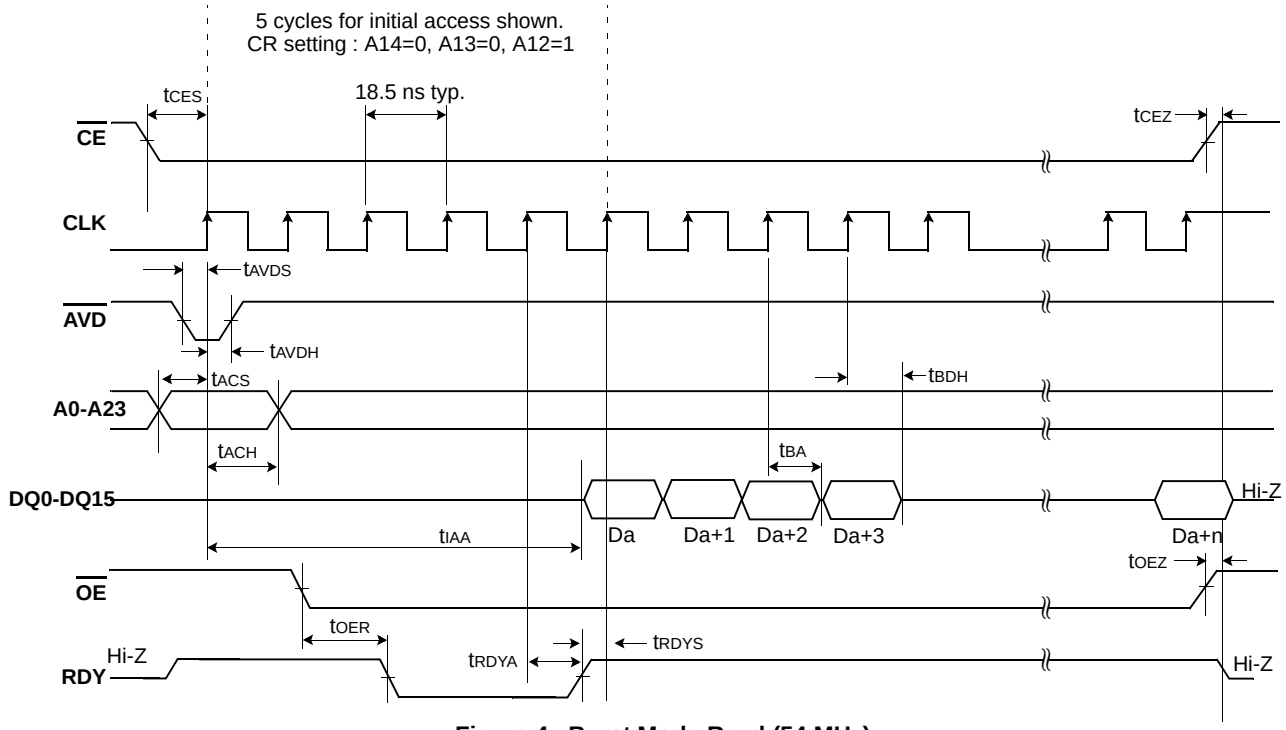



**Figure 4. Burst Mode Read (54 MHz)**

## SWITCHING WAVEFORMS

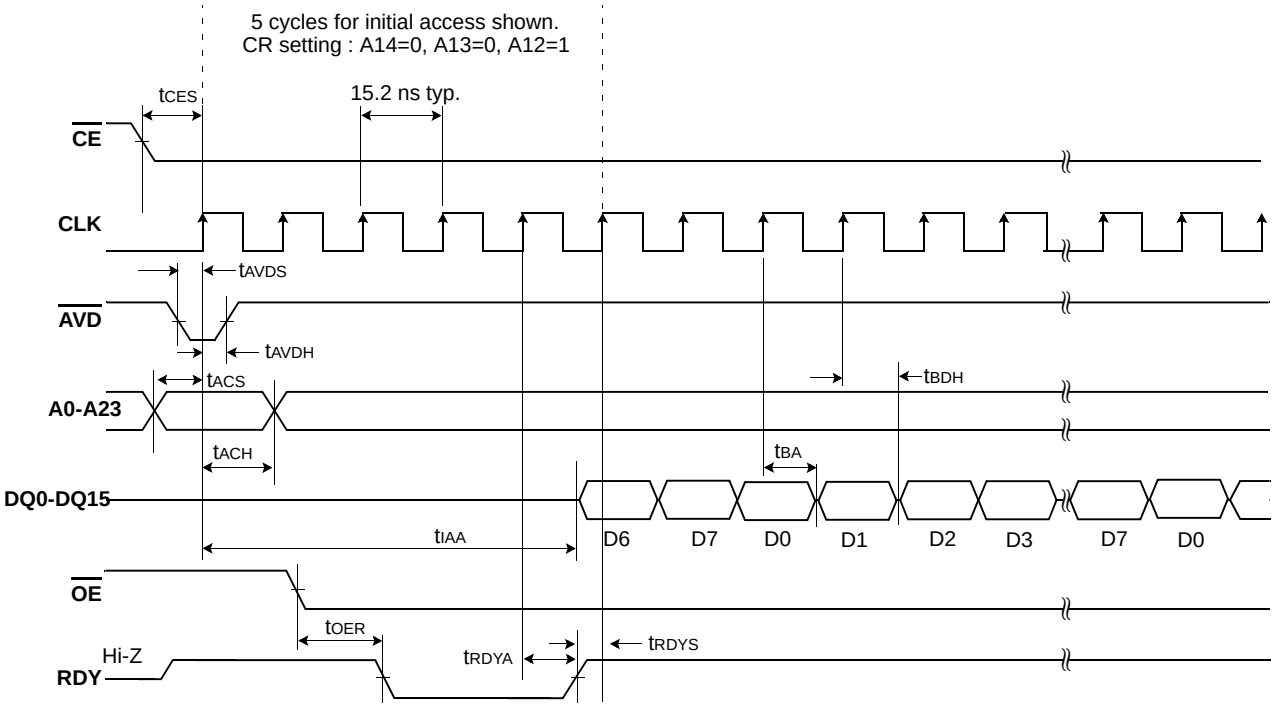



**Figure 5. 8 word Linear Burst Mode with Wrap Around (66 MHz)**

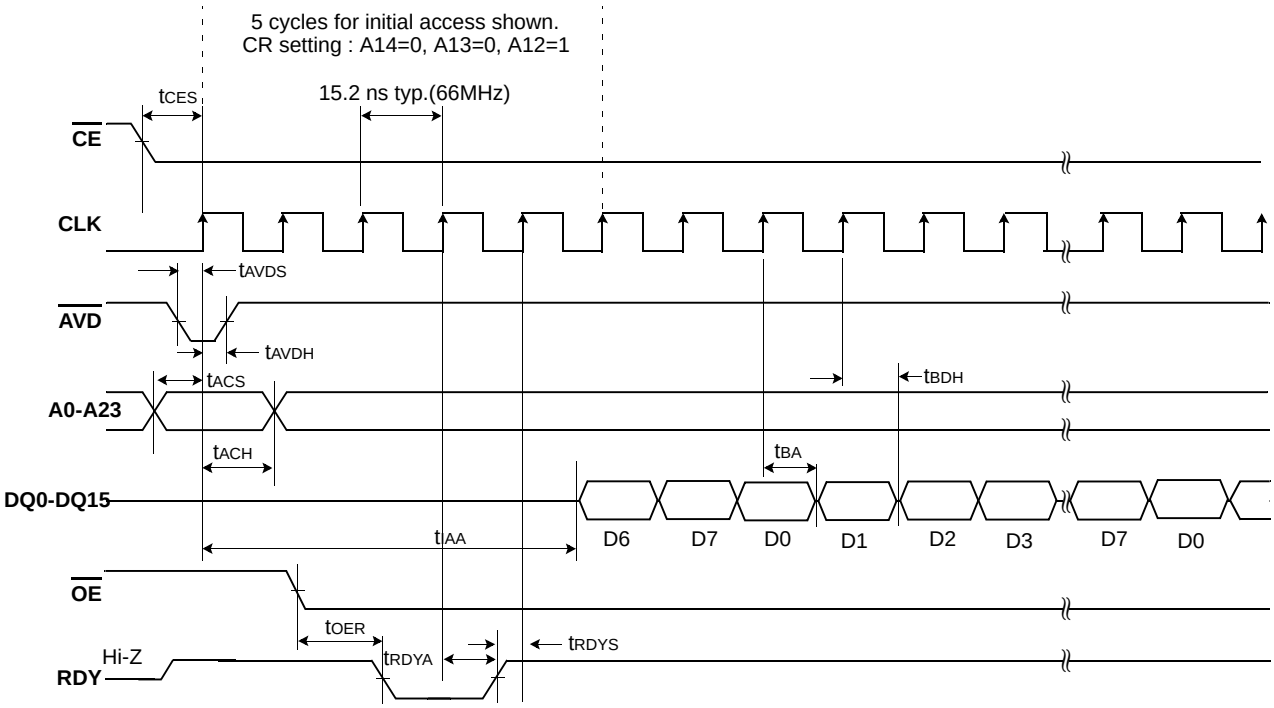



**Figure 6. 8 word Linear Burst with RDY Set One Cycle Before Data (CR setting : A18=1)**

## SWITCHING WAVEFORMS

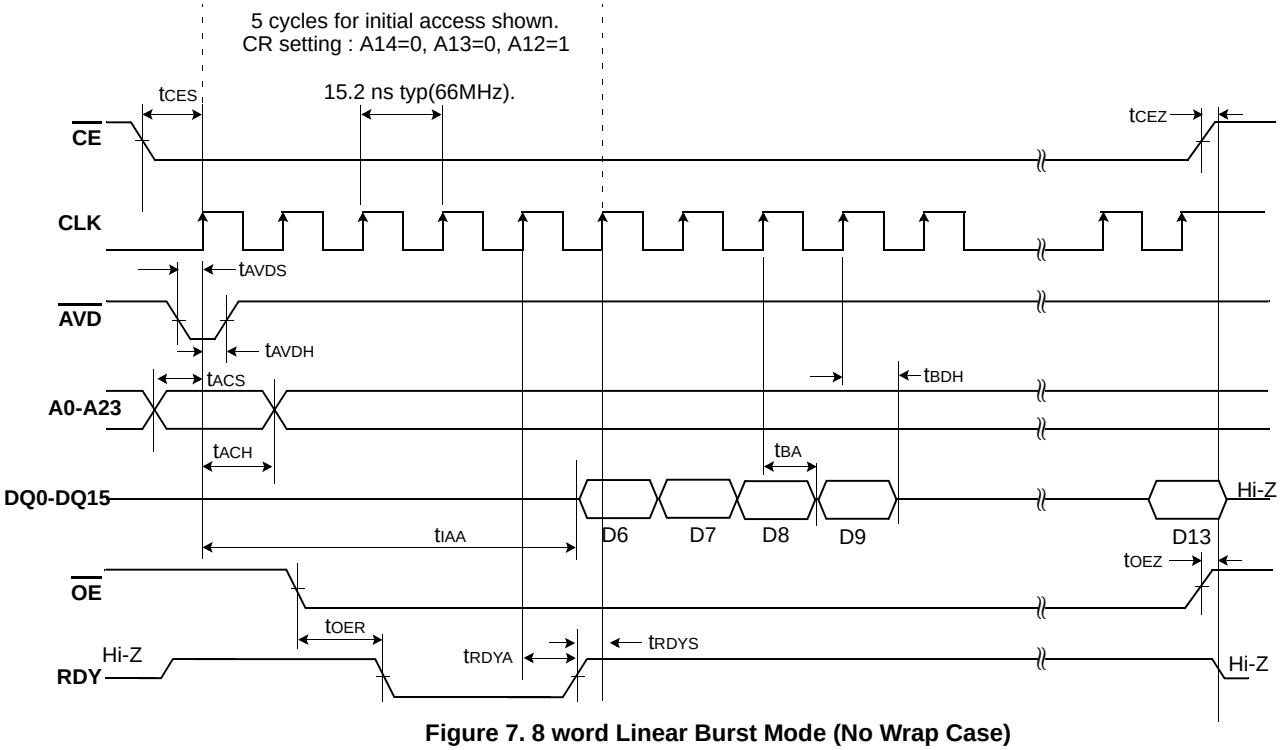



**Figure 7. 8 word Linear Burst Mode (No Wrap Case)**

## AC CHARACTERISTICS

### Asynchronous Read

| Parameter | | Symbol | 7B | | 7C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Access Time from $\overline{CE}$ Low | | $t_{CE}$ | - | 90 | - | 80 | ns |
| Asynchronous Access Time | | $t_{AA}$ | - | 90 | - | 80 | ns |
| $\overline{AVD}$ Low Setup Time to $\overline{CE}$ Enable | | $t_{AVDCS}$ | 0 | - | 0 | - | ns |
| $\overline{AVD}$ Low Hold Time from $\overline{CE}$ Disable | | $t_{AVDCH}$ | 0 | - | 0 | - | ns |
| Output Enable to Output Valid | | $t_{OE}$ | - | 20 | - | 20 | ns |
| Output Enable Hold Time | Read | $t_{OEH}$ | 0 | - | 0 | - | ns |
| | Toggle and Data Polling | | 10 | - | 10 | - | ns |
| Output Disable to High Z(Note 1) | | $t_{OEZ}$ | - | 15 | - | 15 | ns |

**Note:** 1. Not 100% tested.

## SWITCHING WAVEFORMS

### Asynchronous Mode Read

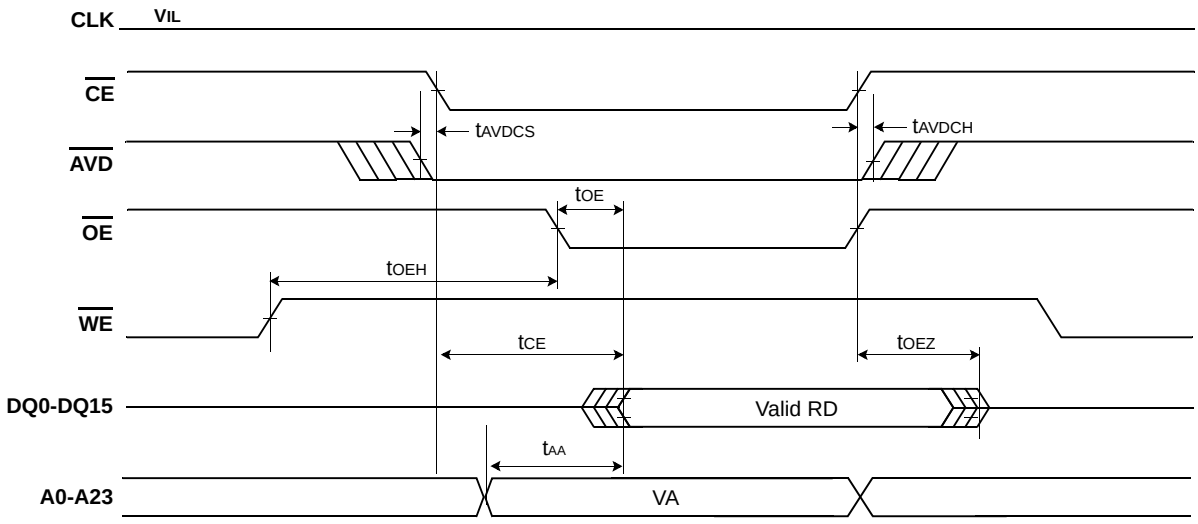



**Figure 8. Asynchronous Mode Read**

**Note:** VA=Valid Read Address, RD=Read Data.

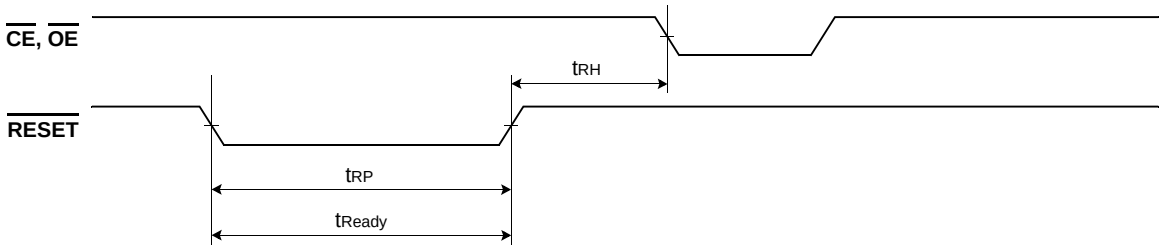
## AC CHARACTERISTICS

### Hardware Reset($\overline{RESET}$)

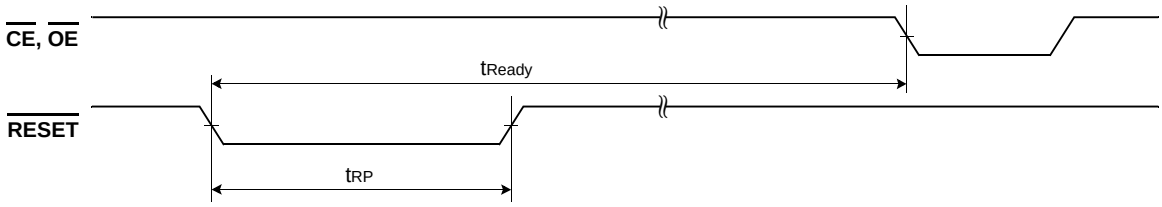
| Parameter | Symbol | All Speed Options | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $\overline{RESET}$ Pin Low(During Internal Routines) to Read Mode (Note) | $t_{Ready}$ | - | 20 | μs |
| $\overline{RESET}$ Pin Low(NOT During Internal Routines) to Read Mode (Note) | $t_{Ready}$ | - | 500 | ns |
| $\overline{RESET}$ Pulse Width | $t_{RP}$ | 200 | - | ns |
| Reset High Time Before Read (Note) | $t_{RH}$ | 200 | - | ns |
| $\overline{RESET}$ Low to Standby Mode | $t_{RPD}$ | 20 | - | μs |

**Note:** Not 100% tested.

## SWITCHING WAVEFORMS




Reset Timings NOT during Internal Routines




Reset Timings during Internal Routines

**Figure 9. Reset Timings**

## AC CHARACTERISTICS

### Erase/Program Operation

| Parameter | Symbol | 7B, 7C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $\overline{WE}$ Cycle Time(Note 1) | $t_{WC}$ | 100 | - | - | ns |
| Address Setup Time(Note 2) | $t_{AS}$ | 0 | - | - | ns |
| Address Hold Time(Note 2) | $t_{AH}$ | 50 | - | - | ns |
| Data Setup Time | $t_{DS}$ | 50 | - | - | ns |
| Data Hold Time | $t_{DH}$ | 0 | - | - | ns |
| Read Recovery Time Before Write | $t_{GHWL}$ | - | 0 | - | ns |
| $\overline{CE}$ Setup Time | $t_{CS}$ | 5 | - | - | ns |
| $\overline{CE}$ Hold Time | $t_{CH}$ | 5 | - | - | ns |
| $\overline{WE}$ Pulse Width | $t_{WP}$ | 70 | - | - | ns |
| $\overline{WE}$ Pulse Width High | $t_{WPH}$ | 30 | - | - | ns |
| Latency Between Read and Write Operations | $t_{SR/W}$ | 0 | - | - | ns |
| Word Programming Operation | $t_{PGM}$ | - | 11.5 | - | µs |
| Accelerated Single word Programming Operation | $t_{ACCPGM}$ | - | 6.5 | - | µs |
| Accelerated Quad word Programming Operation | $t_{ACCPGM\_QUAD}$ | - | 6.5 | - | µs |
| Block Erase Operation (Note 3) | $t_{BERS}$ | - | 0.7 | - | sec |
| $V_{PP}$ Rise and Fall Time | $t_{VPP}$ | 500 | - | - | ns |
| $V_{PP}$ Setup Time (During Accelerated Programming) | $t_{VPS}$ | 1 | - | - | µs |
| $V_{CC}$ Setup Time | $t_{VCS}$ | 50 | - | - | µs |

**Notes:**
1. Not 100% tested.
2. In write timing, addresses are latched on the falling edge of $\overline{WE}$.
3. Include the preprogramming time.

### FLASH Erase/Program Performance

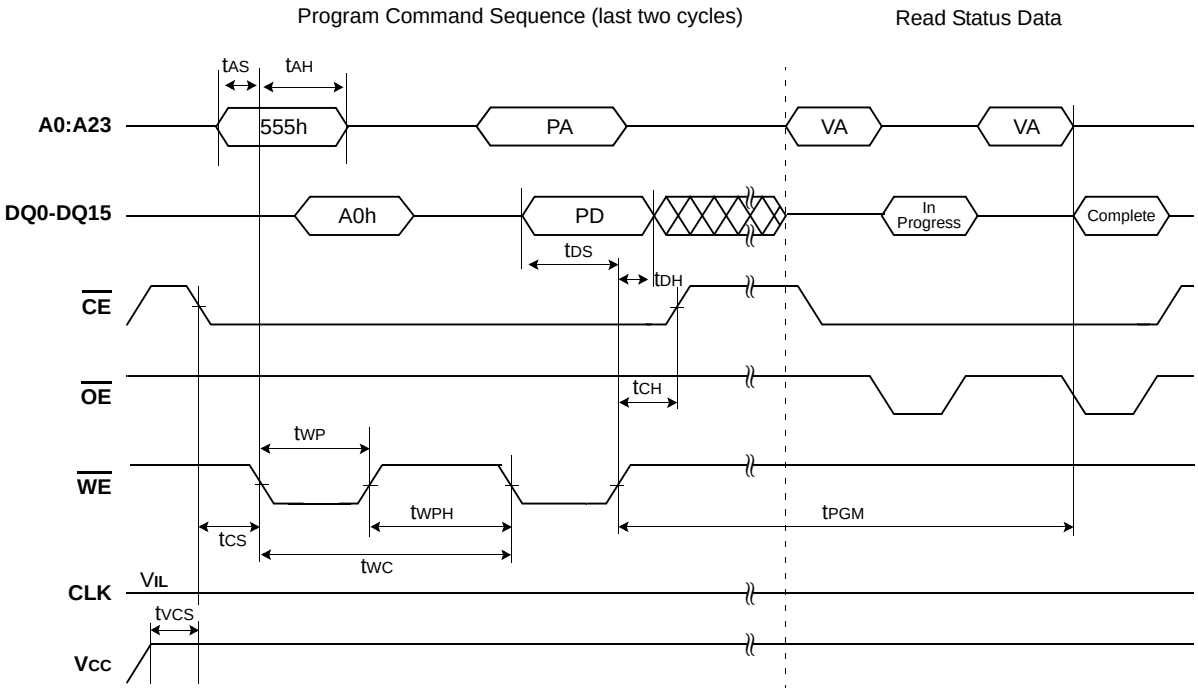
| Parameter | | Limits | | | Unit | Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Block Erase Time | 32 Kword | - | 0.7 | 14 | sec | Includes 00h programming prior to erasure |
| | 4 Kword | - | 0.2 | 4 | | |
| Chip Erase Time | | - | 360 | - | | |
| Word Programming Time | | - | 11.5 | 210 | µs | Excludes system level overhead |
| Accelerated Sinlge Programming Time (@word) | | - | 6.5 | 120 | | |
| Accelerated Quad Programming Time (@word) | | - | 1.6 | 30 | | |
| Chip Programming Time | | - | 193 | - | sec | |
| Accelerated Single word Chip Programming Time | | - | 109 | - | | |
| Accelerated Quad word Chip Programming Time | | - | 27 | - | | |
| Erase/Program Endurance (Note 3) | | 100,000 | - | - | Cycles | Minimum 100,000 cycles guaranteed in all Bank |

**Notes:**

1. 25°C, $V_{CC}$ = 1.8V, 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the two or four bus cycle command necessary to program each word. In the preprogramming step of the Internal Erase Routine, all words are programmed to 00H before erasure.
3. 100K Program/Erase Cycle in all Bank

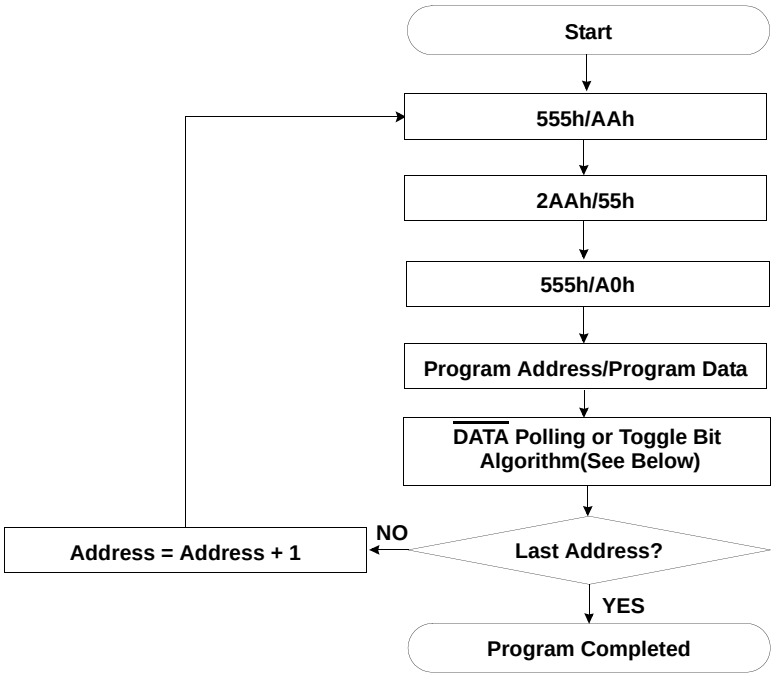
## SWITCHING WAVEFORMS

### Program Operations

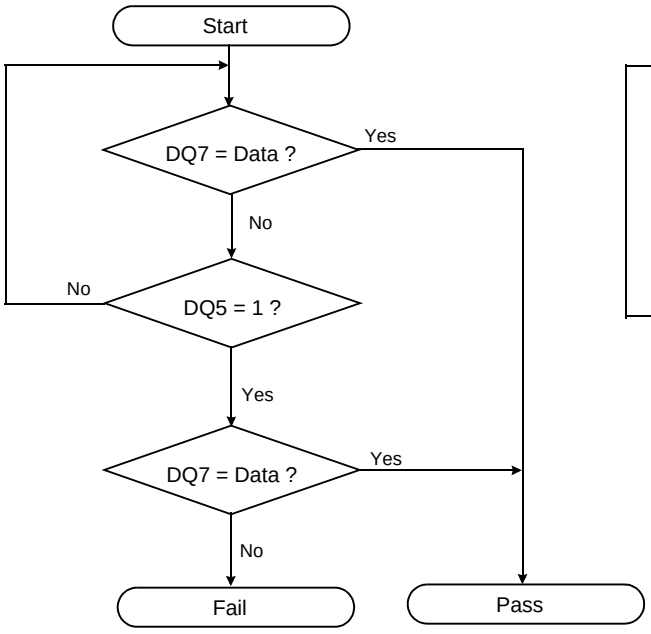



**Notes:**
1. PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
2. “In progress” and “complete” refer to status of program operation.
3. A16–A23 are don’t care during command sequence unlock cycles.
4. Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.
5. $\overline{AVD}$ Setup/Hold Time to $\overline{CE}$ Enable are same to Asynchronous Mode Read

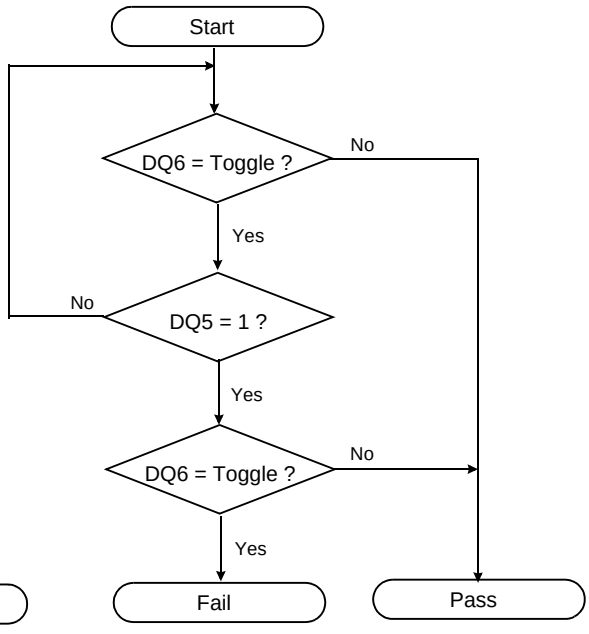
**Figure 10. Program Operation Timing**




**Program Command Sequence (address/data)**




**Data Polling Algorithms**

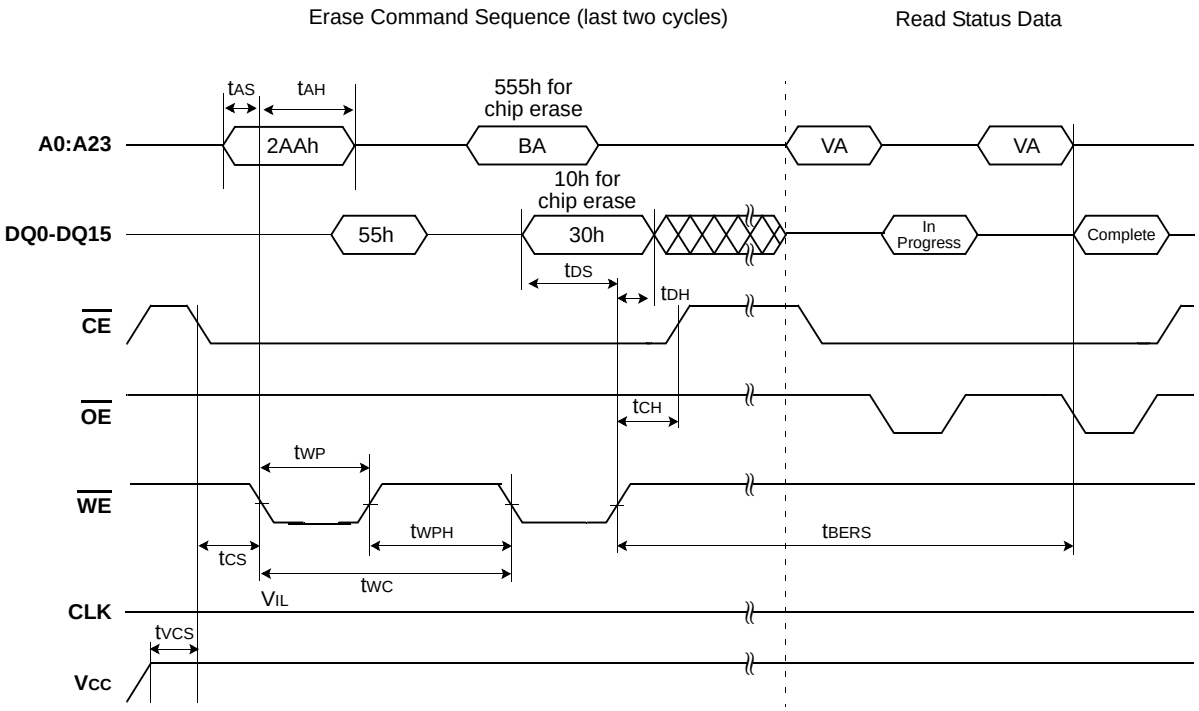



**Toggle Bit Algorithms**

**Figure 11. Program Operation Flow Chart**

## SWITCHING WAVEFORMS

### Erase Operation




**Notes:**

1. BA is the block address for Block Erase.
2. Address bits A16–A23 are don't cares during unlock cycles in the command sequence.
3. Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.
4. $\overline{AVD}$ Setup/Hold Time to $\overline{CE}$ Enable are same to Asynchronous Mode Read

**Figure 12. Chlp/Block Erase Operations**

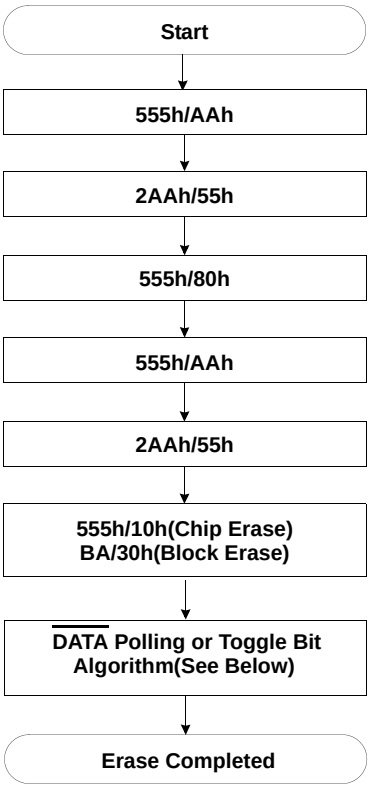
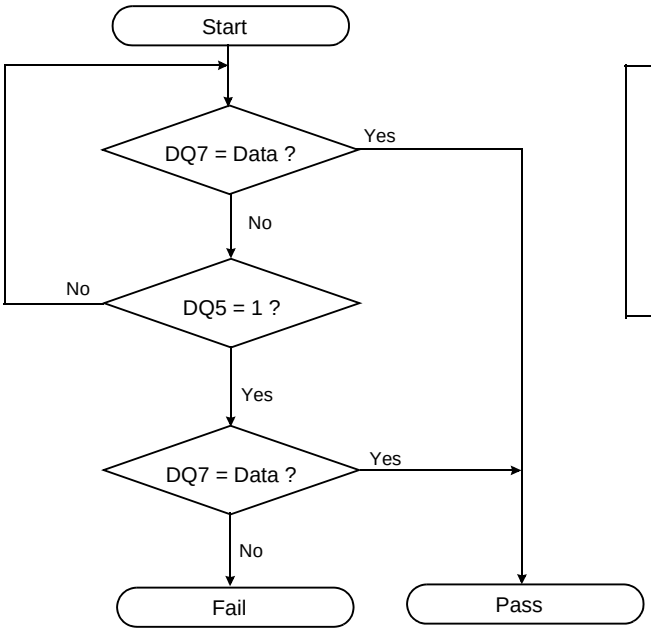
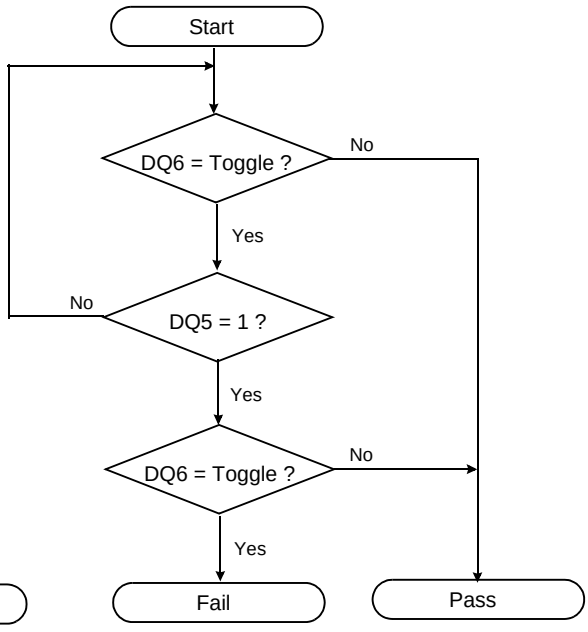



**Figure 13. Erase Operation Flow Chart**



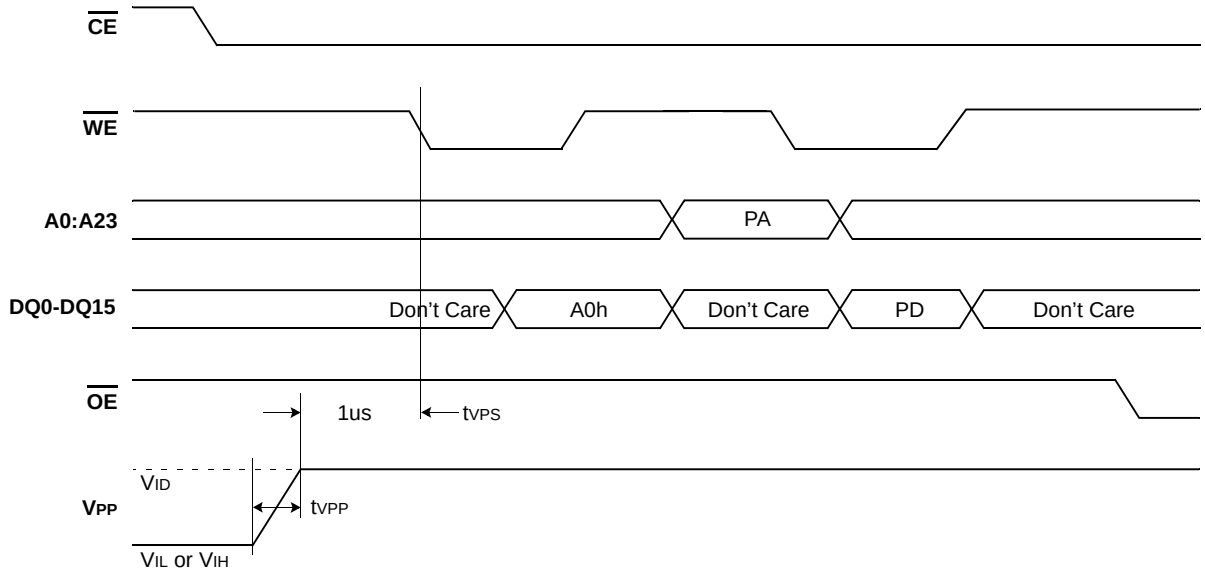

**Data Polling Algorithms**



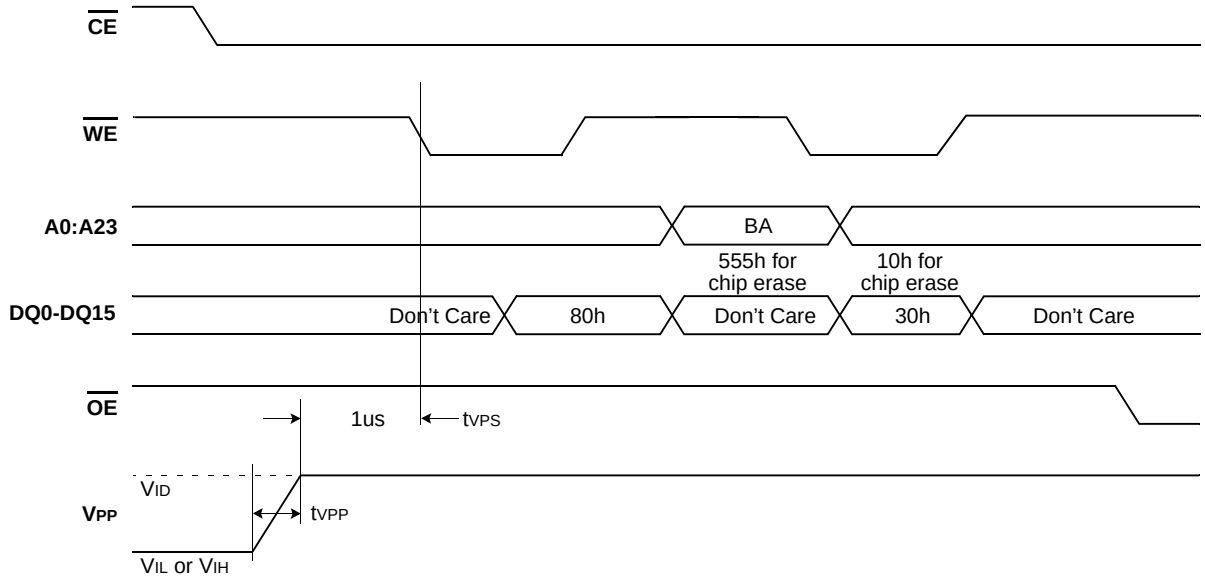

**Toggle Bit Algorithms**

## SWITCHING WAVEFORMS

### Unlock Bypass Program Operations(Accelerated Program)




### Unlock Bypass Block Erase Operations




**Notes:**

1. $V_{PP}$ can be left high for subsequent programming pulses.
2. Use setup and hold times from conventional program operations.
3. Unlock Bypass Program/Erase commands can be used when the $V_{ID}$ is applied to Vpp.
4. $\overline{AVD}$ Setup/Hold Time to $\overline{CE}$ Enable are same to Asynchronous Mode Read

**Figure 14. Unlock Bypass Operation Timings**

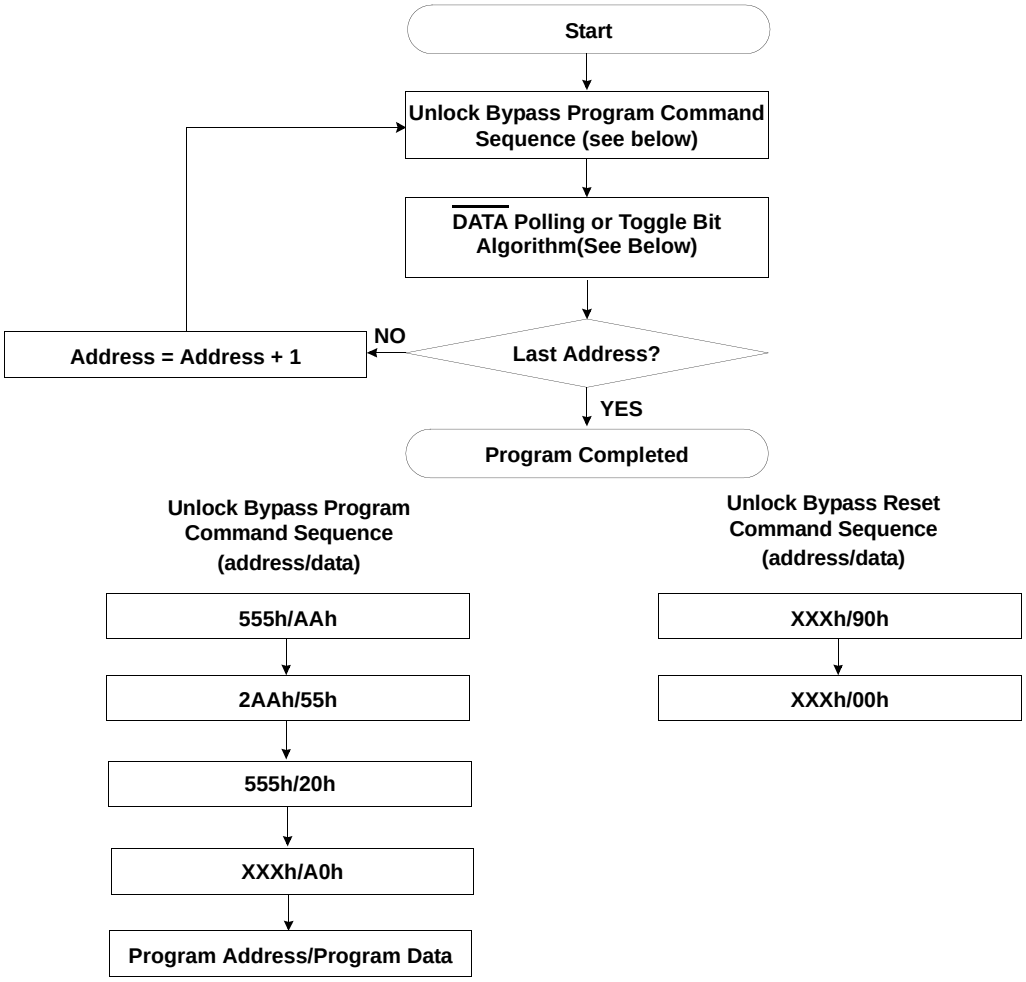
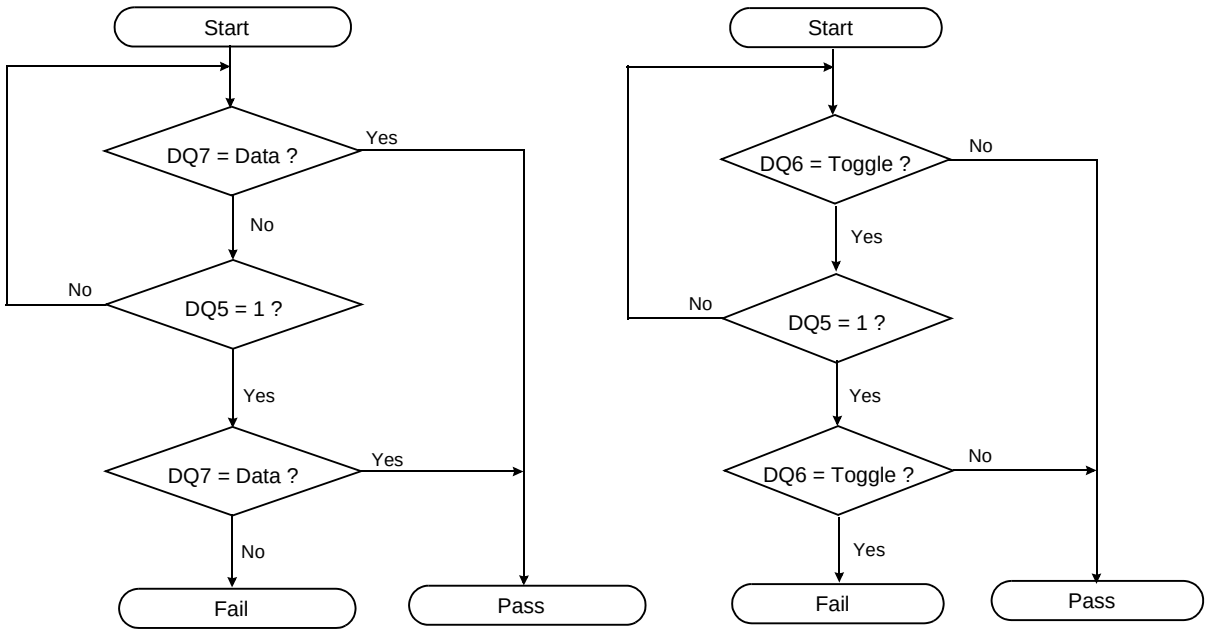


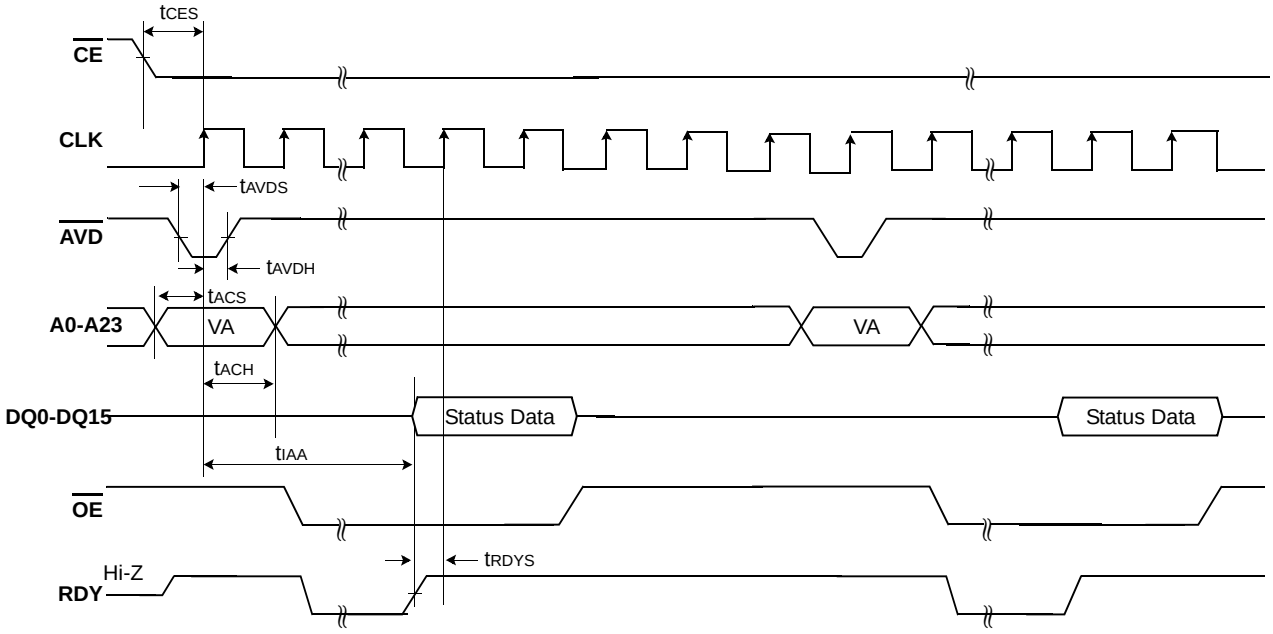

**Figure 15. Unlock Bypass Operation Flow Chart**




**Data Polling Algorithms** **Toggle Bit Algorithms**

## SWITCHING WAVEFORMS

### Data Polling Operations

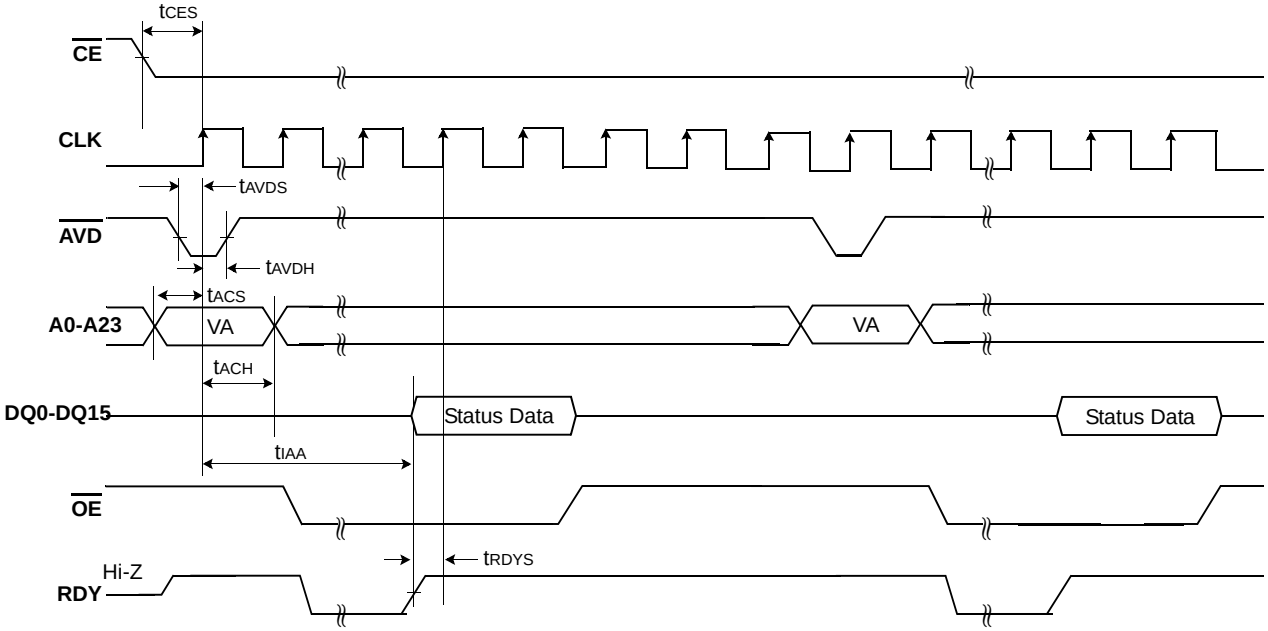



**Notes:**

1. VA = Valid Address. When the Internal Routine operation is complete, and Data Polling will output true data.

**Figure 16. Data Polling Timings (During Internal Routine)**

### Toggle Bit Operations




**Notes:**

1. VA = Valid Address. When the Internal Routine operation is complete, the toggle bits will stop toggling.

**Figure 17. Toggle Bit Timings(During Internal Routine)**

## SWITCHING WAVEFORMS

### Read While Write Operations

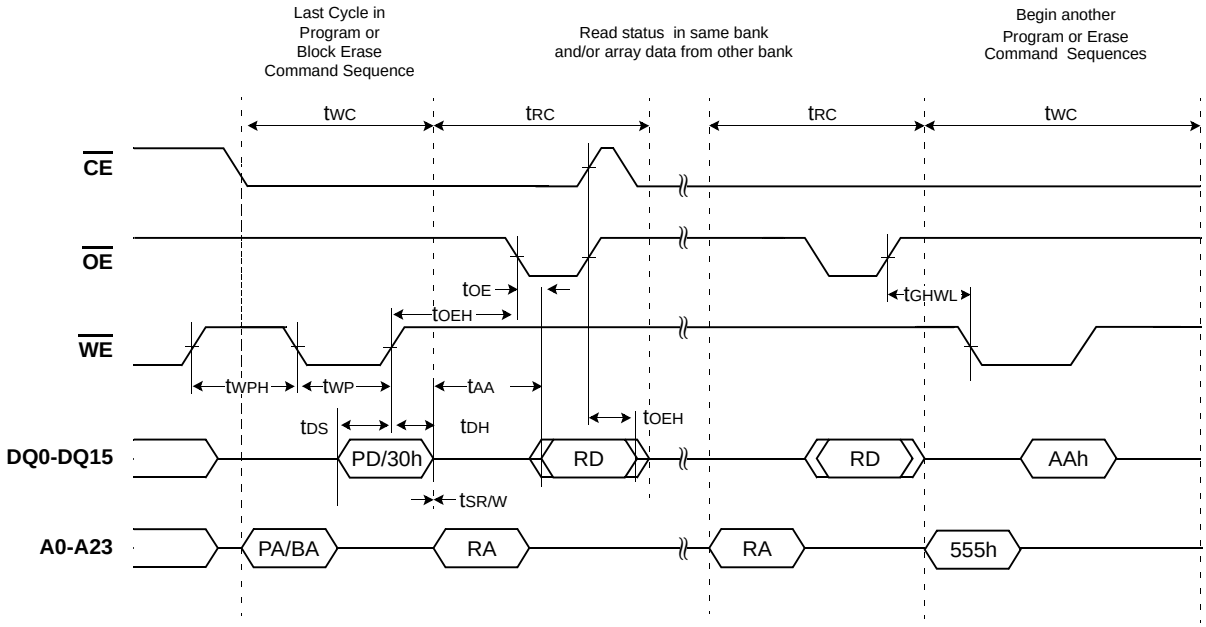



**Figure 18. Read While Write Operation**

**Note:**
Breakpoints in waveforms indicate that system may alternately read array data from the “non-busy bank” and checking the status of the program or erase operation in the “busy” bank.

## Crossing of First Word Boundary in Burst Read Mode

The additional clock insertion for word boundary is needed ***only at the first crossing*** of word boundary. This means that no addtional clock cycle is needed from 2nd word boundary crossing to the end of continuous burst read. Also, the number of addtional clock cycle for the first word boundary can varies from zero to three cycles, and the exact number of additional clock cycle depends on the starting address of burst read.

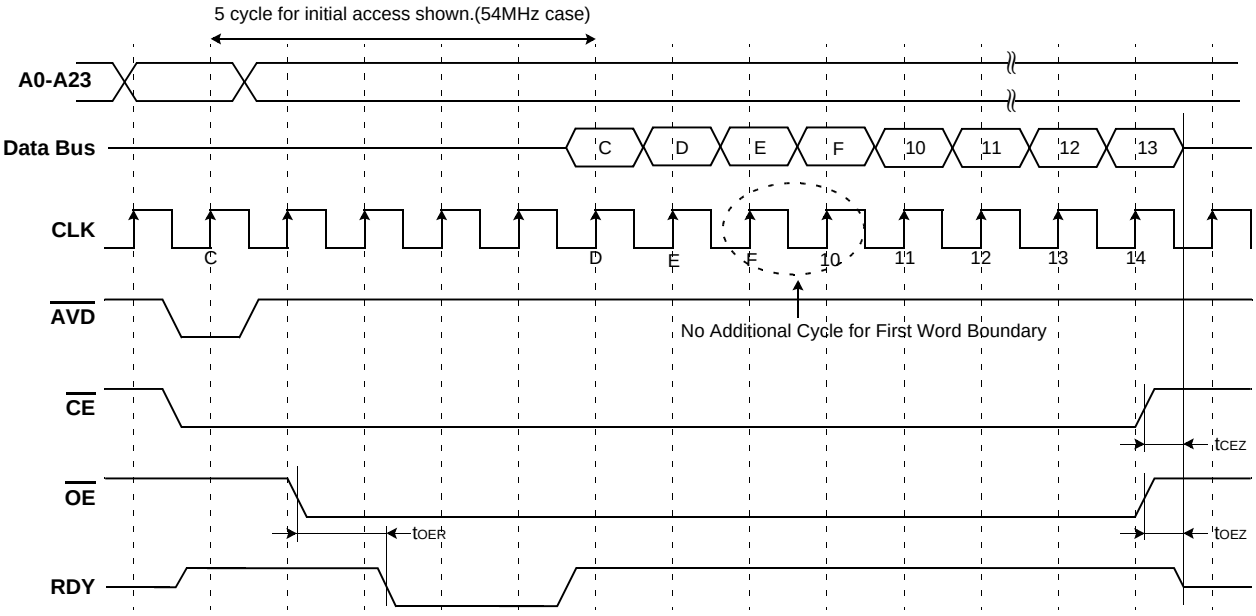
The rule to determine the additional clock cycle is as follows. All addresses can be divided into 4 groups. The applied rule is "The residue obtained when the address is divided by 4" or "two LSB bits of address". Using this rule, all address can be divided by 4 different groups as shown in below table. For simplicity of terminology, "4N" stands for the address of which the residue is "0"(or the two LSB bits are "00") and "4N+1" for the address of which the residue is "1"(or the two LSB bits are "01"), etc.

The additional clock cycles for first word boundary crossing are zero, one, two or three when the burst read start from "4N" address, "4N+1" address, "4N+2" address or "4N+3" address respectively.

**Starting Address vs. Additional Clock Cycles for first word boundary**

| Srarting Address Group for Burst Read | The Residue of (Address/4) | LSB Bits of Address | Additional Clock Cycles for First Word Boundary Crossing |
|---|---|---|---|
| 4N | 0 | 00 | 0 cycle |
| 4N+1 | 1 | 01 | 1 cycle |
| 4N+2 | 2 | 10 | 2 cycles |
| 4N+3 | 3 | 11 | 3 cycles |

**Case 1 : Start from "4N" address group**

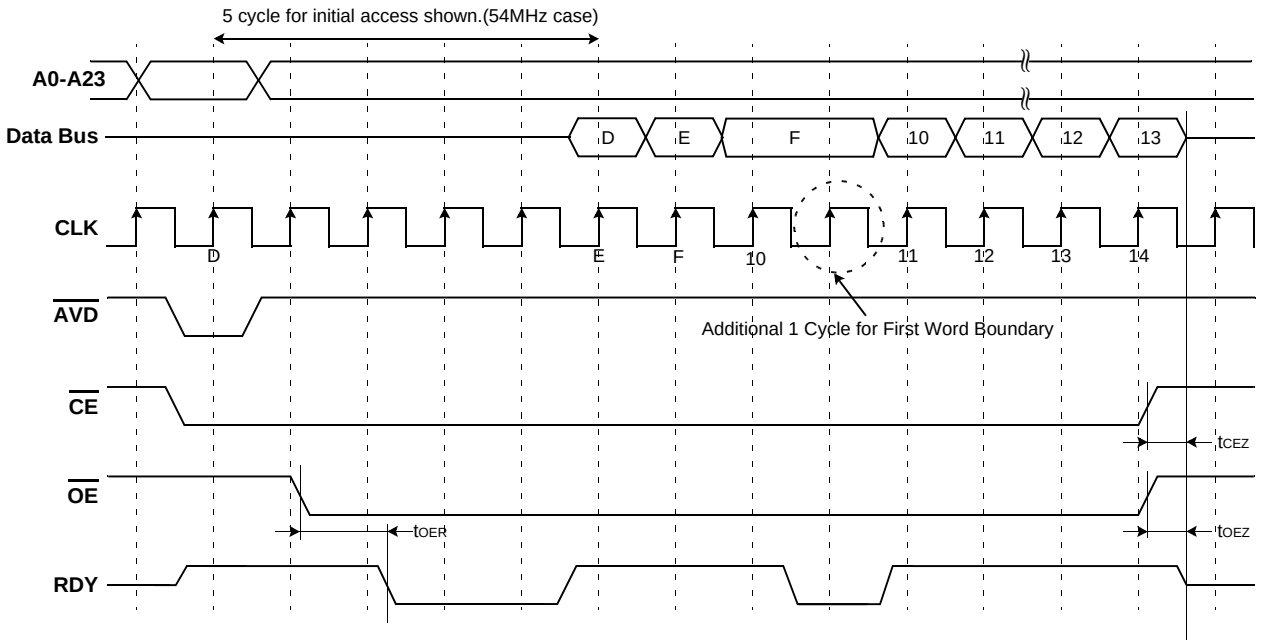



**Notes:**

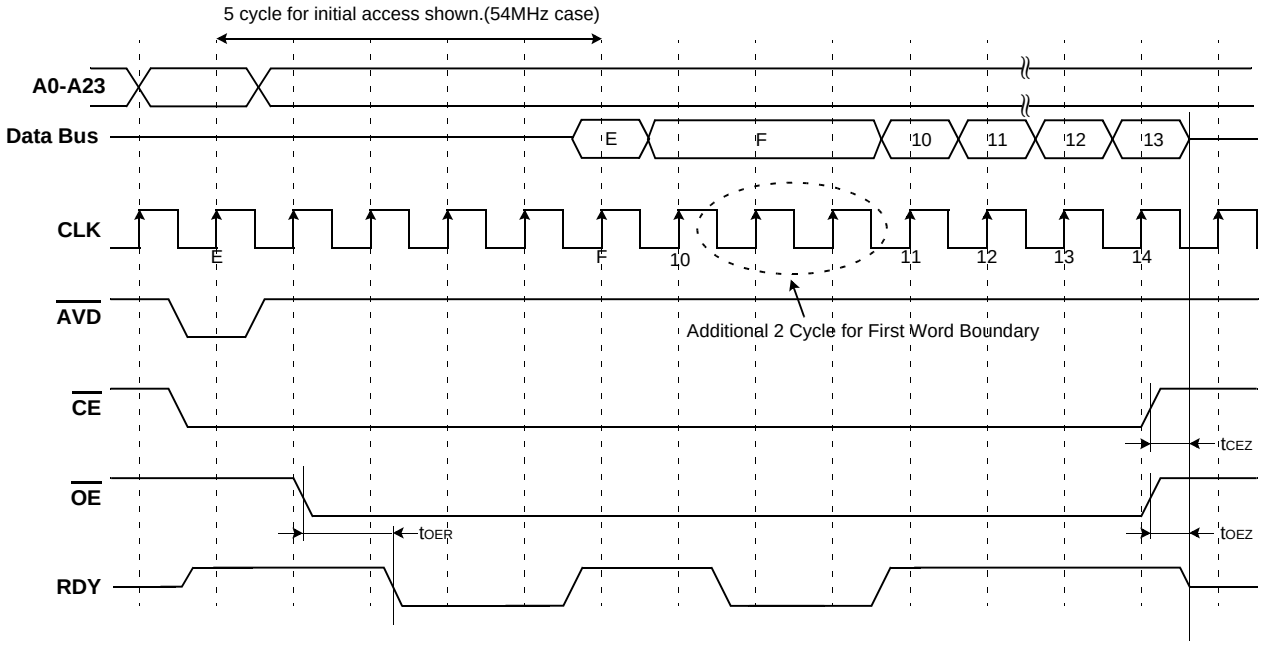
1. Address boundry occurs every 16 words beginning at address 00000FH , 00001FH , 00002FH , etc.
2. Address 000000H is also a boundry crossing.
3. No additional clock cycles are needed except for 1st boundary crossing.

**Figure 19. Crossing of first word boundary in burst read mode.**

**Case2 : Start from "4N+1" address group**




**Case 3 : Start from "4N+2" address group**

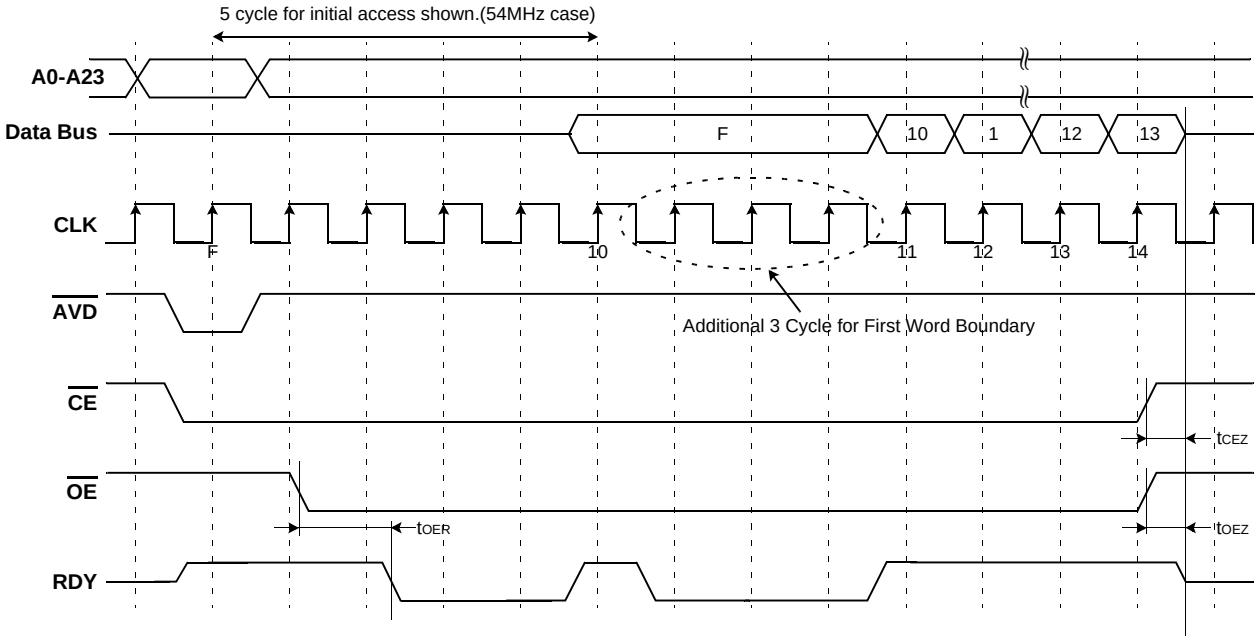



**Notes:**

1. Address boundry occurs every 16 words beginning at address 00000FH , 00001FH , 00002FH , etc.
2. Address 000000H is also a boundry crossing.
3. No additional clock cycles are needed except for 1st boundary crossing.

**Figure 20. Crossing of first word boundary in burst read mode.**

**Case4 : Start from "4N+3" address group**




**Notes:**

1. Address boundry occurs every 16 words beginning at address 00000FH , 00001FH , 00002FH , etc.
2. Address 000000H is also a boundry crossing.
3. No additional clock cycles are needed except for 1st boundary crossing.

**Figure 21. Crossing of first word boundary in burst read mode.**