

18Mb DDRII SRAM Specification

165FBGA with Pb & Pb-Free
(RoHS compliant)

INFORMATION IN THIS DOCUMENT IS PROVIDED IN RELATION TO SAMSUNG PRODUCTS, AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

NOTHING IN THIS DOCUMENT SHALL BE CONSTRUED AS GRANTING ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE,

TO ANY INTELLECTUAL PROPERTY RIGHTS IN SAMSUNG PRODUCTS OR TECHNOLOGY. ALL INFORMATION IN THIS DOCUMENT IS PROVIDED

ON AS "AS IS" BASIS WITHOUT GUARANTEE OR WARRANTY OF ANY KIND.

1. For updates or additional information about Samsung products, contact your nearest Samsung office.
2. Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where Product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

* Samsung Electronics reserves the right to change products or specification without notice.

www.DataSheet4U.com

Document Title

512Kx36-bit, 1Mx18-bit DDRII CIO b4 SRAM

Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|-----------------|--|-------------------|---------------|
| 0.0 | 1. Initial document. | Dec. 16, 2002 | Advance |
| 0.1 | 2. Add the speed bin (-25) | Jan. 27, 2003 | Preliminary |
| 0.2 | 1. Correct the JTAG ID register definition 2. Correct the AC timing parameter (delete the tKH \bar{K} H Max value) | Mar. 20, 2003 | Preliminary |
| 0.3 | 1. Change the Maximum Clock cycle time. 2. Correct the 165FBGA package ball size. | April. 4, 2003 | Preliminary |
| 0.4 | 1. Add the power up/down sequencing comment. 2. Update the DC current parameter (Icc and Isb). 3. Change the Max. speed bin from -33 to -30. | June. 20, 2003 | Preliminary |
| 0.5 | 1. Change the ISB1. | Oct. 20, 2003 | Preliminary |

| Speed Bin | From | To |
|-----------|------|-----|
| -30 | 200 | 230 |
| -25 | 180 | 210 |
| -20 | 160 | 190 |
| -16 | 140 | 170 |

| | | | |
|-----|---|---------------|-------|
| 1.0 | 1. Final spec release | Oct. 31, 2003 | Final |
| 2.0 | 1. Delete the x8 Org. 2. Delete the 300MHz speed bin | Nov. 28, 2003 | Final |
| 3.0 | 1. Add the Industrial temp. & Lead Free Package | Nov. 10, 2004 | Final |
| 4.0 | 1. Add the 300MHz speed bin | Mar. 29, 2006 | Final |
| 5.0 | 1. Change Vss/SA to NC/SA in Pin Configuration | Jul. 26, 2006 | Final |

K71163684B K71161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

512Kx36-bit, 1Mx18-bit DDRII CIO b4 SRAM

FEATURES

- 1.8V+0.1V/-0.1V Power Supply.
- DLL circuitry for wide output data valid window and future frequency scaling.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O, 1.8V+0.1V/-0.1V for 1.8V I/O.
- Pipelined, double-data rate operation.
- Common data input/output bus.
- HSTL I/O
- Full data coherency, providing most current data.
- Synchronous pipeline read with self timed late write.
- Registered address, control and data input/output.
- DDR (Double Data Rate) Interface on read and write ports.
- Fixed 4-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks (K and \overline{K}) for accurate DDR timing at clock rising edges only.
- Two input clocks for output data (C and \overline{C}) to minimize clock-skew and flight-time mismatches.
- Two echo clocks (CQ and \overline{CQ}) to enhance output data traceability.
- Single address bus.
- Byte write (x18, x36) function.
- Simple depth expansion with no data contention.
- Programmable output impedance.
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball array) with body size of 13mmx15mm. & Lead Free
- Operating in commercial and industrial temperature range.

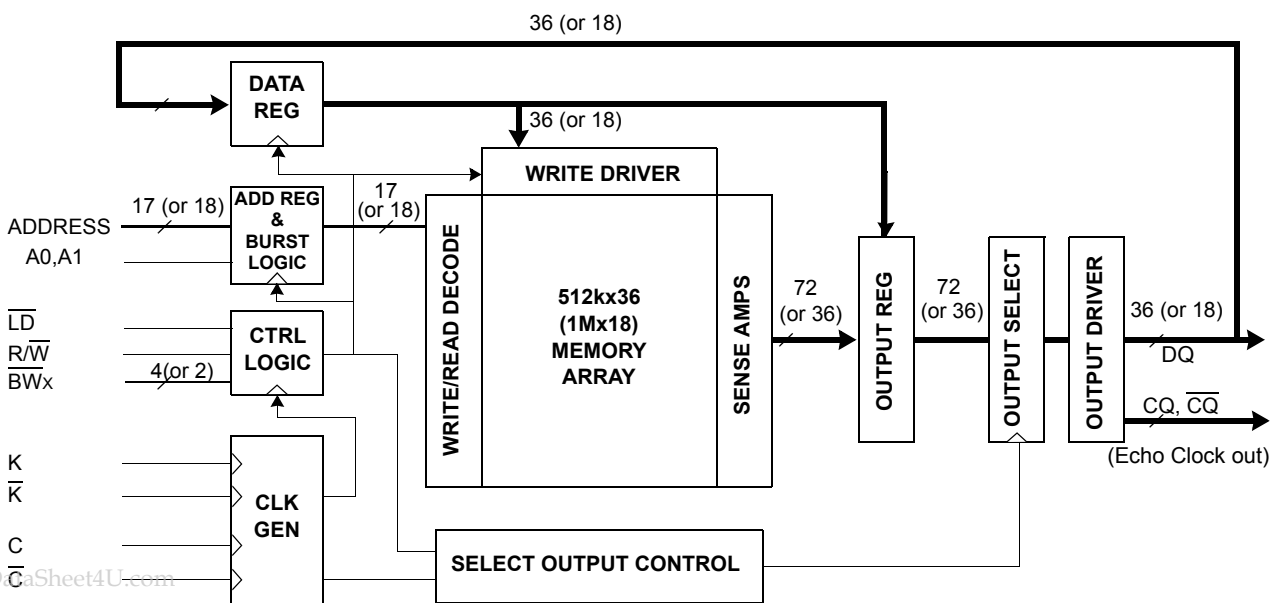
| Organization | Part Number | Cycle Time | Access Time | Unit |
|--------------|-----------------------|------------|-------------|------|
| X36 | K71163684B-E(F)C(I)30 | 3.3 | 0.45 | ns |
| | K71163684B-E(F)C(I)25 | 4.0 | 0.45 | ns |
| | K71163684B-E(F)C(I)20 | 5.0 | 0.45 | ns |
| | K71163684B-E(F)C(I)16 | 6.0 | 0.50 | ns |
| X18 | K71161884B-E(F)C(I)30 | 3.3 | 0.45 | ns |
| | K71161884B-E(F)C(I)25 | 4.0 | 0.45 | ns |
| | K71161884B-E(F)C(I)20 | 5.0 | 0.45 | ns |
| | K71161884B-E(F)C(I)16 | 6.0 | 0.50 | ns |

* -E(F)C(I)

E(F) [Package type] : E-Pb Free, F-Pb

C(I) [Operating Temperature] : C-Commercial, I-Industrial

FUNCTIONAL BLOCK DIAGRAM



Notes: 1. Numbers in () are for x18 device

DDRII SRAM and Double Data Rate comprise a new family of products developed by Cypress, Hitachi, IDT, Micron, NEC and Samsung technology.

K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

PIN CONFIGURATIONS(TOP VIEW) K7I163684B(512Kx36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|-------------------|--------|--------|------|-------------------|----------------|-------------------|-----------------|------|--------|------|
| A | \overline{CQ} | NC/SA* | NC/SA* | R/W | \overline{BW}_2 | \overline{K} | \overline{BW}_1 | \overline{LD} | SA | NC/SA* | CQ |
| B | NC | DQ27 | DQ18 | SA | \overline{BW}_3 | K | \overline{BW}_0 | SA | NC | NC | DQ8 |
| C | NC | NC | DQ28 | Vss | SA | SA0 | SA1 | Vss | NC | DQ17 | DQ7 |
| D | NC | DQ29 | DQ19 | Vss | Vss | Vss | Vss | Vss | NC | NC | DQ16 |
| E | NC | NC | DQ20 | VDDQ | Vss | Vss | Vss | VDDQ | NC | DQ15 | DQ6 |
| F | NC | DQ30 | DQ21 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ5 |
| G | NC | DQ31 | DQ22 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ14 |
| H | \overline{Doff} | VREF | VDDQ | VDDQ | VDD | Vss | VDD | VDDQ | VDDQ | VREF | ZQ |
| J | NC | NC | DQ32 | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ13 | DQ4 |
| K | NC | NC | DQ23 | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ12 | DQ3 |
| L | NC | DQ33 | DQ24 | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ2 |
| M | NC | NC | DQ34 | Vss | Vss | Vss | Vss | Vss | NC | DQ11 | DQ1 |
| N | NC | DQ35 | DQ25 | Vss | SA | SA | SA | Vss | NC | NC | DQ10 |
| P | NC | NC | DQ26 | SA | SA | C | SA | SA | NC | DQ9 | DQ0 |
| R | TDO | TCK | SA | SA | SA | \overline{C} | SA | SA | SA | TMS | TDI |

Notes : 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 3A for 36Mb, 10A for 72Mb, 2A for 144Mb.
2. BW0 controls write to DQ0:DQ8, BW1 controls write to DQ9:DQ17, BW2 controls write to DQ18:DQ26 and BW3 controls write to DQ27:DQ35.

PIN NAME

| SYMBOL | PIN NUMBERS | DESCRIPTION | NOTE |
|--|---|--|------|
| K, \overline{K} | 6B, 6A | Input Clock | |
| C, \overline{C} | 6P, 6R | Input Clock for Output Data | 1 |
| CQ, \overline{CQ} | 11A, 1A | Output Echo Clock | |
| \overline{Doff} | 1H | DLL Disable when low | |
| SA0,SA1 | 6C,7C | Burst Count Address Inputs | |
| SA | 9A,4B,8B,5C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R | Address Inputs | |
| DQ0-35 | 2B,3B,11B,3C,10C,11C,2D,3D,11D,3E,10E,11E,2F,3F 11F,2G,3G,11G,3J,10J,11J,3K,10K,11K,2L,3L,11L 3M,10M,11M,2N,3N,11N,3P,10P,11P | Data Inputs Outputs | |
| R/W | 4A | Read, Write Control Pin, Read active when high | |
| \overline{LD} | 8A | Synchronous Load Pin, bus Cycle sequence is to be defined when low | |
| $\overline{BW}_0, \overline{BW}_1, \overline{BW}_2, \overline{BW}_3$ | 7B,7A,5A,5B | Block Write Control Pin, active when low | |
| VREF | 2H,10H | Input Reference Voltage | |
| ZQ | 11H | Output Driver Impedance Control Input | 2 |
| VDD | 5F,7F,5G,7G,5H,7H,5J,7J,5K,7K | Power Supply (1.8 V) | |
| VDDQ | 4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L | Output Power Supply (1.5V or 1.8V) | |
| Vss | 4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L, 4M-8M,4N,8N | Ground | |
| TMS | 10R | JTAG Test Mode Select | |
| TDI | 11R | JTAG Test Data Input | |
| TCK | 2R | JTAG Test Clock | |
| TDO | 1R | JTAG Test Data Output | |
| NC | 2A,10A,3A,1B,9B,10B,1C,2C,9C,1D,9D,10D,1E,2E,9E, 1F,9F,10F,1G,9G,10G,1J,2J,9J,1K,2K,9K 1L,9L,10L,1M,2M,9M,1N,9N,10N,1P,2P,9P | No Connect | 3 |

Notes: 1. C, \overline{C} , K or \overline{K} cannot be set to VREF voltage.
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

PIN CONFIGURATIONS(TOP VIEW) K7I161884B(1Mx18)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|-------------------|--------|------|------|-----------------|----------------|-------------------|-----------------|------|--------|-----|
| A | \overline{CQ} | NC/SA* | SA | R/W | BW ₁ | \overline{K} | NC | \overline{LD} | SA | NC/SA* | CQ |
| B | NC | DQ9 | NC | SA | NC | K | $\overline{BW_0}$ | SA | NC | NC | DQ8 |
| C | NC | NC | NC | Vss | SA | SA0 | SA1 | Vss | NC | DQ7 | NC |
| D | NC | NC | DQ10 | Vss | Vss | Vss | Vss | Vss | NC | NC | NC |
| E | NC | NC | DQ11 | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ6 |
| F | NC | DQ12 | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ5 |
| G | NC | NC | DQ13 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | NC |
| H | \overline{Doff} | VREF | VDDQ | VDDQ | VDD | Vss | VDD | VDDQ | VDDQ | VREF | ZQ |
| J | NC | NC | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ4 | NC |
| K | NC | NC | DQ14 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ3 |
| L | NC | DQ15 | NC | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ2 |
| M | NC | NC | NC | Vss | Vss | Vss | Vss | Vss | NC | DQ1 | NC |
| N | NC | NC | DQ16 | Vss | SA | SA | SA | Vss | NC | NC | NC |
| P | NC | NC | DQ17 | SA | SA | C | SA | SA | NC | NC | DQ0 |
| R | TDO | TCK | SA | SA | SA | \overline{C} | SA | SA | SA | TMS | TDI |

Notes: 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 10A for 36Mb, 2A for 72Mb.
2. BW₀ controls write to DQ0:DQ8 and BW₁ controls write to DQ9:DQ17.

PIN NAME

| SYMBOL | PIN NUMBERS | DESCRIPTION | NOTE |
|-----------------------------------|---|--|------|
| K, \overline{K} | 6B, 6A | Input Clock | |
| C, \overline{C} | 6P, 6R | Input Clock for Output Data | 1 |
| CQ, \overline{CQ} | 11A, 1A | Output Echo Clock | |
| \overline{Doff} | 1H | DLL Disable when low | |
| SA0,SA1 | 6C,7C | Burst Count Address Inputs | |
| SA | 3A,9A,4B,8B,5C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R | Address Inputs | |
| DQ0-17 | 2B,11B,10C,3D,3E,11E,2F,11F,3G,10J,3K,11K,2L,11L 10M,3N,3P,11P | Data Inputs Outputs | |
| R/W | 4A | Read, Write Control Pin, Read active when high | |
| \overline{LD} | 8A | Synchronous Load Pin, bus Cycle sequence is to be defined when low | |
| BW ₀ , BW ₁ | 7B, 5A | Block Write Control Pin, active when low | |
| VREF | 2H,10H | Input Reference Voltage | |
| ZQ | 11H | Output Driver Impedance Control Input | 2 |
| VDD | 5F,7F,5G,7G,5H,7H,5J,7J,5K,7K | Power Supply (1.8 V) | |
| VDDQ | 4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L | Output Power Supply (1.5V or 1.8V) | |
| Vss | 4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N | Ground | |
| TMS | 10R | JTAG Test Mode Select | |
| TDI | 11R | JTAG Test Data Input | |
| TCK | 2R | JTAG Test Clock | |
| TDO | 1R | JTAG Test Data Output | |
| NC | 2A,10A,7A,1B,3B,5B,9B,10B,1C,2C,3C,9C,11C,1D,2D,9D,10D, 11D,1E,2E,9E,10E,1F,3F,9F,10F,1G,2G,9G,10G,11G 1J,2J,3J,9J,11J,1K,2K,9K,10K,1L,3L,9L,10L 1M,2M,3M,9M,11M,1N,2N,9N,10N,11N,1P,2P,9P,10P | No Connect | 3 |

Notes: 1. C, \overline{C} , K or \overline{K} cannot be set to VREF voltage.
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

GENERAL DESCRIPTION

The K71163684B and K71161884B are 18,874,368-bits DDR Common I/O Synchronous Pipelined Burst SRAMs.

They are organized as 524,288 words by 36bits for K71163684B and 1,048,576 words by 18 bits for K71161884B.

Address, data inputs, and all control signals are synchronized to the input clock (K or \overline{K}). Normally data outputs are synchronized to output clocks (C and \overline{C}), but when C and \overline{C} are tied high, the data outputs are synchronized to the input clocks (K and \overline{K}). Read data are referenced to echo clock (CQ or \overline{CQ}) outputs. Read address and write address are registered on rising edges of the input K clocks. Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 4-bit sequential for both read and write operations. Synchronous pipeline read and late write enable high speed operations. Simple depth expansion is accomplished by using \overline{LD} for port selection. Byte write operation is supported with \overline{BW}_0 and \overline{BW}_1 (\overline{BW}_2 and \overline{BW}_3) pins for x18 (x36) device. Nibble write operation is supported with \overline{NW}_0 and \overline{NW}_1 pins for x8 device. IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoring package pads attachment status with system.

The K71163684B and K71161884B are implemented with SAMSUNG's high performance 6T CMOS technology and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.

READ OPERATIONS

Read cycles are initiated by initiating $\overline{R/W}$ as high at the rising edge of the positive input clock K . Address is presented and stored in the read address register synchronized with K clock.

For 4-bit burst DDR operation, it will access four 36-bit, 18-bit or 8-bit data words with each read command. The first pipelined data is transferred out of the device triggered by \overline{C} clock following next \overline{K} clock rising edge. Next burst data is triggered by the rising edge of following C clock rising edge.

Continuous read operations are initiated with K clock rising edge. And pipelined data are transferred out of device on every rising edge of both C and \overline{C} clocks. In case C and \overline{C} tied to high, output data are triggered by K and \overline{K} instead of C and \overline{C} .

When the \overline{LD} is disabled after a read operation, the K71163684B and K71161884B will first complete burst read operation before entering into deselect mode at the next K clock rising edge. Then output drivers disabled automatically to high impedance state.

ECHO CLOCK OPERATION

To assure the output traceability, the SRAM provides the output Echo clock, pair of compliment clock CQ and \overline{CQ} , which are synchronized with internal data output. Echo clocks run free during normal operation. The Echo clock is triggered by internal output clock signal, and transferred to external through same structures as output driver.

POWER-UP/POWER-DOWN SUPPLY VOLTAGE SEQUENCING

The following power-up supply voltage application is recommended: V_{SS} , V_{DD} , V_{DDQ} , V_{REF} , then V_{IN} . V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN} , V_{REF} , V_{DDQ} , V_{DD} , V_{SS} . V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

WRITE OPERATIONS

Write cycles are initiated by activating $\overline{R/\overline{W}}$ as low at the rising edge of the positive input clock K.
Address is presented and stored in the write address register synchronized with next K clock.

For 4-bit burst DDR operation, it will write two 36-bit, 18-bit or 8-bit data words with each write command.
The first "late wrote" data is transferred and registered in to the device synchronous with next K clock rising edge.
Next burst data is transferred and registered synchronous with following \overline{K} clock rising edge.

Continuous write operations are initiated with K rising edge.
And "late wrote" data is presented to the device on every rising edge of both K and \overline{K} clocks.

When the \overline{LD} is disabled, the K71163684B and K71161884B will enter into deselect mode.
The device disregards input data presented on the same cycle \overline{W} disabled.

The K71163684B and K71161884B support byte write operations.
With activating $\overline{BW_0}$ or $\overline{BW_1}$ ($\overline{BW_2}$ or $\overline{BW_3}$) in write cycle, only one byte of input data is presented.
In K71161884B $\overline{BW_0}$ controls write operation to D0:D8, $\overline{BW_1}$ controls write operation to D9:D17.
And in K71163684B $\overline{BW_2}$ controls write operation to D18:D26, $\overline{BW_3}$ controls write operation to D27:D35.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to Vss through a precision resistor(RQ).
The value of RQ (within 15%) is five times the output impedance desired.

For example, 250 Ω resistor will give an output impedance of 50 Ω .
Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles.
In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.

There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

CLOCK CONSIDERATION

K71163684B and K71161884B utilize internal DLL (Delay-Locked Loops) for maximum output data valid window.
It can be placed into a stopped-clock state to minimize power with a modest restart time of 1024 clock cycles.
Circuitry automatically resets the DLL when absence of input clock is detected.

SINGLE CLOCK MODE

K71163684B and K71161884B can be operated with the single clock pair K and \overline{K} ,
instead of C or \overline{C} for output clocks.
To operate these devices in single clock mode, C and \overline{C} must be tied high during power up and must be maintained high during operation.
After power up, this device can't change to or from single clock mode.
System flight time and clock skew could not be compensated in this mode.

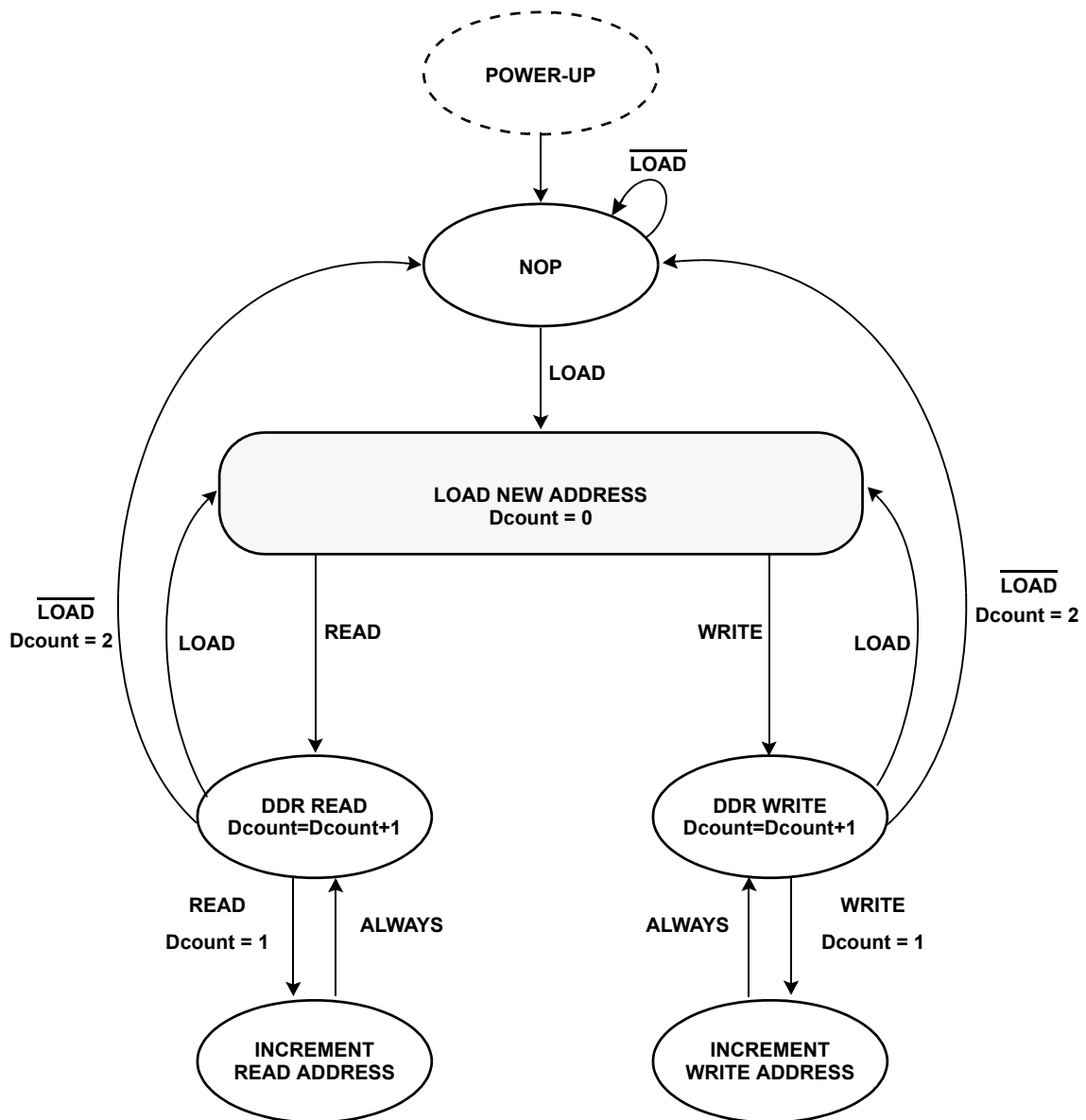
DEPTH EXPANSION

Each port can be selected and deselected independently with $\overline{R/\overline{W}}$ be shared among all SRAMs and provide a new \overline{LD} signal for each bank.
Before chip deselected, all read and write pending operations are completed.

LINEAR BURST SEQUENCE TABLE

| BURST SEQUENCE | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | SA ₁ | SA ₀ | SA ₁ | SA ₀ | SA ₁ | SA ₀ | SA ₁ | SA ₀ |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Fourth Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

STATE DIAGRAM



- Notes:
1. Internal burst counter is fixed as 4-bit linear, i.e. when first address is A0+0, next internal burst address is A0+1.
 2. "LOAD" refers to read new address active status with \overline{LD} =Low, "LOAD" refers to read new address inactive status with \overline{LD} =High.
 3. "READ" refers to read active read status with R/\overline{W} =High, "WRITE" refers to write active status with R/\overline{W} =Low

K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

| K | $\overline{\text{LD}}$ | R/ $\overline{\text{W}}$ | Q | | | | OPERATION |
|------------|------------------------|--------------------------|---|--|---|--|--------------|
| | | | Q(A0) | Q(A1) | Q(A2) | Q(A3) | |
| Stopped | X | X | Previous state | Previous state | Previous state | Previous state | Clock Stop |
| \uparrow | H | X | High-Z | High-Z | High-Z | High-Z | No Operation |
| \uparrow | L | H | Q _{OUT} at $\overline{\text{C}}(\text{t}+1)$ | Q _{OUT} at $\text{C}(\text{t}+2)$ | Q _{OUT} at $\overline{\text{C}}(\text{t}+2)$ | Q _{OUT} at $\text{C}(\text{t}+3)$ | Read |
| \uparrow | L | L | Din at K(t+1) | Din at $\overline{\text{K}}(\text{t}+1)$ | Din at K(t+2) | Din at $\overline{\text{K}}(\text{t}+2)$ | Write |

Notes: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (\uparrow).

3. Before enter into clock stop status, all pending read and write operations will be completed.

WRITE TRUTH TABLE(x18)

| K | $\overline{\text{K}}$ | $\overline{\text{BW}}_0$ | $\overline{\text{BW}}_1$ | OPERATION |
|------------|-----------------------|--------------------------|--------------------------|---|
| \uparrow | | L | L | WRITE ALL BYTES (K \uparrow) |
| | \uparrow | L | L | WRITE ALL BYTES ($\overline{\text{K}}\uparrow$) |
| \uparrow | | L | H | WRITE BYTE 0 (K \uparrow) |
| | \uparrow | L | H | WRITE BYTE 0 ($\overline{\text{K}}\uparrow$) |
| \uparrow | | H | L | WRITE BYTE 1 (K \uparrow) |
| | \uparrow | H | L | WRITE BYTE 1 ($\overline{\text{K}}\uparrow$) |
| \uparrow | | H | H | WRITE NOTHING (K \uparrow) |
| | \uparrow | H | H | WRITE NOTHING ($\overline{\text{K}}\uparrow$) |

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{\text{K}}$ (\uparrow).

3. Assumes a WRITE cycle was initiated.

4. This table illustrates operation for x18 devices.

WRITE TRUTH TABLE(x36)

| K | $\overline{\text{K}}$ | $\overline{\text{BW}}_0$ | $\overline{\text{BW}}_1$ | $\overline{\text{BW}}_2$ | $\overline{\text{BW}}_3$ | OPERATION |
|------------|-----------------------|--------------------------|--------------------------|--------------------------|--------------------------|---|
| \uparrow | | L | L | L | L | WRITE ALL BYTES (K \uparrow) |
| | \uparrow | L | L | L | L | WRITE ALL BYTES ($\overline{\text{K}}\uparrow$) |
| \uparrow | | L | H | H | H | WRITE BYTE 0 (K \uparrow) |
| | \uparrow | L | H | H | H | WRITE BYTE 0 ($\overline{\text{K}}\uparrow$) |
| \uparrow | | H | L | H | H | WRITE BYTE 1 (K \uparrow) |
| | \uparrow | H | L | H | H | WRITE BYTE 1 ($\overline{\text{K}}\uparrow$) |
| \uparrow | | H | H | L | L | WRITE BYTE 2 and BYTE 3 (K \uparrow) |
| | \uparrow | H | H | L | L | WRITE BYTE 2 and BYTE 3 ($\overline{\text{K}}\uparrow$) |
| \uparrow | | H | H | H | H | WRITE NOTHING (K \uparrow) |
| | \uparrow | H | H | H | H | WRITE NOTHING ($\overline{\text{K}}\uparrow$) |

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{\text{K}}$ (\uparrow).

3. Assumes a WRITE cycle was initiated.

www.DataSheet4U.com

K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|------------|-----------------|-----------|
| Voltage on VDD Supply Relative to VSS | VDD | -0.5 to 2.9 | V |
| Voltage on VDDQ Supply Relative to VSS | VDDQ | -0.5 to VDD | V |
| Voltage on Input Pin Relative to VSS | VIN | -0.5 to VDD+0.3 | V |
| Storage Temperature | TSTG | -65 to 150 | °C |
| Operating Temperature | Commercial | TOPR | 0 to 70 |
| | Industrial | TOPR | -40 to 85 |
| Storage Temperature Range Under Bias | TBIAS | -10 to 85 | °C |

*Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDDQ must not exceed VDD during normal operation.

DC ELECTRICAL CHARACTERISTICS(VDD=1.8V ±0.1V, TA=0°C to +70°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | MAX | UNIT | NOTE |
|-------------------------------|--------|---|-------------|-------------|------|------|
| Input Leakage Current | IIL | VDD=Max ; VIN=VSS to VDDQ | -2 | +2 | μA | |
| Output Leakage Current | IOL | Output Disabled, | -2 | +2 | μA | |
| Operating Current (x36) : DDR | ICC | VDD=Max , IOUT=0mA Cycle Time ≥ tKHKH Min | -30 | 550 | mA | 1,5 |
| | | | -25 | 500 | | |
| | | | -20 | 450 | | |
| | | | -16 | 400 | | |
| Operating Current (x18) : DDR | ICC | VDD=Max , IOUT=0mA Cycle Time ≥ tKHKH Min | -25 | 450 | mA | 1,5 |
| | | | -25 | 400 | | |
| | | | -20 | 350 | | |
| | | | -16 | 300 | | |
| Standby Current(NOP): DDR | ISB1 | Device deselected, IOUT=0mA, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V | -30 | 230 | mA | 1,6 |
| | | | -25 | 210 | | |
| | | | -20 | 190 | | |
| | | | -16 | 170 | | |
| Output High Voltage | VOH1 | | VDDQ/2-0.12 | VDDQ/2+0.12 | V | 2,7 |
| Output Low Voltage | VOL1 | | VDDQ/2-0.12 | VDDQ/2+0.12 | V | 3,7 |
| Output High Voltage | VOH2 | I _{OH} =-1.0mA | VDDQ-0.2 | VDDQ | V | 4 |
| Output Low Voltage | VOL2 | I _{OL} =1.0mA | VSS | 0.2 | V | 4 |
| Input Low Voltage | VIL | | -0.3 | VREF-0.1 | V | 8,9 |
| Input High Voltage | VIH | | VREF+0.1 | VDDQ+0.3 | V | 8,10 |

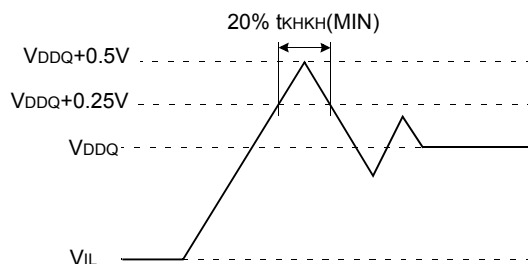
Notes: 1. Minimum cycle. IOUT=0mA.
2. $|I_{OH}| = (V_{DDQ}/2)/(R_Q/5) \pm 15\%$ for $175\Omega \leq R_Q \leq 350\Omega$.
3. $|I_{OL}| = (V_{DDQ}/2)/(R_Q/5) \pm 15\%$ for $175\Omega \leq R_Q \leq 350\Omega$.
4. Minimum Impedance Mode when ZQ pin is connected to VDDQ.
5. Operating current is calculated with 50% read cycles and 50% write cycles.
6. Standby Current is only after all pending read and write burst operations are completed.
7. Programmable Impedance Mode.
8. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.
9. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.5V(pulse width ≤ 3ns).
10. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=VDDQ+0.85V(pulse width ≤ 3ns).

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=1.8V \pm 0.1V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

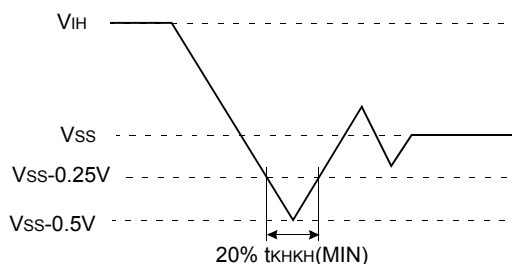
| PARAMETER | SYMBOL | MIN | MAX | UNIT | NOTES |
|--------------------|---------------|-----------------|-----------------|------|-------|
| Input High Voltage | V_{IH} (AC) | $V_{REF} + 0.2$ | - | V | 1,2 |
| Input Low Voltage | V_{IL} (AC) | - | $V_{REF} - 0.2$ | V | 1,2 |

Notes: 1. This condition is for AC function test only, not for AC parameter test.
2. To maintain a valid level, the transition edge of the input must:
a) Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$
b) Reach at least the target AC level
c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$

Overshoot Timing



Undershoot Timing



Note: For power-up, $V_{IH} \leq V_{DDQ} + 0.3V$ and $V_{DD} \leq 1.7V$ and $V_{DDQ} \leq 1.4V$ $t \leq 200ms$

OPERATING CONDITIONS ($0^{\circ}C \leq T_A \leq 70^{\circ}C$)

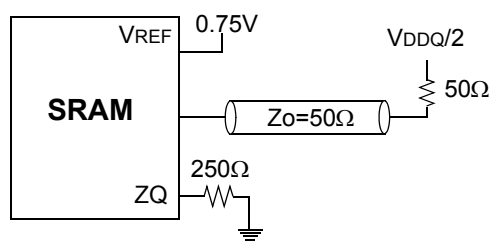
| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|-------------------|-----------|------|------|------|
| Supply Voltage | V_{DD} | 1.7 | 1.9 | V |
| | V_{DDQ} | 1.4 | 1.9 | V |
| Reference Voltage | V_{REF} | 0.68 | 0.95 | V |
| Ground | V_{SS} | 0 | 0 | V |

AC TEST CONDITIONS

| Parameter | Symbol | Value | Unit |
|-------------------------------|-----------------|-------------|------|
| Core Power Supply Voltage | V_{DD} | 1.7~1.9 | V |
| Output Power Supply Voltage | V_{DDQ} | 1.4~1.9 | V |
| Input High/Low Level | V_{IH}/V_{IL} | 1.25/0.25 | V |
| Input Reference Level | V_{REF} | 0.75 | V |
| Input Rise/Fall Time | T_R/T_F | 0.3/0.3 | ns |
| Output Timing Reference Level | | $V_{DDQ}/2$ | V |

Note: Parameters are tested with $R_Q=250\Omega$

AC TEST OUTPUT LOAD



AC TIMING CHARACTERISTICS(V_{DD}=1.8V±0.1V, T_A=0°C to +70°C)

| PARAMETER | SYMBOL | -30 | | -25 | | -20 | | -16 | | UNIT | NOTE |
|--|----------------------|-------|------|-------|------|-------|------|-------|------|-------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Clock | | | | | | | | | | | |
| Clock Cycle Time (K, \overline{K} , C, \overline{C}) | tKHKH | 3.30 | 8.40 | 4.00 | 8.40 | 5.00 | 8.40 | 6.00 | 8.40 | ns | |
| Clock Phase Jitter (K, \overline{K} , C, \overline{C}) | tKC var | | 0.20 | | 0.20 | | 0.20 | | 0.20 | ns | 5 |
| Clock High Time (K, \overline{K} , C, \overline{C}) | tKHKL | 1.32 | | 1.60 | | 2.00 | | 2.40 | | ns | |
| Clock Low Time (K, \overline{K} , C, \overline{C}) | tKLKH | 1.32 | | 1.60 | | 2.00 | | 2.40 | | ns | |
| Clock to $\overline{\text{Clock}}$ ($K\uparrow \rightarrow \overline{K}\uparrow$, $C\uparrow \rightarrow \overline{C}\uparrow$) | tKH \overline{K} H | 1.49 | | 1.80 | | 2.20 | | 2.70 | | ns | |
| Clock to data clock ($K\uparrow \rightarrow C\uparrow$, $\overline{K}\uparrow \rightarrow \overline{C}\uparrow$) | tKHCH | 0.00 | 1.45 | 0.00 | 1.80 | 0.00 | 2.30 | 0.00 | 2.80 | ns | |
| DLL Lock Time (K, C) | tKC lock | 1024 | | 1024 | | 1024 | | 1024 | | cycle | 6 |
| K Static to DLL reset | tKC reset | 30 | | 30 | | 30 | | 30 | | ns | |
| Output Times | | | | | | | | | | | |
| C, \overline{C} High to Output Valid | tCHQV | | 0.45 | | 0.45 | | 0.45 | | 0.50 | ns | 3 |
| C, \overline{C} High to Output Hold | tCHQX | -0.45 | | -0.45 | | -0.45 | | -0.50 | | ns | 3 |
| C, \overline{C} High to Echo Clock Valid | tCHCQV | | 0.45 | | 0.45 | | 0.45 | | 0.50 | ns | |
| C, \overline{C} High to Echo Clock Hold | tCHCQX | -0.45 | | -0.45 | | -0.45 | | -0.50 | | ns | |
| CQ, \overline{CQ} High to Output Valid | tCQHQV | | 0.27 | | 0.30 | | 0.35 | | 0.40 | ns | 7 |
| CQ, \overline{CQ} High to Output Hold | tCQHQX | -0.27 | | -0.30 | | -0.35 | | -0.40 | | ns | 7 |
| \overline{C} , High to Output High-Z | tCHQZ | | 0.45 | | 0.45 | | 0.45 | | 0.50 | ns | 3 |
| \overline{C} , High to Output Low-Z | tCHQX1 | -0.45 | | -0.45 | | -0.45 | | -0.50 | | ns | 3 |
| Setup Times | | | | | | | | | | | |
| Address valid to K rising edge | tAVKH | 0.40 | | 0.50 | | 0.60 | | 0.70 | | ns | |
| Control inputs valid to K rising edge | tIVKH | 0.40 | | 0.50 | | 0.60 | | 0.70 | | ns | 2 |
| Data-in valid to K, \overline{K} rising edge | tDVKH | 0.30 | | 0.35 | | 0.40 | | 0.50 | | ns | |
| Hold Times | | | | | | | | | | | |
| K rising edge to address hold | tKHAX | 0.40 | | 0.50 | | 0.60 | | 0.70 | | ns | |
| K rising edge to control inputs hold | tKHIX | 0.40 | | 0.50 | | 0.60 | | 0.70 | | ns | |
| K, \overline{K} rising edge to data-in hold | tKHDX | 0.30 | | 0.35 | | 0.40 | | 0.50 | | ns | |

- Notes:** 1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signal are \overline{R} and \overline{W} .
In case of BW₀, BW₁ (BW₂, BW₃, also for x36) signal follow the data setup/hold times.
3. If C, \overline{C} are tied high, K, \overline{K} become the references for C, \overline{C} timing parameters.
4. To avoid bus contention, at a given voltage and temperature t_{CHQX1} is bigger than t_{CHQZ}.
The specs as shown do not imply bus contention because t_{CHQX1} is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than t_{CHQZ}, which is a MAX parameter (worst case at 70°C, 1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. V_{dd} slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{dd} and input clock are stable.

K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

PIN CAPACITANCE

| PRMETER | SYMBOL | TESTCONDITION | Typ | MAX | Unit | NOTES |
|-----------------------------------|------------------|----------------------|-----|-----|------|-------|
| Address Control Input Capacitance | C _{IN} | V _{IN} =0V | 4 | 5 | pF | |
| Input and Output Capacitance | C _{OUT} | V _{OUT} =0V | 6 | 7 | pF | |
| Clock Capacitance | C _{CLK} | - | 5 | 6 | pF | |

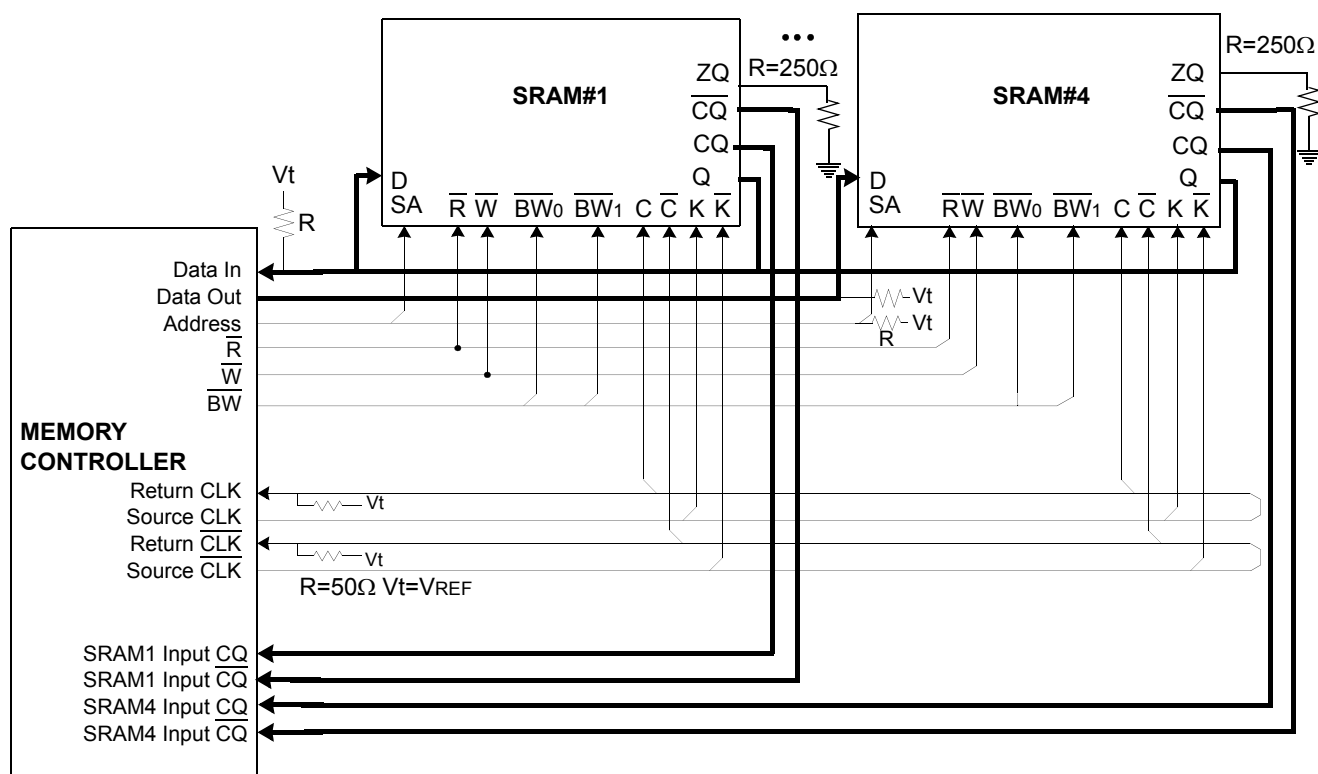
Note: 1. Parameters are tested with R_Q=250Ω and V_{DDQ}=1.5V.
2. Periodically sampled and not 100% tested.

THERMAL RESISTANCE

| PRMETER | SYMBOL | TYP | Unit | NOTES |
|---------------------|-----------------|------|------|-------|
| Junction to Ambient | θ _{JA} | 17.1 | °C/W | |
| Junction to Case | θ _{JC} | 3.3 | °C/W | |

Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J = T_A + P_D \times \theta_{JA}$

APPLICATION INFORMATION



512Kx36 & 1Mx18 DDRII CIO b4 SRAM

The diagram illustrates the timing characteristics of the K9F2G08U000 memory device across 12 clock cycles. The signals shown are:

- K**: Clock signal.
- \bar{K}** : Inverted clock signal.
- \bar{LD}** : Latch Enable signal.
- R/\bar{W}** : Read/Write control signal.
- SA**: Address bus signal.
- DQ**: Data bus signal.
- C**: Command Strobe signal.
- \bar{C}** : Inverted Command Strobe signal.
- CQ**: Command Latch Enable signal.
- \bar{CQ}** : Inverted Command Latch Enable signal.

The operations shown are:

- NOP** (No Operation) at cycles 1, 6, and 7.
- READ (burst of 4)** at cycles 2, 3, 4, and 5.
- WRITE (burst of 4)** at cycles 8, 9, 10, and 11.
- READ (burst of 4)** at cycles 12, 13, 14, and 15.

Key timing parameters and setup/hold times are indicated:

- Setup/Hold times for Address (SA):** t_{AVKH} (Address Valid to Clock High), $t_{KHAX'}$ (Clock High to Address X' Valid), $t_{KHX'}$ (Clock High to Address X' Invalid).
- Setup/Hold times for Data (DQ):** t_{KHCH} (Clock High to Data Valid), t_{CHQV} (Data Valid to Clock High), t_{CHQX} (Data Invalid to Clock High), t_{CQHX} (Data Invalid to Clock High), t_{CQHV} (Data Valid to Clock High), t_{CQHZ} (Data Invalid to Clock High).
- Setup/Hold times for Command (C):** t_{KHCH} (Clock High to Command Valid), t_{KHKL} (Clock High to Command Latch Enable Valid), t_{KLKH} (Command Latch Enable Valid to Clock High), t_{KHKH} (Clock High to Command Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Invalid).
- Setup/Hold times for Command Latch Enable (CQ):** t_{KHCH} (Clock High to Command Latch Enable Valid), t_{KHKL} (Clock High to Command Latch Enable Valid), t_{KLKH} (Command Latch Enable Valid to Clock High), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid).
- Setup/Hold times for Command Latch Enable (CQ):** t_{KHCH} (Clock High to Command Latch Enable Valid), t_{KHKL} (Clock High to Command Latch Enable Valid), t_{KLKH} (Command Latch Enable Valid to Clock High), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid).
- Setup/Hold times for Command Latch Enable (CQ):** t_{KHCH} (Clock High to Command Latch Enable Valid), t_{KHKL} (Clock High to Command Latch Enable Valid), t_{KLKH} (Command Latch Enable Valid to Clock High), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid), t_{KHKH} (Clock High to Command Latch Enable Invalid).

Legend:

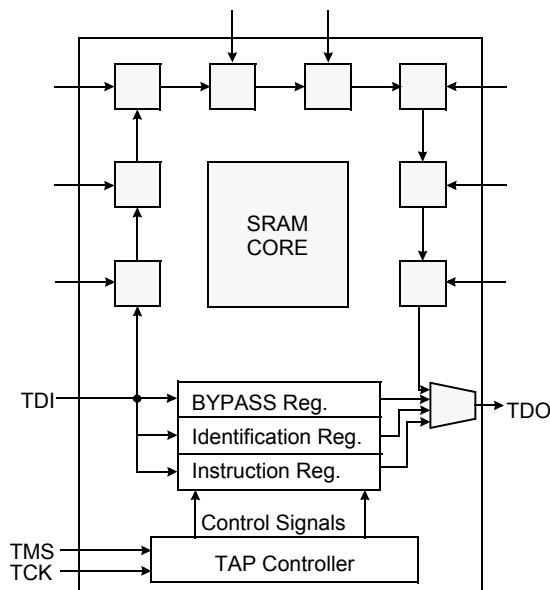
- DON'T CARE
- UNDEFINED

1. Q₀₁ refers to output from address A. Q₀₂ refers to output from the next internal burst address following A, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies, it may be required to prevent bus contention.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG BLOCK DIAGRAM



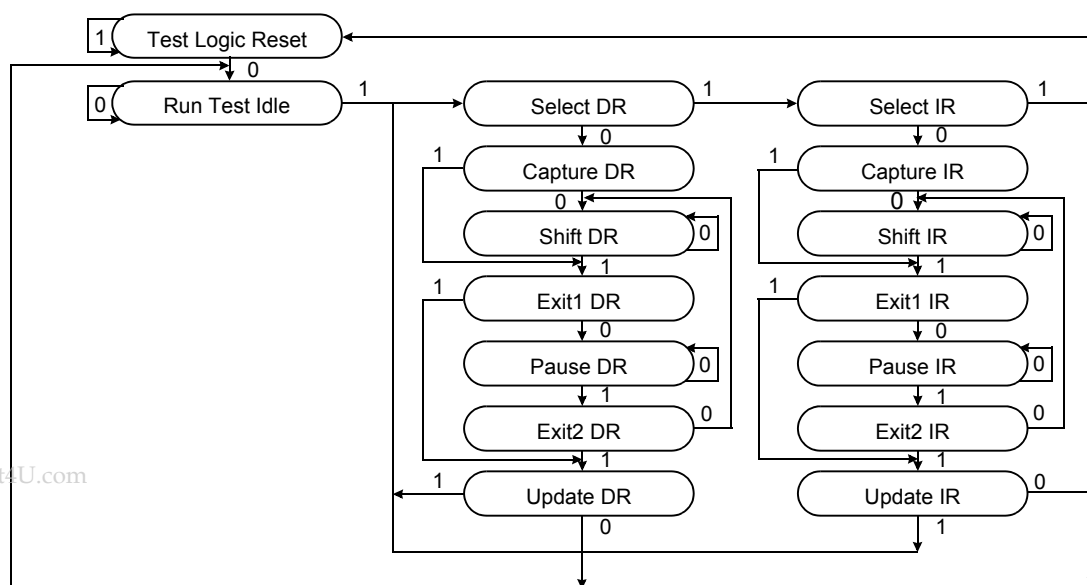
JTAG INSTRUCTION CODING

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|-----|-----|-----|-------------|-------------------------|-------|
| 0 | 0 | 0 | EXTEST | Boundary Scan Register | 1 |
| 0 | 0 | 1 | IDCODE | Identification Register | 3 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 2 |
| 0 | 1 | 1 | RESERVED | Do Not Use | 6 |
| 1 | 0 | 0 | SAMPLE | Boundary Scan Register | 5 |
| 1 | 0 | 1 | RESERVED | Do Not Use | 6 |
| 1 | 1 | 0 | RESERVED | Do Not Use | 6 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 4 |

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP CONTROLLER STATE DIAGRAM



K7I163684B K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

SCAN REGISTER DEFINITION

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---------|----------------------|-----------------|-------------|---------------|
| 512Kx36 | 3 bits | 1 bit | 32 bits | 107 bits |
| 1Mx18 | 3 bits | 1 bit | 32 bits | 107 bits |

ID REGISTER DEFINITION

| Part | Revision Number (31:29) | Part Configuration (28:12) | Samsung JEDEC Code (11: 1) | Start Bit(0) |
|---------|----------------------------|-------------------------------|-------------------------------|--------------|
| 512Kx36 | 000 | 00def0wx0t0q0b0s0 | 00001001110 | 1 |
| 1Mx18 | 000 | 00def0wx0t0q0b0s0 | 00001001110 | 1 |

Note : Part Configuration

/def=001 for 18Mb, /wx=11 for x36, 10 for x18

/t=1 for DLL Ver., 0 for non-DLL Ver. /q=1 for QDR, 0 for DDR /b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

BOUNDARY SCAN EXIT ORDER

| ORDER | PIN ID |
|-------|--------|
| 1 | 6R |
| 2 | 6P |
| 3 | 6N |
| 4 | 7P |
| 5 | 7N |
| 6 | 7R |
| 7 | 8R |
| 8 | 8P |
| 9 | 9R |
| 10 | 11P |
| 11 | 10P |
| 12 | 10N |
| 13 | 9P |
| 14 | 10M |
| 15 | 11N |
| 16 | 9M |
| 17 | 9N |
| 18 | 11L |
| 19 | 11M |
| 20 | 9L |
| 21 | 10L |
| 22 | 11K |
| 23 | 10K |
| 24 | 9J |
| 25 | 9K |
| 26 | 10J |
| 27 | 11J |
| 28 | 11H |
| 29 | 10G |
| 30 | 9G |
| 31 | 11F |
| 32 | 11G |
| 33 | 9F |
| 34 | 10F |
| 35 | 11E |
| 36 | 10E |

| ORDER | PIN ID |
|-------|----------|
| 37 | 10D |
| 38 | 9E |
| 39 | 10C |
| 40 | 11D |
| 41 | 9C |
| 42 | 9D |
| 43 | 11B |
| 44 | 11C |
| 45 | 9B |
| 46 | 10B |
| 47 | 11A |
| 48 | Internal |
| 49 | 9A |
| 50 | 8B |
| 51 | 7C |
| 52 | 6C |
| 53 | 8A |
| 54 | 7A |
| 55 | 7B |
| 56 | 6B |
| 57 | 6A |
| 58 | 5B |
| 59 | 5A |
| 60 | 4A |
| 61 | 5C |
| 62 | 4B |
| 63 | 3A |
| 64 | 1H |
| 65 | 1A |
| 66 | 2B |
| 67 | 3B |
| 68 | 1C |
| 69 | 1B |
| 70 | 3D |
| 71 | 3C |
| 72 | 1D |

| ORDER | PIN ID |
|-------|--------|
| 73 | 2C |
| 74 | 3E |
| 75 | 2D |
| 76 | 2E |
| 77 | 1E |
| 78 | 2F |
| 79 | 3F |
| 80 | 1G |
| 81 | 1F |
| 82 | 3G |
| 83 | 2G |
| 84 | 1J |
| 85 | 2J |
| 86 | 3K |
| 87 | 3J |
| 88 | 2K |
| 89 | 1K |
| 90 | 2L |
| 91 | 3L |
| 92 | 1M |
| 93 | 1L |
| 94 | 3N |
| 95 | 3M |
| 96 | 1N |
| 97 | 2M |
| 98 | 3P |
| 99 | 2N |
| 100 | 2P |
| 101 | 1P |
| 102 | 3R |
| 103 | 4R |
| 104 | 4P |
| 105 | 5P |
| 106 | 5N |
| 107 | 5R |

Note: 1. NC pins are read as "X" (i.e. don't care.)

JTAG DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-----------------|-----------------|-----|----------------------|------|------|
| Power Supply Voltage | V _{DD} | 1.7 | 1.8 | 1.9 | V | |
| Input High Level | V _{IH} | 1.3 | - | V _{DD} +0.3 | V | |
| Input Low Level | V _{IL} | -0.3 | - | 0.5 | V | |
| Output High Voltage(I _{OH} =-2mA) | V _{OH} | 1.4 | - | V _{DD} | V | |
| Output Low Voltage(I _{OL} =2mA) | V _{OL} | V _{SS} | - | 0.4 | V | |

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

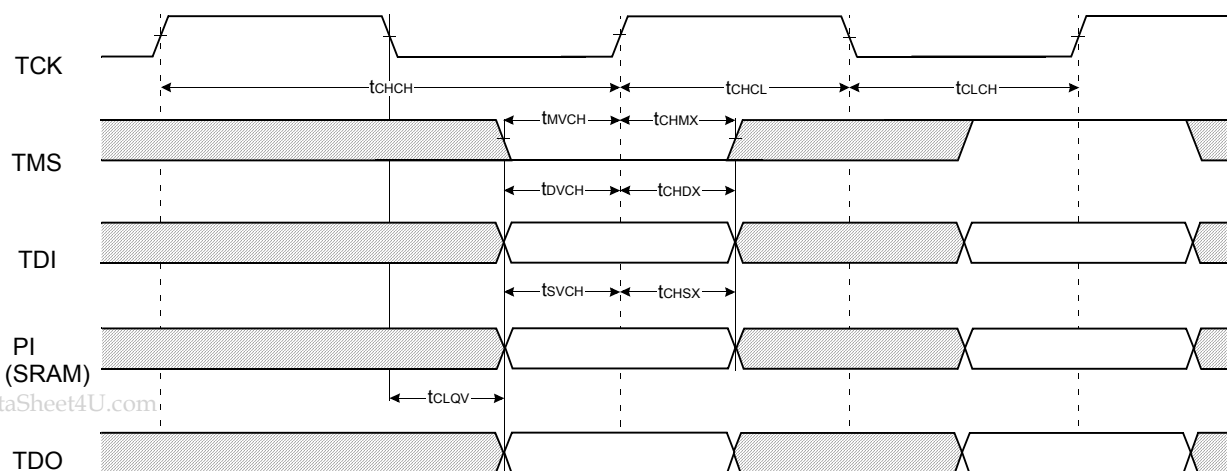
| Parameter | Symbol | Min | Unit | Note |
|---|----------------------------------|---------|------|------|
| Input High/Low Level | V _{IH} /V _{IL} | 1.8/0.0 | V | |
| Input Rise/Fall Time | TR/TF | 1.0/1.0 | ns | |
| Input and Output Timing Reference Level | | 0.9 | V | 1 |

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

| Parameter | Symbol | Min | Max | Unit | Note |
|---------------------------|-------------------|-----|-----|------|------|
| TCK Cycle Time | t _{CHCH} | 50 | - | ns | |
| TCK High Pulse Width | t _{CHCL} | 20 | - | ns | |
| TCK Low Pulse Width | t _{CLCH} | 20 | - | ns | |
| TMS Input Setup Time | t _{MVCH} | 5 | - | ns | |
| TMS Input Hold Time | t _{CHMX} | 5 | - | ns | |
| TDI Input Setup Time | t _{DVCH} | 5 | - | ns | |
| TDI Input Hold Time | t _{CHDX} | 5 | - | ns | |
| SRAM Input Setup Time | t _{SVCH} | 5 | - | ns | |
| SRAM Input Hold Time | t _{CHSX} | 5 | - | ns | |
| Clock Low to Output Valid | t _{CLQV} | 0 | 10 | ns | |

JTAG TIMING DIAGRAM



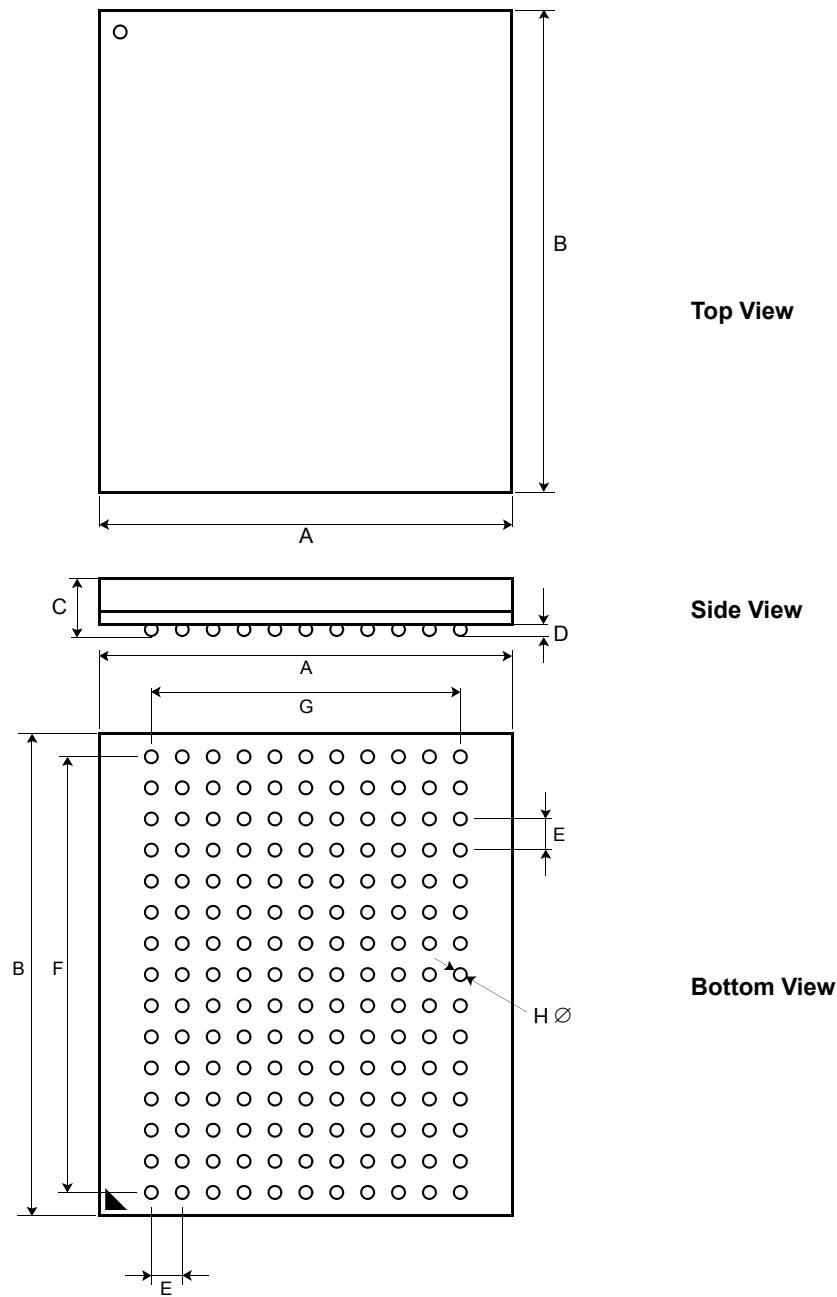
www.DataSheet4U.com

K7I163684B
K7I161884B

512Kx36 & 1Mx18 DDRII CIO b4 SRAM

165 FBGA PACKAGE DIMENSIONS

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



| Symbol | Value | Units | Note | Symbol | Value | Units | Note |
|--------|-----------------|-------|------|--------|----------------|-------|------|
| A | 13 ± 0.1 | mm | | E | 1.0 | mm | |
| B | 15 ± 0.1 | mm | | F | 14.0 | mm | |
| C | 1.3 ± 0.1 | mm | | G | 10.0 | mm | |
| D | 0.35 ± 0.05 | mm | | H | 0.5 ± 0.05 | mm | |