Document Title

1Mx36 & 2Mx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial draft	May. 10. 2001	Advance
0.1	1. Add 165FBGA package	Aug. 29. 2001	Preliminary
0.2	1. Update JTAG scan order	Dec. 03. 2001	Preliminary
0.3	1. Change pin out for 165FBGA - x18/x36 ; 11B => from A to NC , 2R ==> from NC to A .	Feb. 14 . 2002	Preliminary
0.4	1. Insert pin at JTAG scan order of 165FBGA in connection with pin out change - x18/x36 ; insert Pin ID of 2R to $\overline{\text{BIT}}$ number of 69	Apr. 20. 2002	Preliminary
0.5	1. Add Icc, Isb, Isb1 and Isb2 values.	May. 10. 2002	Preliminary
1.0	1. Correct the pin name of 100TQFP.	Oct. 15. 2002	Final
1.1	1. Change the Stand-by current (Isb) Before After Isb - 65 : 100 140 - 75 : 90 130 - 85 : 80 130 Isb1 : 90 110 Isb2 : 80 100	Oct. 17, 2003	Final
2.0	1. Delete the 119BGA and 165FBGA package. 2. Delete the 8.5ns speed bin	Nov. 18, 2003	Final

32Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
2Mx18	K7B321825M-QC65/75	SB	3.3	6.5/7.5ns	Q: 100TQFP	C ; Commercial Temp.Range I ; Industrial Temp.Range
	K7A321800M-QC(I)25/20/14	SPB(2E1D)	3.3	250/200/138MHz		
1Mx36	K7B323625M-Q)C65/75	SB	3.3	6.5/7.5ns		
	K7A323600M-QC(I)25/20/14	SPB(2E1D)	3.3	250/200/138MHz		

1Mx36 & 2Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package

FAST ACCESS TIMES

PARAMETER	Symbol	-65	-75	Unit
Cycle Time	t_{CYC}	7.5	8.5	ns
Clock Access Time	t_{CD}	6.5	7.5	ns
Output Enable Access Time	t_{OE}	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B323625M and K7B321825M are 37,748,736-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 1M(2M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with $\overline{CS_1}$ high, ADSP is blocked to control signals.

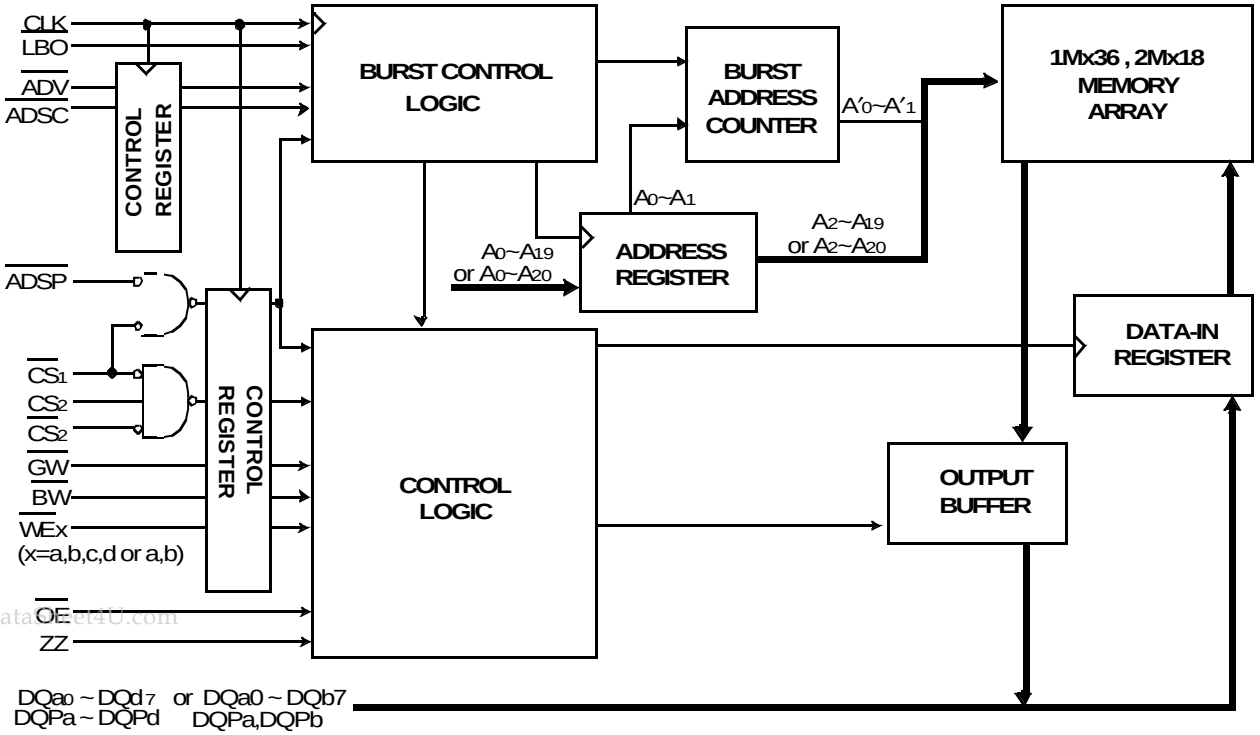
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

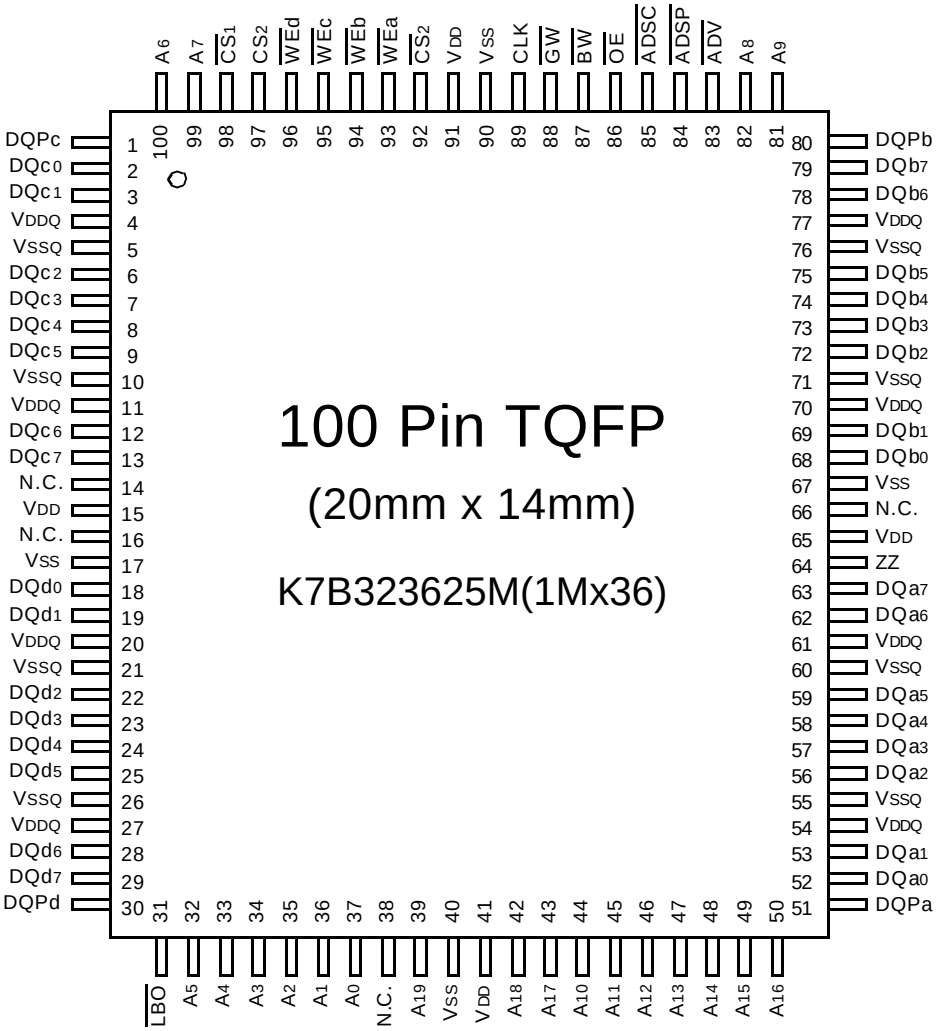
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B323625M and K7B321825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

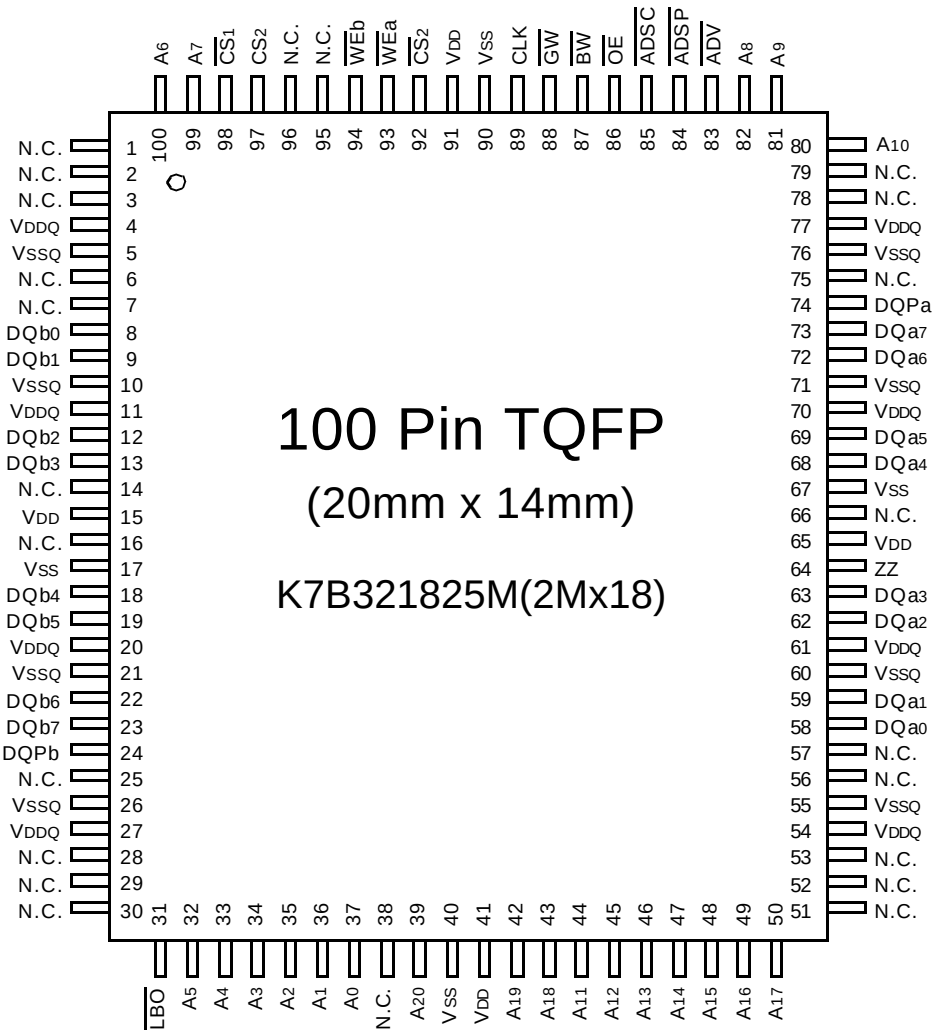


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,39 42,43,44,45,46,47,48, 49,50,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	$DQa_{0\sim a7}$	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{CLK}$	Clock	89	$DQb_{0\sim b7}$		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	$DQc_{0\sim c7}$		2,3,6,7,8,9,12,13
$\overline{CS_2}$	Chip Select	97	$DQd_{0\sim d7}$		18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	$DQPa\sim Pd$		51,80,1,30
$\overline{WE}$x(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{20}	Address Inputs	32,33,34,35,36,37,39 42,43,44,45,46,47,48, 49,50 80,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,51,52,53,56,57,66, 75,78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
$\overline{CLK}$	Clock	89	DQa_0 ~ a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb_0 ~ b_7		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92			
$\overline{WE}$x(x=a,b)	Byte Write Inputs	93,94	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

FUNCTION DESCRIPTION

The K7B323625M and K7B321825M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B163625M, a 512Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS_1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Notes :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

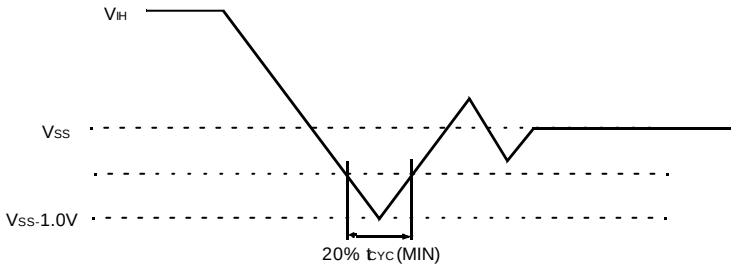
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note :** Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	µA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL}, Cycle Time ≥ t_{CYC} Min	-65	-	310	mA	1,2
			-75	-	290		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-65	-	140	mA	
			-75	-	130		
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or		-	110	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	100	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

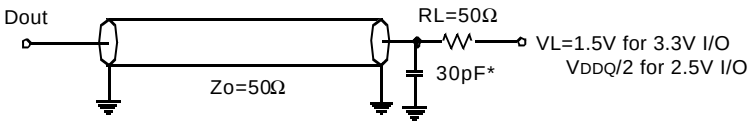


TEST CONDITIONS

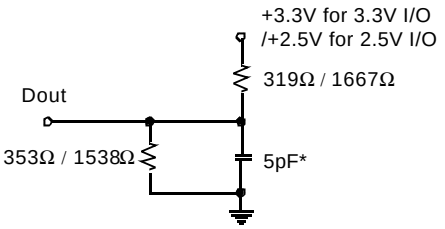
(V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=3.3V+0.165/-0.165V or V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



Output Load(B),
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

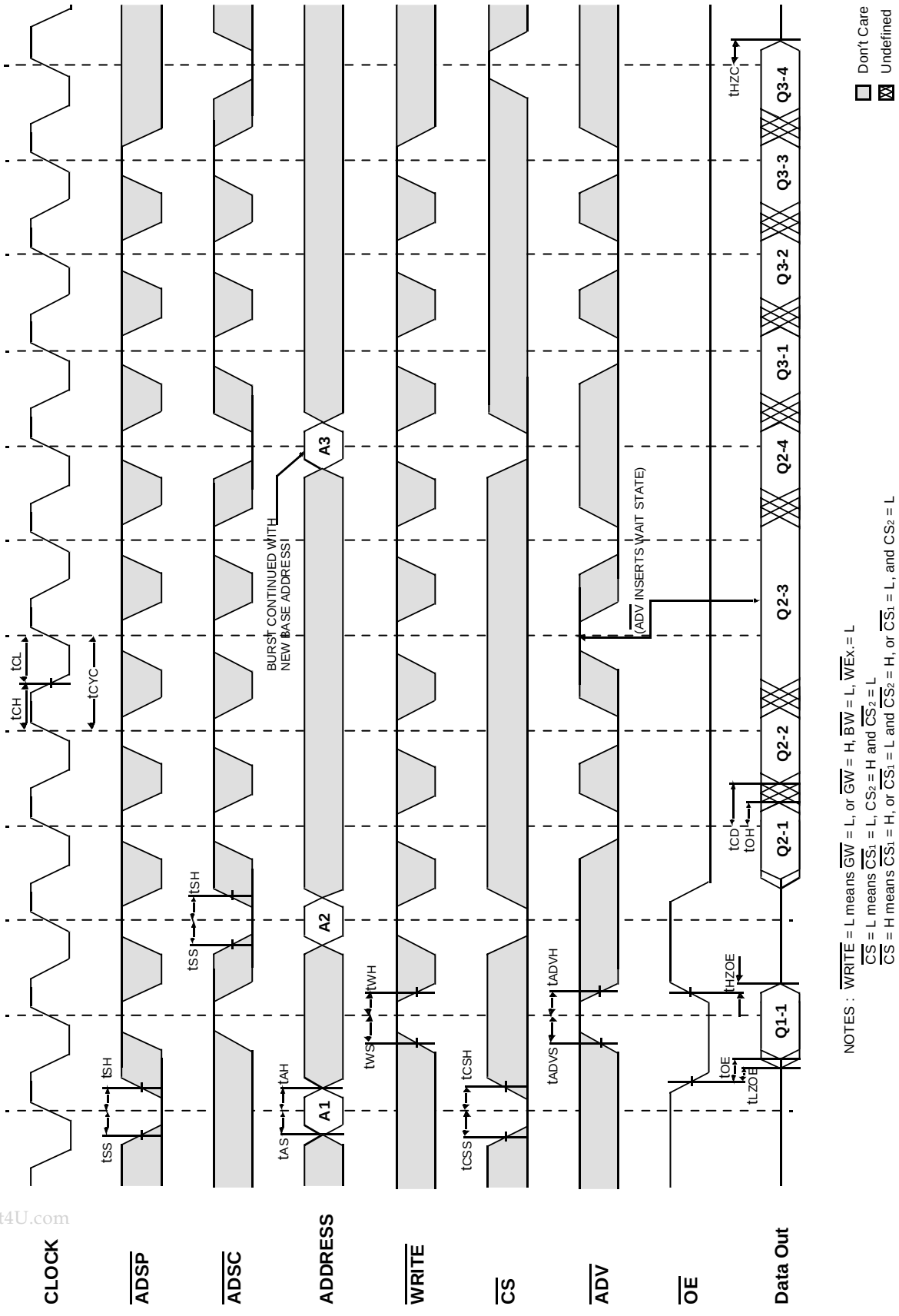
Fig. 1

AC TIMING CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	-65		-75		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tCYC	7.5	-	8.5	-	ns
Clock Access Time	tCD	-	6.5	-	7.5	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.5	ns
Clock High to Output Low-Z	tLZC	2.5	-	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	ns
Clock High to Output High-Z	tHZC	-	3.8	-	4.0	ns
Clock High Pulse Width	tCH	2.2	-	2.5	-	ns
Clock Low Pulse Width	tCL	2.2	-	2.5	-	ns
Address Setup to Clock High	tAS	1.5	-	2.0	-	ns
Address Status Setup to Clock High	tSS	1.5	-	2.0	-	ns
Data Setup to Clock High	tDS	1.5	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	1.5	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

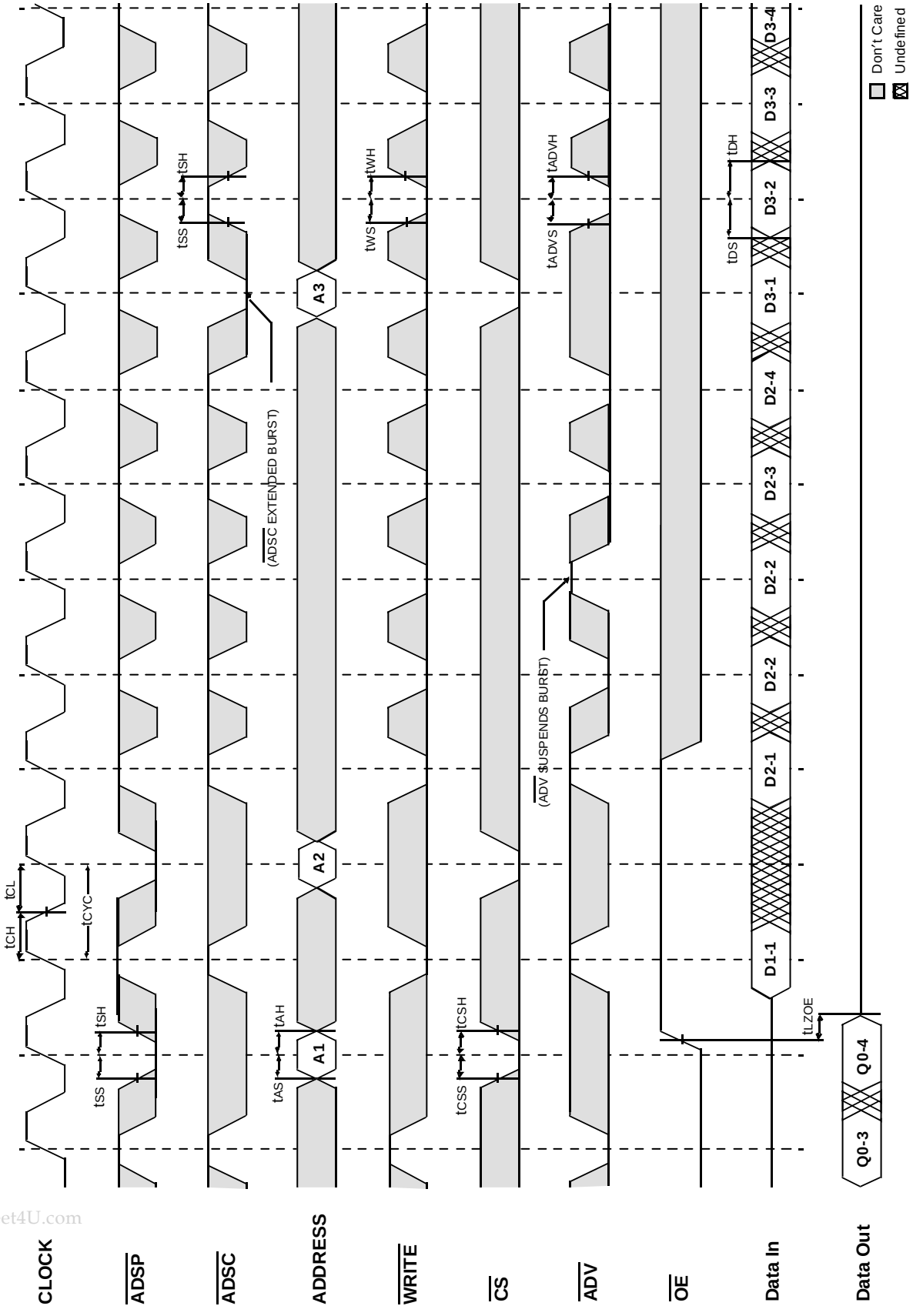
Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE

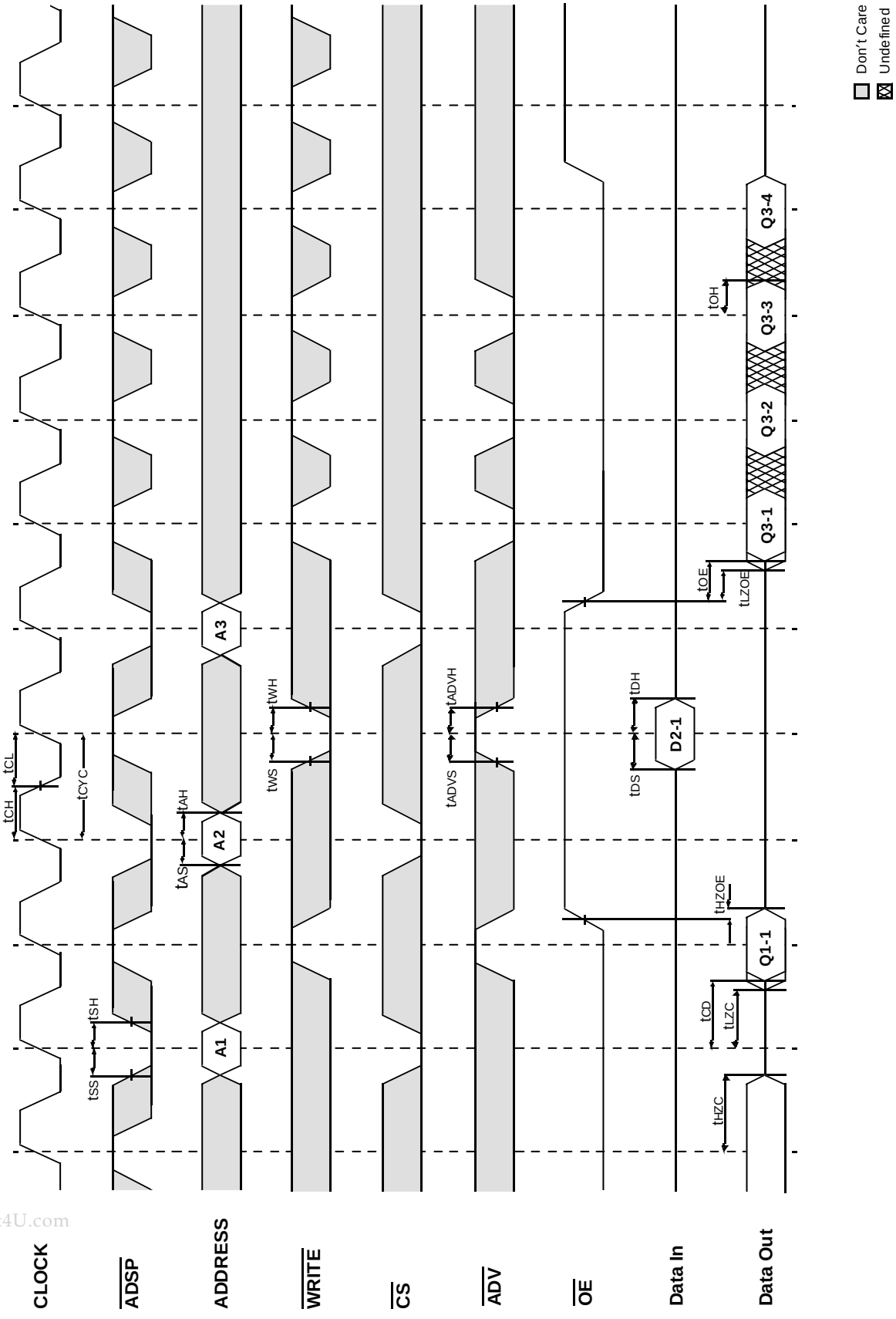


NOTES : WRITE = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L

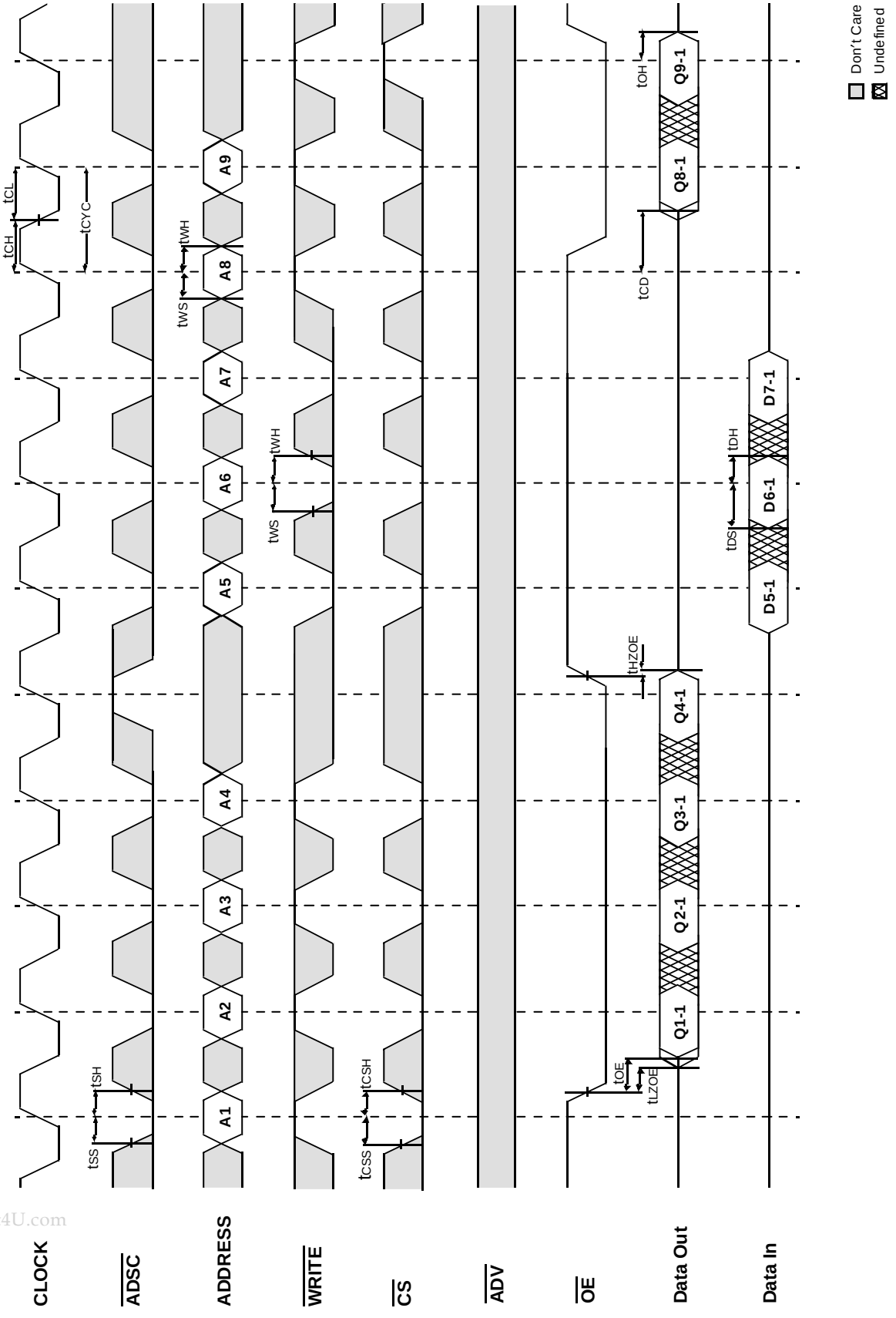
TIMING WAVEFORM OF WRTE CYCLE



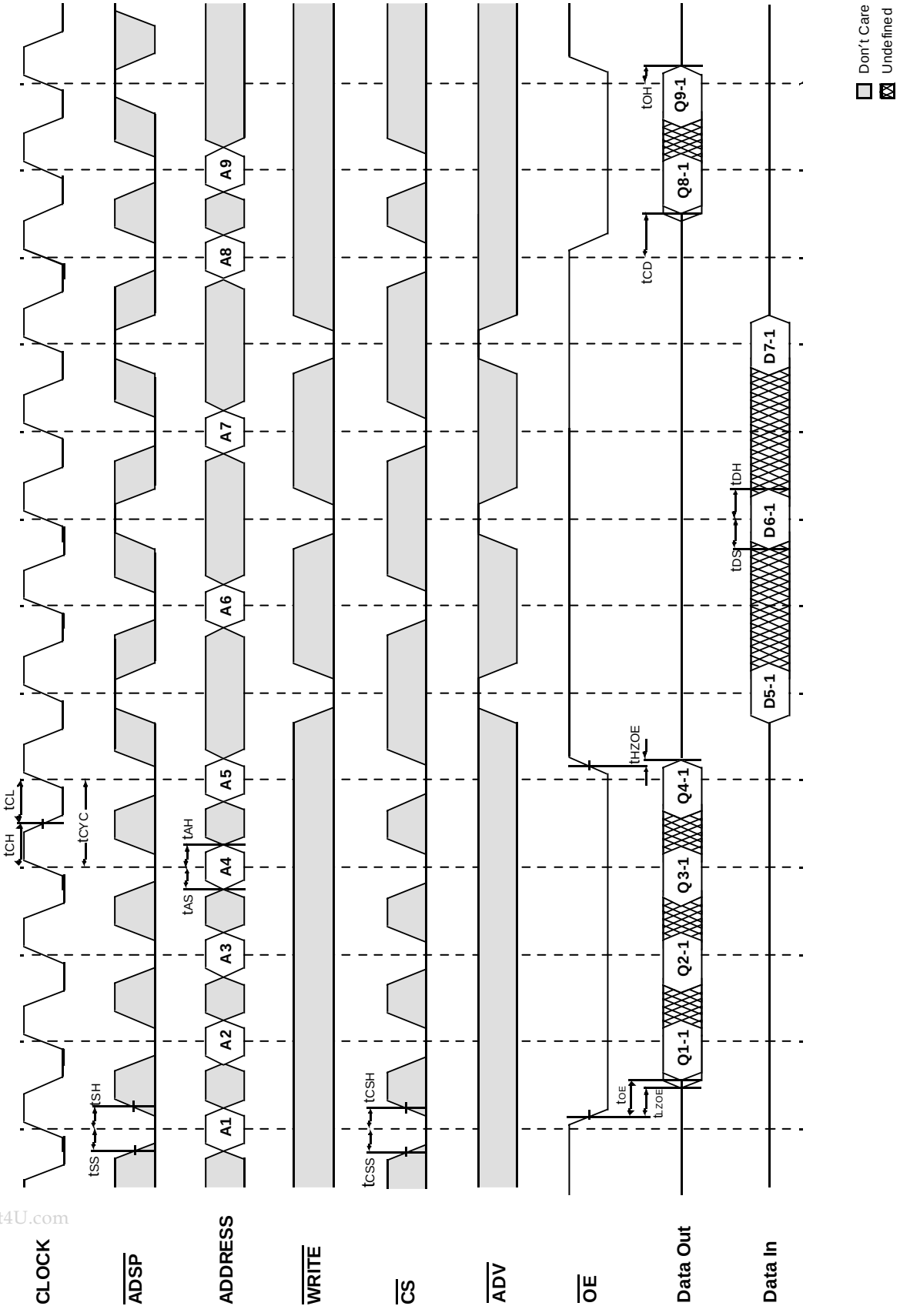
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



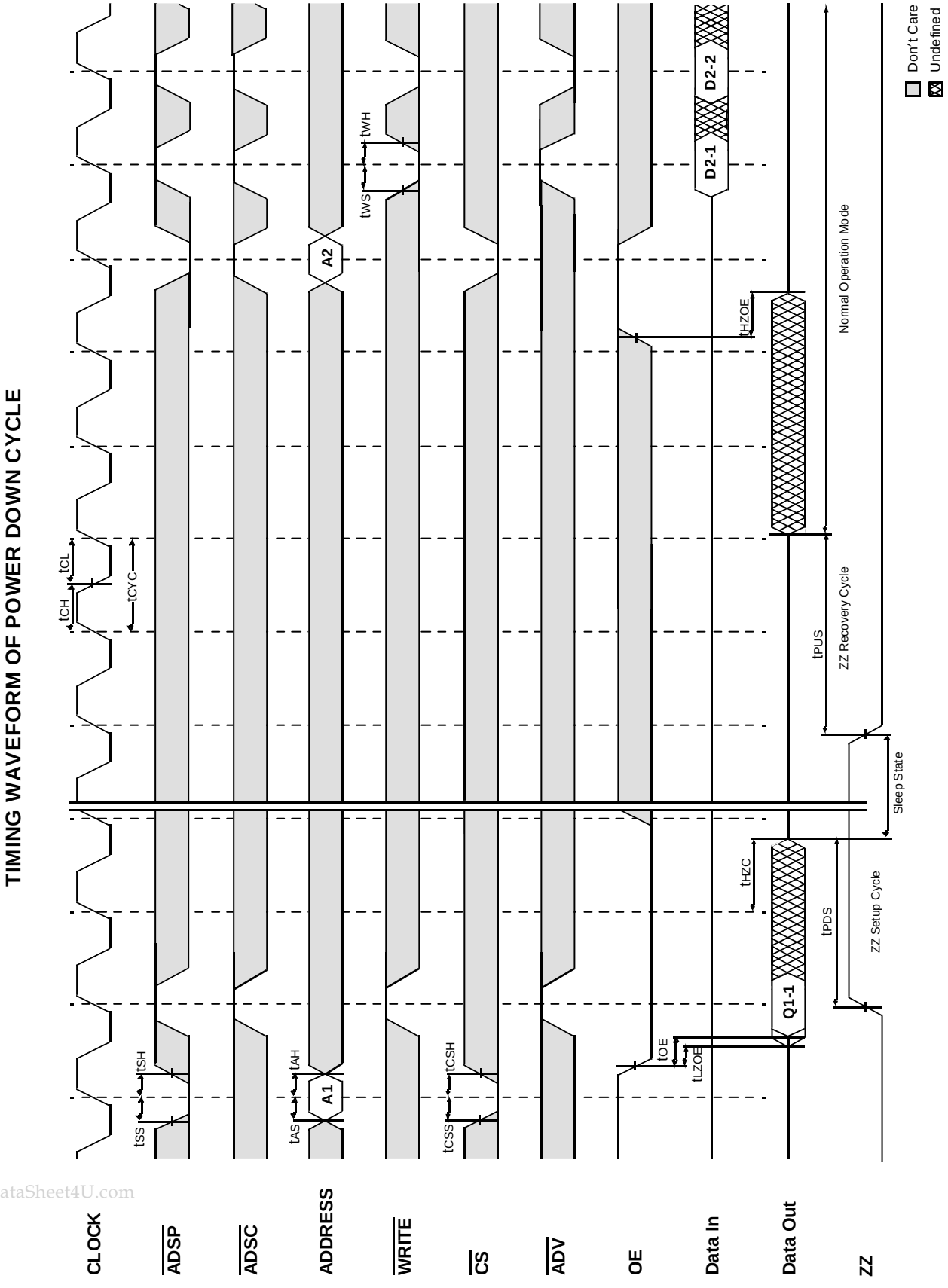
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



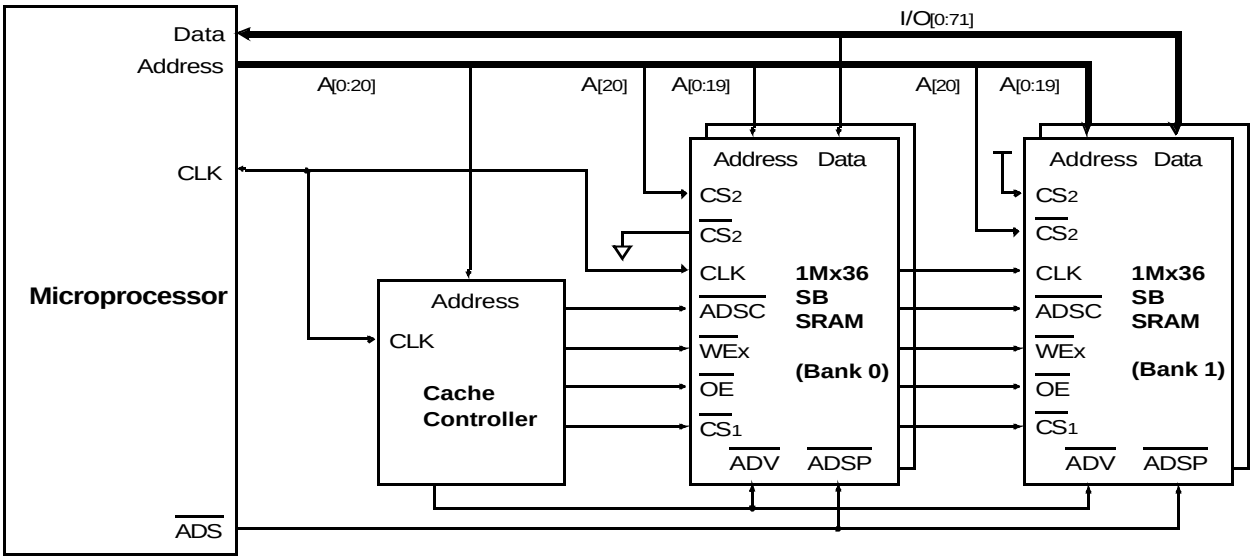
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

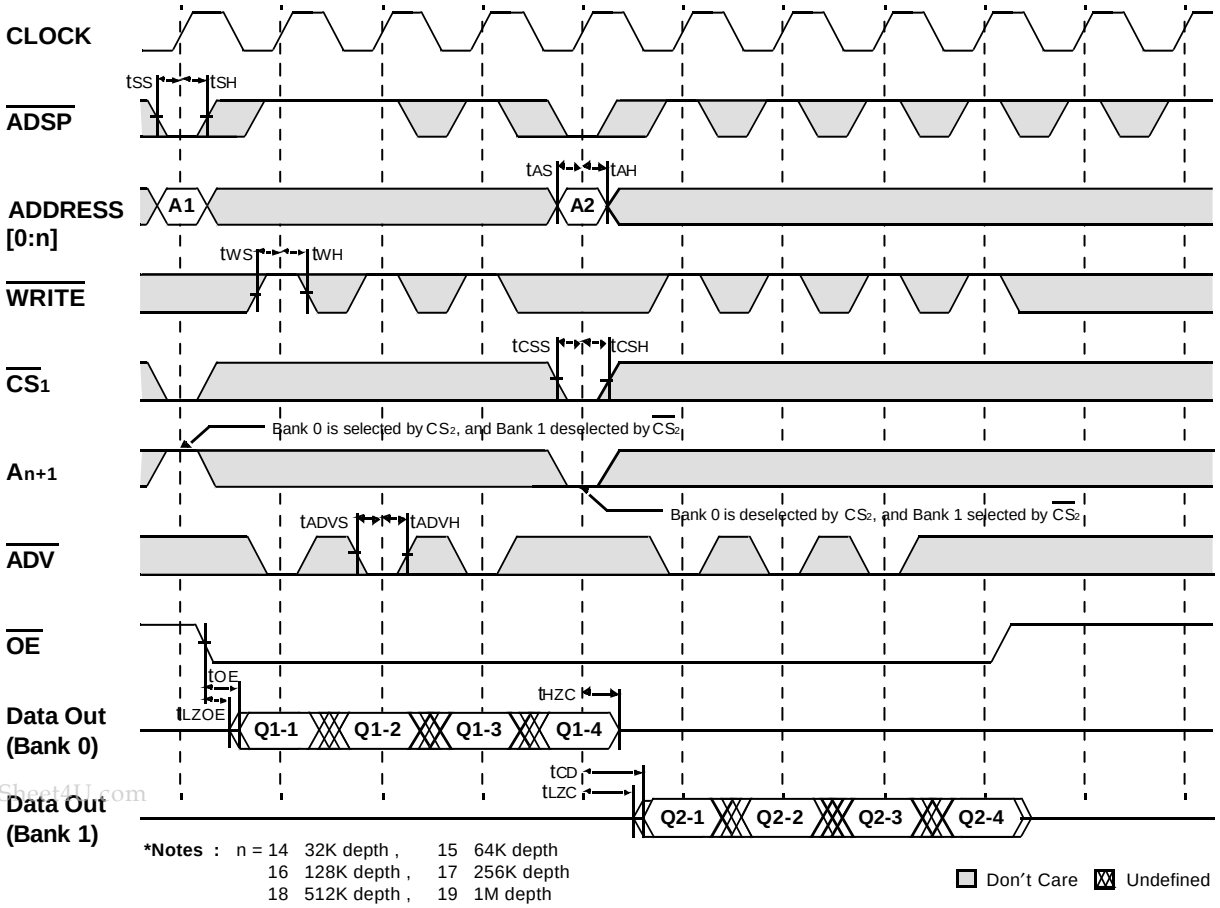
DEPTH EXPANSION

The Samsung 1Mx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)



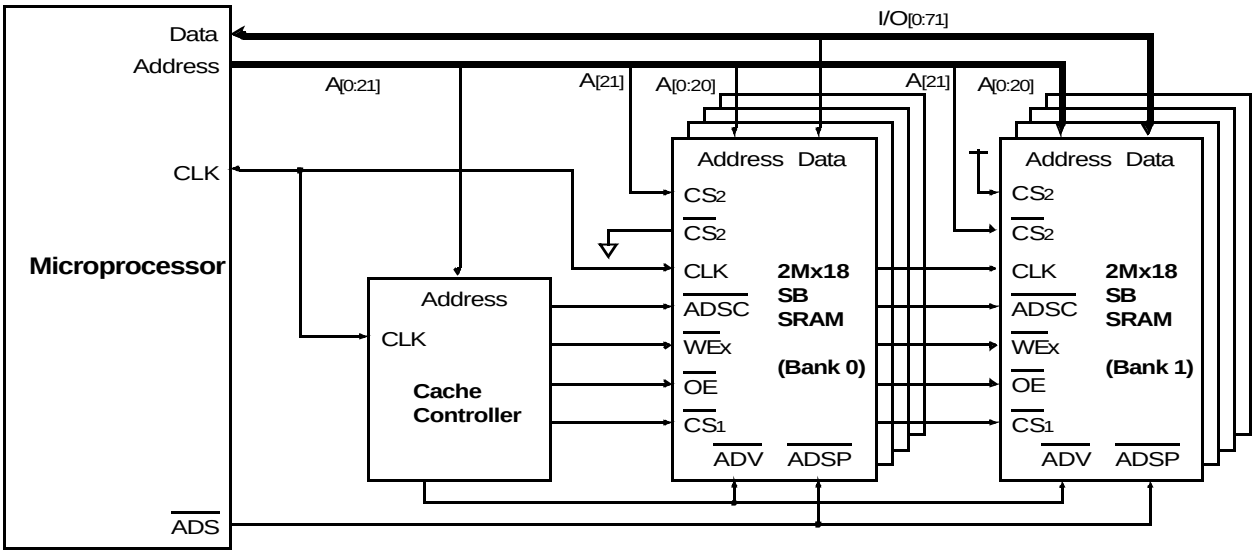
***Notes :** n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

Don't Care Undefined

APPLICATION INFORMATION

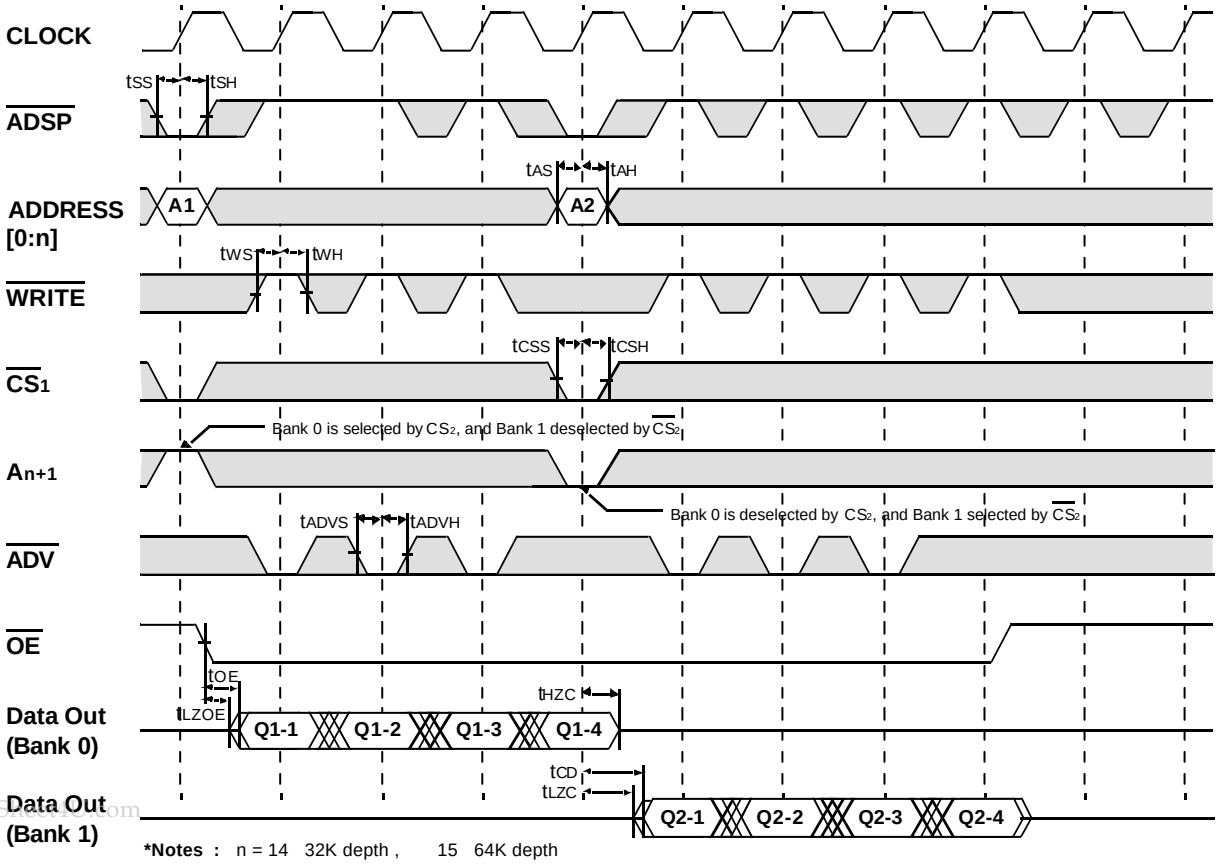
DEPTH EXPANSION

The Samsung 2Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 2M depth to 4M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



***Notes :** n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth
20 2M depth

Don't Care Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units ; millimeters/Inches