64M-Bit (4Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
  4,194,304 x 16(word mode)
- Fast access time
  3.3V Operation : 100ns(Max.)@C_L=50pF,
  120ns(Max.)@C_L=100pF
  3.0V Operation : 120ns(Max.)@C_L=100pF
- Supply voltage : single +3.3V/ single +3.0V
- Current consumption
  Operating : 40mA(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
  -. K3N7V(U)4000C-DC: 42-DIP-600

GENERAL DESCRIPTION

The K3N7V(U)4000C-DC is a fully static mask programmable ROM organized 4,194,304x16 bit. It is fabricated using silicon-gate CMOS process technology.

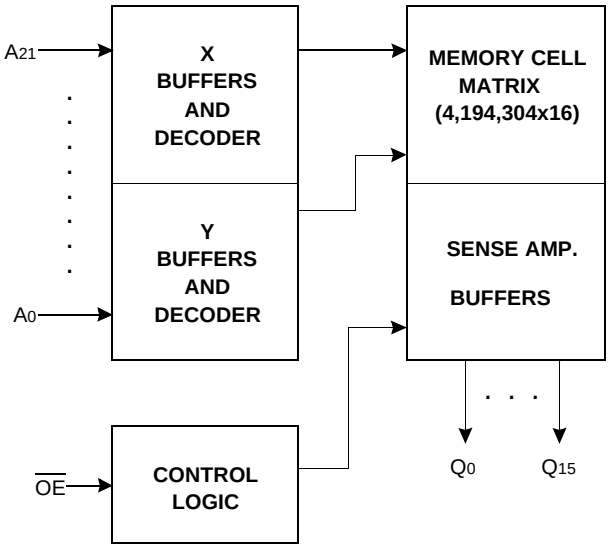
This device operates with a low power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

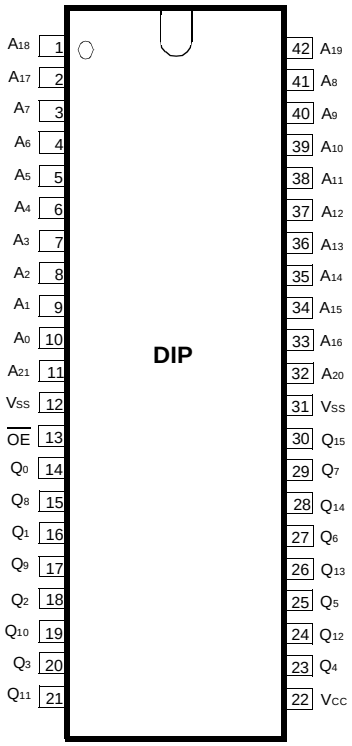
The K3N7V(U)4000C-DC is packaged in a 42-DIP.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_{21}	Address Inputs
Q_0 - Q_{15}	Data Outputs
$\overline{OE}$	Output Enable
V_{CC}	Power
V_{SS}	Ground

PIN CONFIGURATION



K3N7V(U)4000C-DC

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to +4.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7/3.0	3.0/3.3	3.3/3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}	Cycle=5MHz, all outputs open, $\overline{CE}$=$\overline{OE}$=V_{IL}, V_{IN}=0.45V to 2.4V (AC Test Condition)	Vcc=3.3V±0.3V	-	40	mA
			Vcc=3.0V±0.3V	-	35	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		-	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		-	10	µA
Input High Voltage, All Inputs	V_{IH}			2.0	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.6	V
Output High Voltage Level	V_{OH}	I_{OH}=-400µA		2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

$\overline{OE}$	Mode	Data	Power
H	Operating	High-Z	Active
L	Operating	Q_0~Q_{15} : Dout	Active

CAPACITANCE(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0°C to +70°C, V_{CC}=3.3V/3.0V±0.3V, unless otherwise noted.)

TEST CONDITIONS

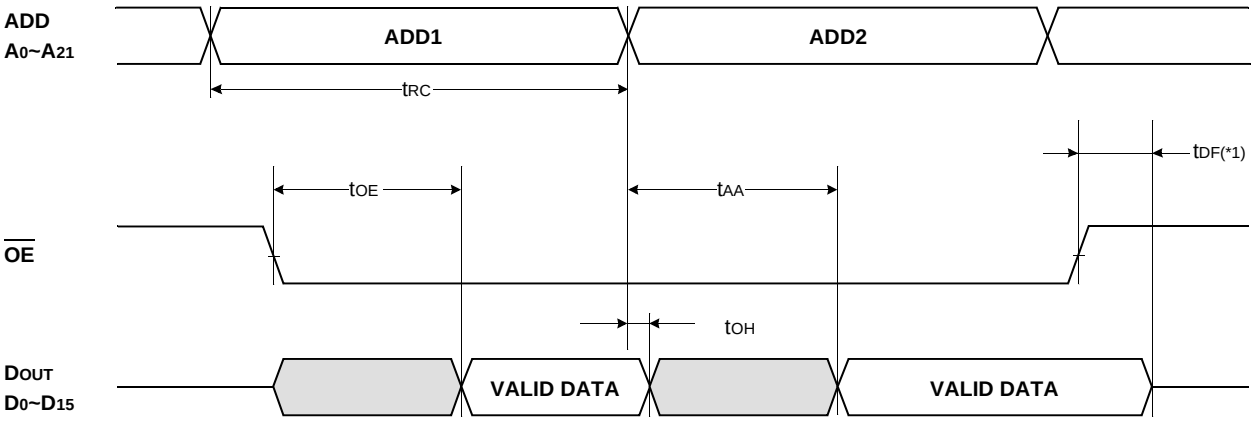
Item	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=50pF or 100pF

READ CYCLE

Item	Symbol	K3N7V4000C-DC10 (C_L=50pF)		K3N7V4000C-DC12 (C_L=100pF)		K3N7U4000C-DC12 (C_L=100pF)		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		120		ns
Address Access Time	t_{AA}		100		120		120	ns
Output Enable Access Time	t_{OE}		50		60		60	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



NOTES :

*1. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.