

2SK1611

Silicon N-Channel Power F-MOS FET

■ Features

- High avalanche energy capacity
- V_{GS} : 30V guaranteed
- Low $R_{DS(on)}$, high-speed switching characteristic

■ Applications

- High-speed switching (switching power supply, AC adaptor)
- For high-frequency power amplification

■ Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$)

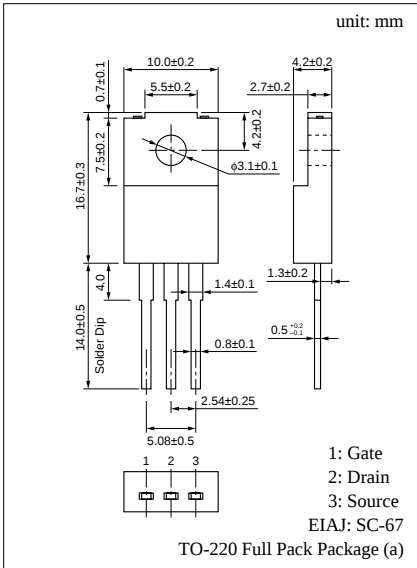
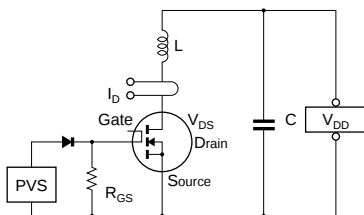
Parameter	Symbol	Ratings	Unit
Drain to Source breakdown voltage	V_{DSS}	800	V
Gate to Source voltage	V_{GSS}	± 30	V
Drain current	DC	I_D	A
	Pulse	I_{DP}	A
Avalanche energy capacity	EAS*	20	mJ
Allowable power dissipation	$T_C = 25^\circ\text{C}$	P_D	50
	$T_a = 25^\circ\text{C}$		2
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

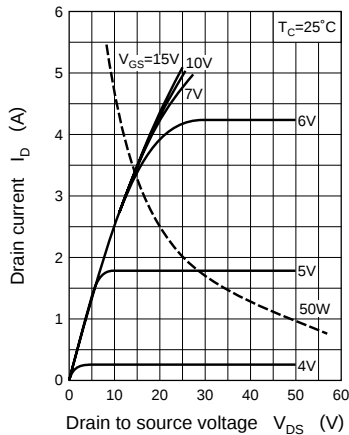
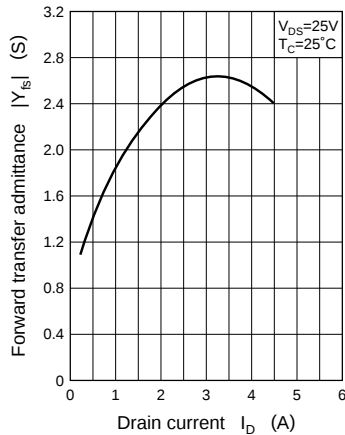
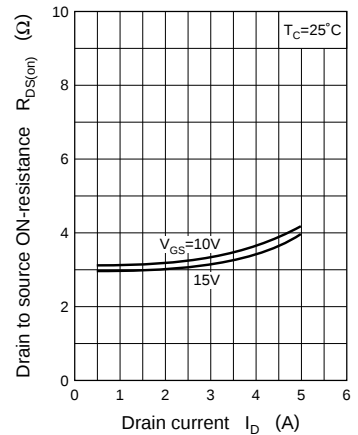
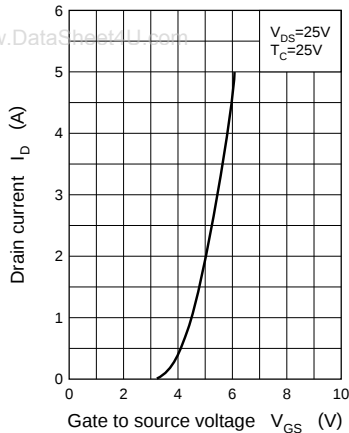
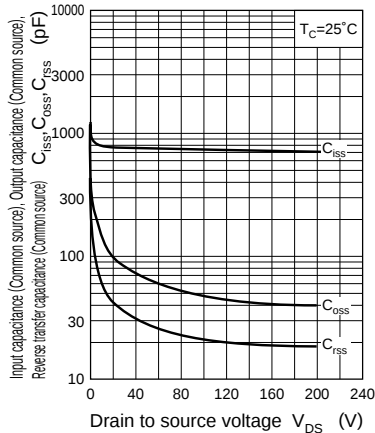
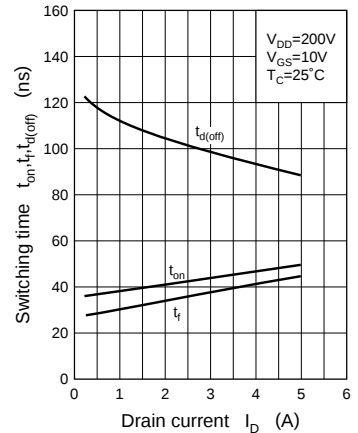
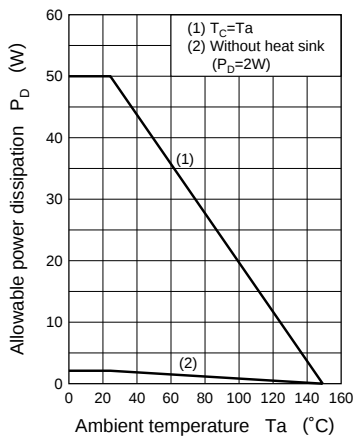
* Single pulse

■ Electrical Characteristics ($T_C = 25^\circ\text{C}$)

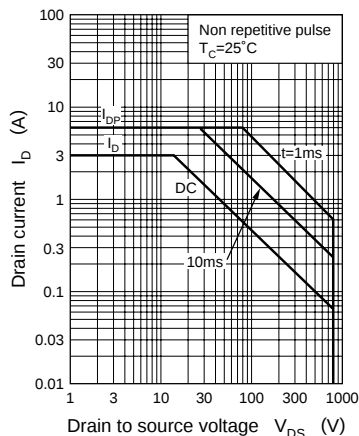
Parameter	Symbol	Conditions	min	typ	max	Unit
Drain to Source cut-off current	I_{DSS}	$V_{DS} = 640\text{V}, V_{GS} = 0$			0.1	mA
Gate to Source leakage current	I_{GSS}	$V_{GS} = \pm 30\text{V}, V_{DS} = 0$			± 1	μA
Drain to Source breakdown voltage	V_{DSS}	$I_D = 1\text{mA}, V_{GS} = 0$	800			V
Avalanche energy capacity	EAS*	$L = 4.5\text{mH}, I_D = 3\text{A}, V_{DD} = 50\text{V}$	20			mJ
Gate threshold voltage	V_{th}	$V_{DS} = 25\text{V}, I_D = 1\text{mA}$	1		5	V
Drain to Source ON-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 2\text{A}$		3.2	4	Ω
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 25\text{V}, I_D = 2\text{A}$	1.5	2.4		S
Input capacitance (Common Source)	C_{iss}	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{MHz}$		730		pF
Output capacitance (Common Source)	C_{oss}			90		pF
Reverse transfer capacitance (Common Source)	C_{rss}			40		pF
Turn-on time	t_{on}	$V_{GS} = 10\text{V}, I_D = 2\text{A}$ $V_{DD} = 200\text{V}, R_L = 100\Omega$		40		ns
Fall time	t_f			35		ns
Turn-off time (delay time)	$t_{d(off)}$			105		ns

* Avalanche energy capacity test circuit



$I_D - V_{DS}$  $|Y_{fs}| - I_D$  $R_{DS(on)} - I_D$  $I_D - V_{GS}$  $C_{iss}, C_{oss}, C_{rss} - V_{DS}$  $t_{on}, t_f, t_{d(off)} - I_D$  $P_D - T_a$ 

Area of safe operation (ASO)

 $EAS - T_j$ 