## K1528D Series

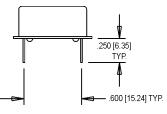
## 14 pin DIP, 5.0 Volt, CMOS, VCXO

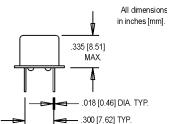






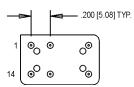
- Former Champion product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation





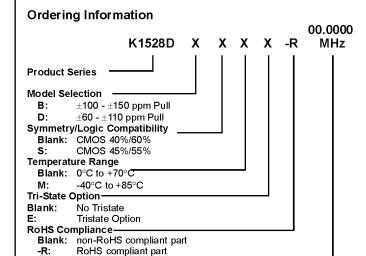






## **Pin Connections**

PIN	FUNCTION				
1	Voltage Control				
7	Ground/Case Ground				
8	Output				
14	+Vdd				



	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes	
	Frequency Range	F	35	1,7,1-1	85	MHz		
	Operating Temperature	T <sub>A</sub>	(See ordering information)					
	Storage Temperature	Ts	-40		+125	°C		
	Frequency Stability	ΔF/F						
	Overall		Inclusive of Calibration, Tempera			nperature		
			Voltage, Load, and Aging			,		
	0°C to 70°C		±25			ppm		
	-40°C to +85°C				±50	ppm		
	Aging					Γ΄.		
١,,	1 <sup>st</sup> Year		-5		+5	ppm		
۱ä	Thereafter (per year)		-2		+2	ppm		
Specifications	Pullability/APR		(See ordering information)					
ij	Control Voltage	Vc	0.5	2.5	4.5	V		
ec	Linearity				15	%	Positive Monotonic Slope	
	Modulation Bandwidth	fm	20			kHz	±3dB	
Sal	Input Impedance	Zin	50k			Ohms	@ 10 kHz	
Electrical	Input Voltage	Vdd	4.75	5.0	5.25	V		
	Input Current	ldd			40	mA		
	Output Type						HCMOS/TTL	
	Load		5 TTL or 15 pF HCMOS				See Note 1	
	Symmetry (Duty Cycle)		(See ordering information)					
	Logic "1" Level	Voh	4.5			V		
	Logic "0" Level	Vol			0.5	V		
	Output Current				±16	mA		
	Rise/Fall Time	Tr/Tf			4	ns		
	Start Up Time				10	ms		
	Phase Jitter @ 40 MHz	ÖJ		2		ps RMS	Integrated 12 kHz – 20 MHz	
	Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from Carrier	
	@40 MHz	-65	-95	-115	-120	-140	dBc/Hz	
<del>-</del>	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)						
jį.	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)						
Environmental	Hermeticity	Per MIL-STD-202, Method 112, (1x10-8 atm. cc/s of Helium)						
<u>ē</u>	Thermal Cycle	to +125°C, 15 min. dwell, 10 cycles)						
2	Solderability	Per EIAJ-STD-002						
Ш	Soldering Conditions							
	1 TTL load - see load circuit diagrams #1 and #2							

Frequency (customer specified)

- 1. TTL load see load circuit diagrams #1 and #2
- 2. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.