JWH5125C

65V/5A Asynchronous Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H5125C is a current mode monolithic buck switching regulator. Operating with an input range of 4.5V~65V, the JWH5125C delivers 5A of continuous output current with an integrated high side N-Channel MOSFET. At light loads, the regulator operates in low frequency to maintain high efficiency. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The JWH5125C guarantees robustness with short-circuit protection, thermal protection, current run-away protection, and input under voltage lockout.

The JWH5125C is available in ESOP8 package, which provides a compact solution with minimal external components.

FEATURES

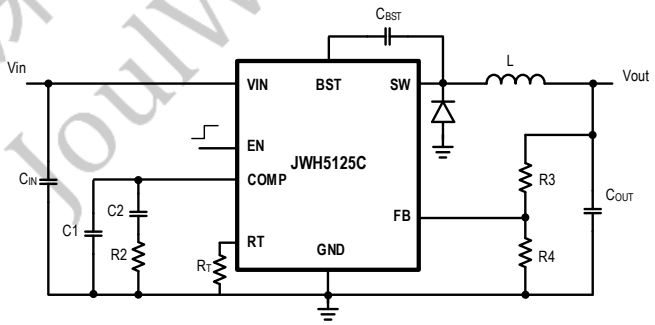
- 4.5V to 65V operating input range
  5A output current
- 0.8V±1% internal voltage reference
- Adjustable switching frequency
- Adjustable UVLO and hysteresis
- Current run-away protection
- Short circuit protection
- Thermal protection
- Available in ESOP8 package

APPLICATIONS

- Industrial Automation and Motor Control
- Vehicle Accessories: GPS Entertainment
- USB Dedicated Charging Ports and Battery Chargers
- 12-V, 24-V and 48-V Industrial, Automotive and Communications Power Systems

TYPICAL APPLICATION

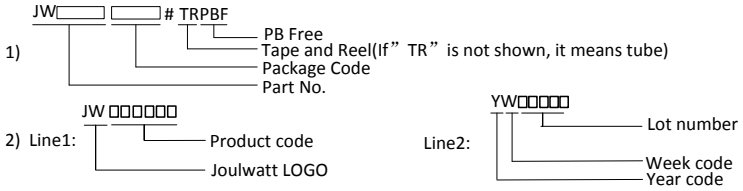
5A Step Down Regulators



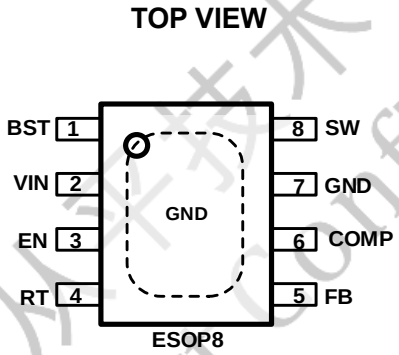
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH5125CESOP#TRPBF	ESOP8	JWH5125C YW□□□□□

Notes:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VIN, SW Pin ..... -0.3V to 69V
SW Pin……-0.6V(-7V for 10ns) to 69V(74V for 20ns)
EN Pin ..... -0.3V to 8.4V
BST Pin ..... SW-0.3V to SW+6V
COMP Pin..... -0.3V to 3V
All Other Pins ..... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} .....4.5V to 65V
Output Voltage Vout.....0.8V to Dmax x VIN
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
ESOP8	42	3.8ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH5125C includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A =-40~125 ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
V_{IN} Under-voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising	3.85	4.25	4.49	V
V_{IN} Under-voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$	V_{IN} falling		200		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		4	6	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1V		180	230	μA
Feedback Voltage	V_{FB}	4.5V≤V_{VIN}≤65V, T_J =-40 ºC ~125 ºC	792	800	808	mV
Power Switch Resistance[5)]	$R_{DS(ON)}$			97	180	mΩ
Power Switch Leakage Current	I_{LEAK}	V_{IN}=65V, V_{EN}=0V, V_{SW}=0V			6	uA
Current Limit Threshold	I_{LIM}		6.28	7.2	8.12	A
Error Amplifier Transconductance	g_M			330		uA/V
Error Amplifier DC Gain[5)]	Gain			1000		V/V
Error Amplifier Source/Sink	I_{EA}			±37		uA
COMP to SW Current Transconductance[5)]	g_{CS}			18		A/V
Switch Frequency	f_{SW}	R_{RT}=200k	370	414	456	kHz
Switch Frequency Range			100		2000	kHz
Minimum On Time[5)]	T_{ON_MIN}			100	130	ns
Minimum Off Time[5)]	T_{OFF_MIN}	V_{FB}=0.4V		165		ns
Soft-start Time[5)]	Tss	10% to 90%		1.25		ms
EN Shutdown Threshold	V_{EN_TH}	V_{EN} rising, FB=0.6V	1.1	1.22	1.34	V
EN Shutdown Hysteresis	V_{EN_HYST}	V_{EN} falling, FB=0.6V		100		mV
Thermal Shutdown[5)]	T_{TSD}			170		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			20		°C

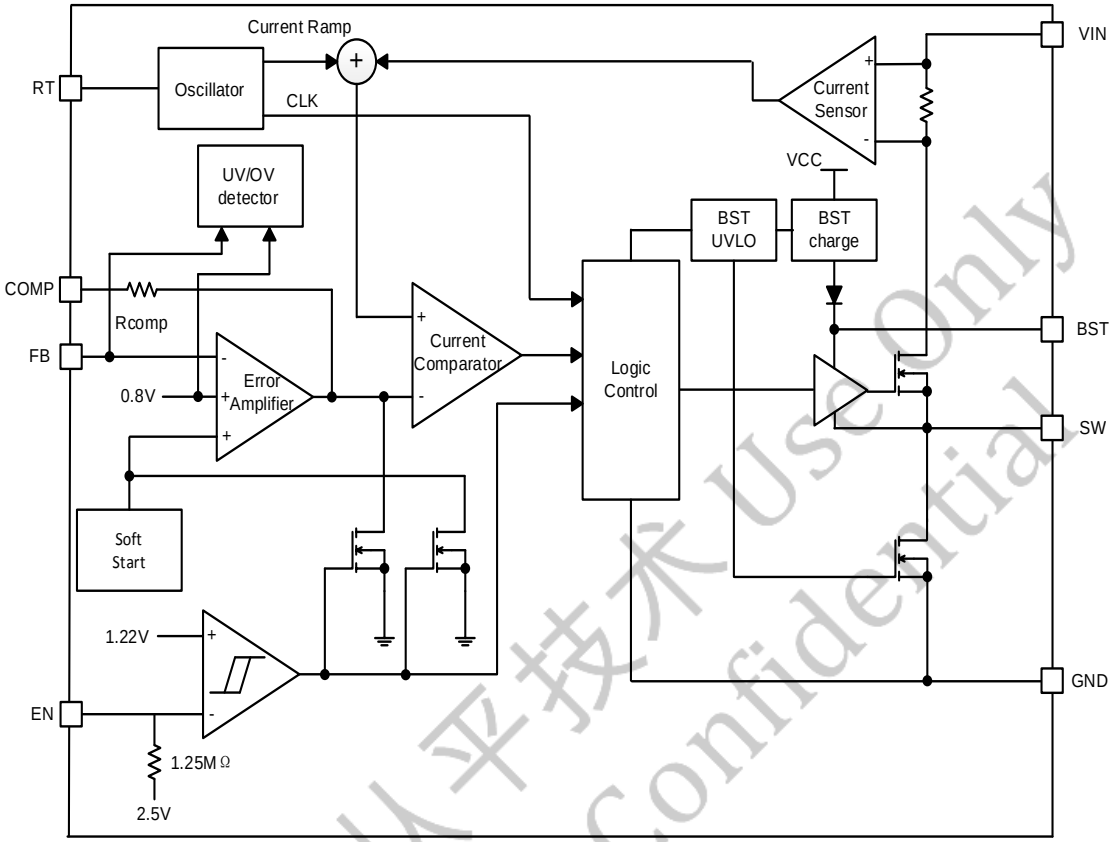
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Pin ESOP8	Name	Description
1	BST	Bootstrap pin for top switch.
2	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 65V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	EN	Drive EN pin high or floating to turn on the regulator and low to turn off the regulator.
4	RT	Switching frequency program. Connect an external resistor from RT pin to ground to set the switching frequency.
5	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 800mV. Connect a resistive divider at FB.
6	COMP	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
7	GND	Ground.
8	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
	Thermal Pad	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

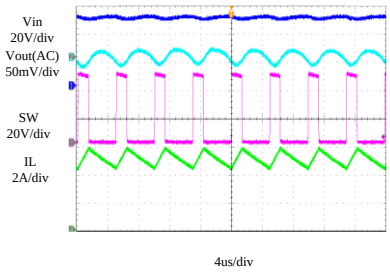
BLOCK DIAGRAM



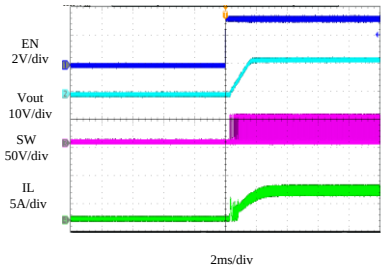
TYPICAL PERFORMANCE CHARACTERISTICS

V_{in} =48V, V_{out}= 12V, L = 33μH, C_{OUT} = 88μF, R_T = 432KΩ, T_A = +25°C, unless otherwise noted

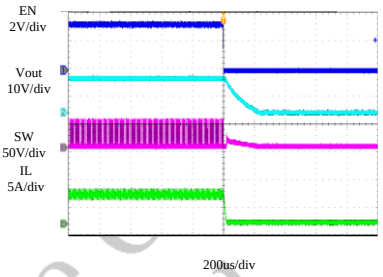
Steady State Test
V_{in}=48V, V_{out}=12V
I_{OUT}=5A



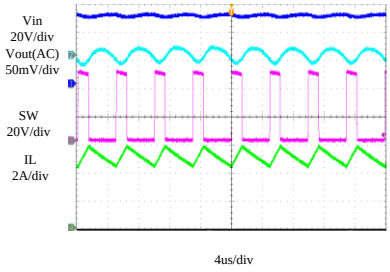
Startup through Enable
V_{in}=48V, V_{out}=12V
I_{OUT}=5A (Resistive load)



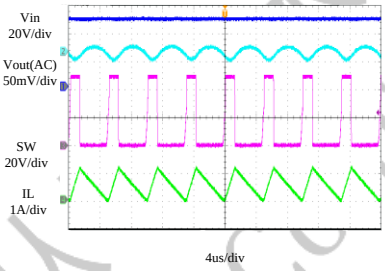
Shutdown through Enable
V_{in}=48V, V_{out}=12V
I_{OUT}=5A (Resistive load)



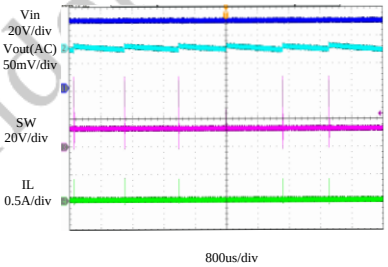
Heavy Load Operation
5A LOAD



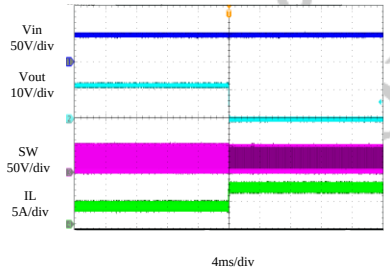
Light Load Operation
0.5A LOAD



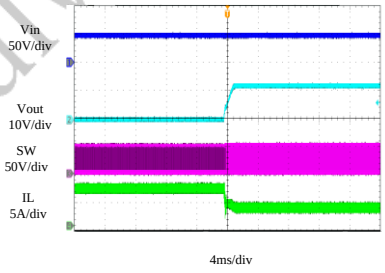
No Load Operation
0 A LOAD



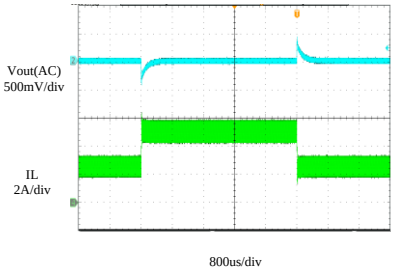
Short Circuit Protection
V_{in}=48V, V_{out}=12V
I_{OUT}=3A-Short



Short Circuit Recovery
V_{in}=48V, V_{out}=12V
I_{OUT}= Short-3A



Load Transient
2.5A LOAD->5A LOAD->2.5A LOAD
C_1=6.8nF, R_1=15k, C_2=100pF



TYPICAL PERFORMANCE CHARACTERISTICS

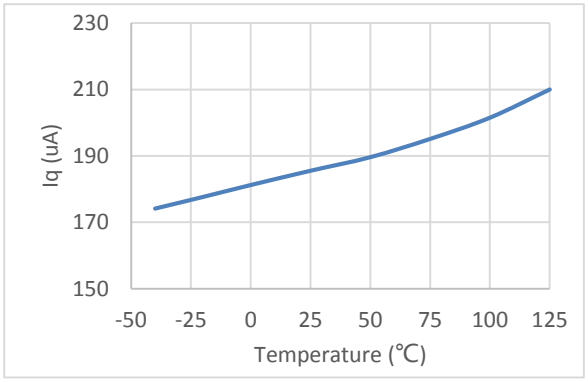


Figure 1. Supply Current vs Junction Temperature

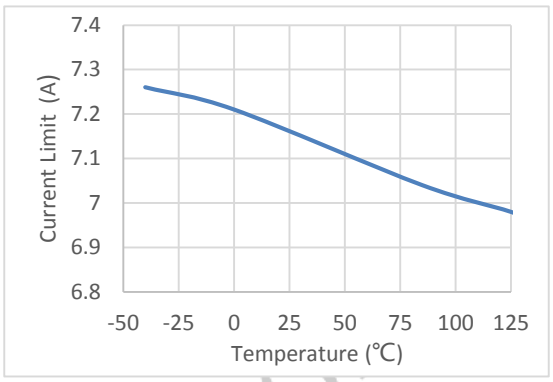


Figure 2. Shutdown Current vs Junction Temperature

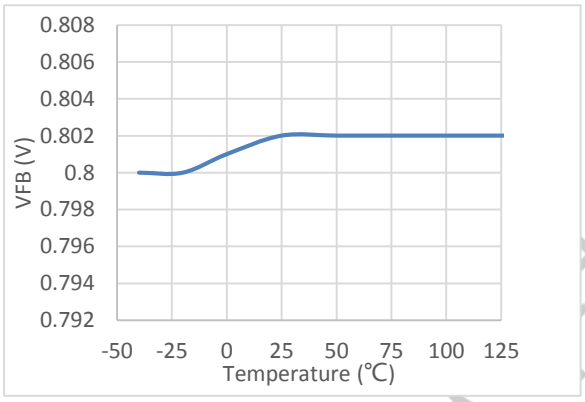


Figure 3. FB Voltage Regulaion vs Junction Temperature

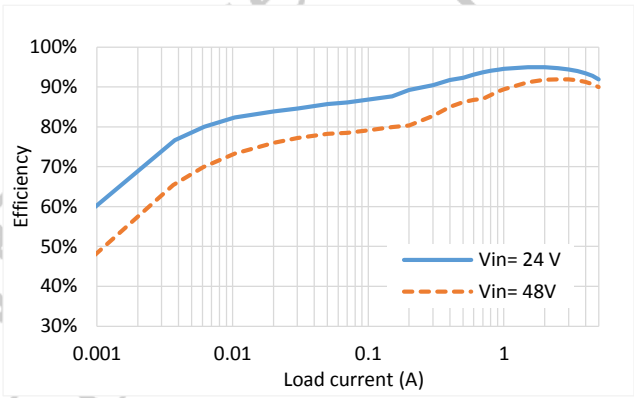


Figure 4. Efficiency vs Load Current

(Vout=12V, L=18μH, R_T=240k)

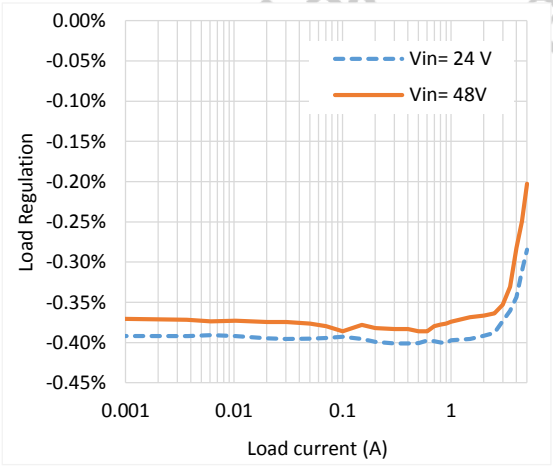


Figure 5. Load Regulation vs Load Current

(Vout=12V, L=18μH, R_T=240k)

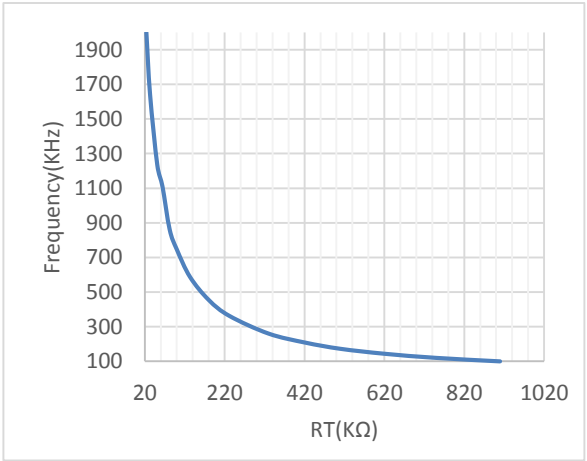


Figure 6. Switch Frequency vs RT

(Vout=12V, L=18μH)

FUNCTIONAL DESCRIPTION

The JWH5125C is an asynchronous, current-mode, step-down regulator. It regulates input voltages from 4.5V to 65V down to an output voltage as low as 0.8V, and is capable of supplying up to 5A of load current.

Power Switch

N-Channel MOSFET switch is integrated on the JWH5125C to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 4.3V rail when SW is low.

Current-Mode Control

The JWH5125C utilizes fixed frequency, peak current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier. The voltage feedback loop is compensated by an external RC network connected between the COMP pin and GND pin.

An internal oscillator initiates the turn on of the high side power switch, and the error amplifier output at the COMP pin controls the high side power switch current that when the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off.

The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. The PFM mode is implemented with a minimum voltage clamp on the COMP pin.

PFM Mode

The JWH5125C operates in PFM mode at light load to improve efficiency by reducing switching and gate drive losses.

During PFM mode operation, the JWH5125C senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters PFM mode is dependent on the output inductor value.

Slope Compensation Output Current

The JWH5125C adds a compensating ramp to the COMP voltage to prevent sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch will constant with duty cycle increases.

Shut-Down Mode

The JWH5125C shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JWH5125C drops below 4uA.

Enable and Adjustable UVLO Protection

The JWH5125C is enabled when the VIN pin voltage rises above 4.25V and the EN pin voltage exceeds the enable threshold of 1.22V. The JWH5125C is disabled when the VIN pin voltage falls below 4.05V or when the EN pin voltage is below 1.12V. The EN pin has an internal pull-up resistor that enables operation of the JWH5125C when the EN pin floats.

If an application requires a higher VIN

under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 1). So that when VIN rises to the pre-set value, EN rises above 1.22V to enable the device and when Vin drops below the pre-set value, EN drops below 1.12V to trigger input under voltage lockout protection.

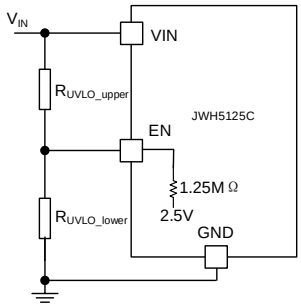


Figure7. Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} = \left(V_{EN\_TH} - \frac{2.5V}{1.25M\Omega * \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_upper} * R_{UVLO\_lower}} + 1}\right) * \left(R_{UVLO\_upper} * \frac{1.25M\Omega + R_{UVLO\_lower}}{1.25M\Omega * R_{UVLO\_lower}} + 1\right)$$

$$V_{UVLO\_HYS} = \left(R_{UVLO\_upper} * \frac{1.25M\Omega + R_{UVLO\_lower}}{1.25M\Omega * R_{UVLO\_lower}} + 1\right) * V_{EN\_HYS}$$

When R_{UVLO_lower} <=100K Ω , V_{UVLO} can be calculated approximately according to the following equation.

$$V_{UVLO} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} * V_{EN\_TH}$$

$$V_{UVLO\_HYS} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} * V_{EN\_HYS}$$

where

V_{EN_TH} is enable shutdown threshold (1.22V typ.);

V_{EN_HYS} is enable shutdown hysteresis (100mV typ.);

Switching Frequency

The switching frequency of JWH5125C can be programmed by the resistor R_T from the RT pin and GND pin over a wide range from 100 kHz to 2000 kHz. The RT pin voltage is typically 1.2V and must have a resistor to ground to set the switching frequency. The R_T resistance can be calculated by the following equation for a given switching frequency f_{SW}.

$$R_T(\mathrm{K\Omega}) = \frac{92417}{f_{sw}(\mathrm{KHz})} - 23$$

$$f_{sw}(\mathrm{KHz}) = \frac{92417}{(R_T + 23)(\mathrm{K\Omega})}$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 100 ns which limit the maximum operating frequency in applications with high input to output step down ratios.

Maximum Switching Frequency

To protect the converter in overload conditions at higher switching frequencies and input voltages, the JWH5125C implements a frequency fold-back. The oscillator frequency is divided by 4 as the FB voltage drops from 0.8V to below 0.35V. When the FB voltage rise above 0.4V, the frequency exist fold-back state. The oscillator frequency is divided by 8 as the FB voltage drops to 0.18V. When the FB voltage rise above 0.2V, the frequency exist fold-back state.

When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency fold-back effectively increases the off time by

increasing the period of the switching cycle providing more time for the inductor current to ramp down.

The frequency fold-back effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down. With a maximum frequency fold-back ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency fold-back protection.

The following equation calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to V_{OUT_SC}. The selected operating frequency should not exceed the calculated value.

$$f_{sw\_sc} = \frac{f_{DIV}}{t_{ON} * \left(\frac{V_{in} - I_{LIMT} * R_{DSON} + V_d}{I_{LIMT} * R_{dc} + V_{out_{sc}} + V_d} + f_{DIV}\right)}$$

The following equation calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output at maximum input voltage.

$$f_{SW\_maxskip} = \frac{1}{t_{ON}} \cdot \left[\frac{I_O \cdot (R_{dc} + V_{OUT}) + V_d}{V_{IN} - I_O \cdot R_{DSON} + V_d}\right]$$

where I_O means output current,
I_{LIM} means current limit
R_{dc} means inductor resistance
V_{IN} means maximum input voltage
V_{OUT} means output voltage
V_{OUT_SC} means output voltage during short
V_d means diode voltage drop
R_{DSON} means switch on resistance
t_{ON} means controllable on time, t_{ON}=130ns
f_{DIV} means frequency divide equals (1,4,8)

RT Short Protection

If the RT pin is detected to be short to ground, JWH5125C is not allowed to switch to prevent abnormal operation state. The regulator can be reactivated again when the short condition at the RT pin is removed.

Overvoltage Protection

Output overvoltage protection (OVP) is designed in JWH5125C to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance and the power supply output voltage increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

Thermal Protection

When the temperature of the JWH5125C rises above 170°C, it is forced into thermal shut-down.

Only when core temperature drops below 150°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

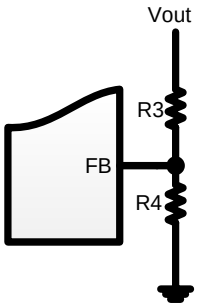
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{out} * \frac{R_4}{R_3 + R_4}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

R4 should be lower than 8 kΩ. Choose R_4 around 2.1kΩ ~ 8kΩ, and then R_3 can be calculated by:

$$R_3 = R_4 * \left(\frac{V_{out}}{0.8} - 1\right)$$



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{out}}{V_{in}} * \left(1 - \frac{V_{out}}{V_{in}}\right)}$$

where I_{OUT} is the load current, V_{out} is the output voltage, V_{in} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_{SW} * \Delta V_{in}} * \frac{V_{out}}{V_{in}} * \left(1 - \frac{V_{out}}{V_{in}}\right)$$

where C_{IN} is the input capacitance value, f_{sw} is the switching frequency, ΔV_{in} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 4.7μF*3/100V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{out} = \frac{V_{out}}{f_{SW} * L} * \left(1 - \frac{V_{out}}{V_{in}}\right) * \left(R_{ESR} + \frac{1}{8 * f_{SW} * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 60μF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{out}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{out}}{V_{in}}\right)$$

where V_{in} is the input voltage, V_{out} is the output voltage, f_{sw} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

External Diode

The JWH5125C requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 65 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the JWH5125C. The select forward voltage of Schottky Diode must be less than the restriction of forward voltage in Figure 8 at operating temperature range to avoid the IC malfunction.

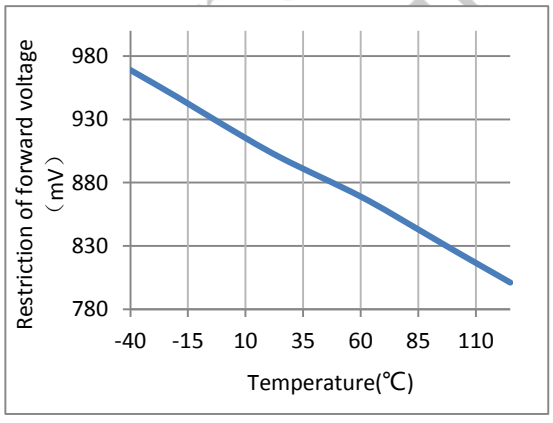


Figure8. Restriction of Forward Voltage vs. Temperature

For the example design, the PDS5100H Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS5100H is 0.52 V at 5 A.

Compensation Network Design

In order to ensure stable operation while maximizing the dynamic performance, the appropriate loop compensation is important. Generally, follow the steps below to calculate the compensation components :

1. Set up the crossover frequency, f_C. In general, one-twentieth to one-sixth of the switching frequency is recommended to be the crossover frequency.
2. R_1 can be determined by:

$$R_1 = \frac{2\pi * f_c * C_{OUT}}{g_M * g_{CS}} * \frac{R_4 + R_3}{R_4} - Rcomp$$

where g_M=325uA/V, g_{CS}=18A/V, Rcomp=5KΩ

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading (R_L). Calculate C_1:

$$C_1 = \frac{C_{OUT} * R_L}{R_1 + Rcomp}$$

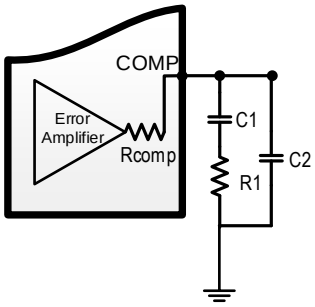
4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero, and optional C_2 can be used to cancel this zero.

$$C_2 = \frac{C_{OUT} * R_{ESR}}{R_1}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_2 = \frac{1}{2\pi * \frac{f_{SW}}{2} * R_1}$$

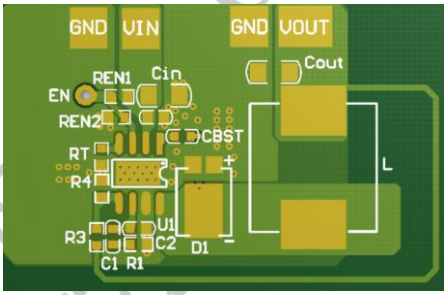
5. Generally, C_2 is an optional component used to enhance noise immunity.



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JWH5125C (VIN pin and GND pin) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. Keep the switching node SW short to prevent excessive capacitive coupling
4. Make Vin, Vout and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

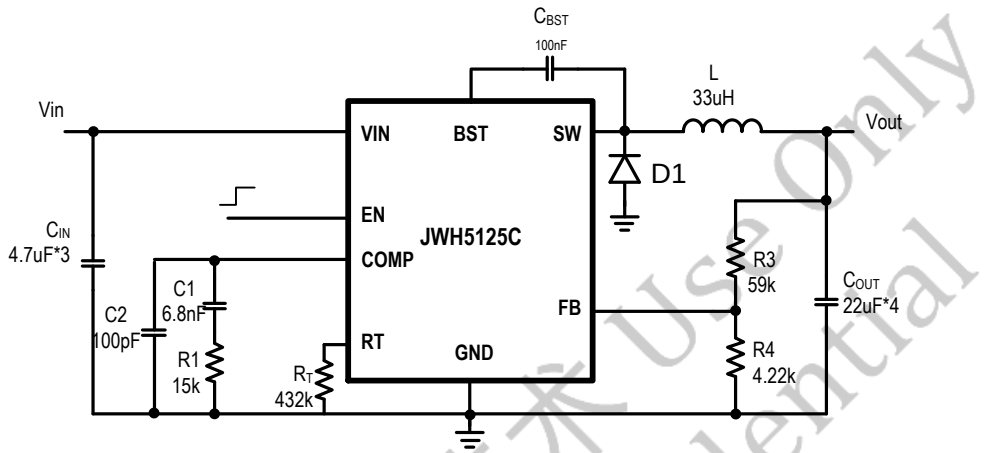


REFERENCE DESIGN

V_{IN}: 14V~65V

V_{OUT}: 12V

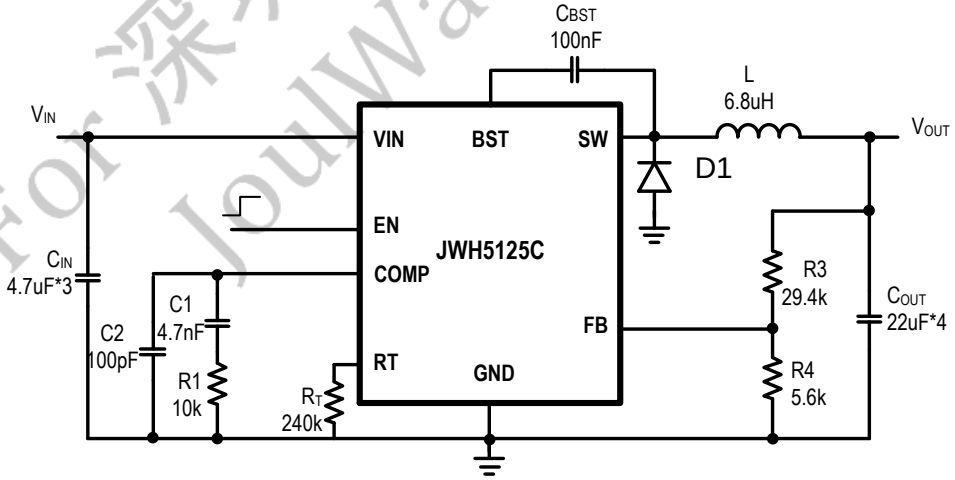
I_{OUT}: 0~5A



V_{IN}: 8V~65V

V_{OUT}: 5V

I_{OUT}: 0~5A



External Components Suggestion (V_{IN}=48V):

V_{OUT}(V)	R_4 (kΩ)	R_3 (kΩ)	R_T (kΩ)	L (μH)	C_{OUT_MIN} (μF)	C_{OUT_EFF} (μF)
3.3	5.6	17.8	240	6.8	88	50
5	5.6	29.4	240	6.8	88	40
12	4.22	59	432	33	88	45

Notes:

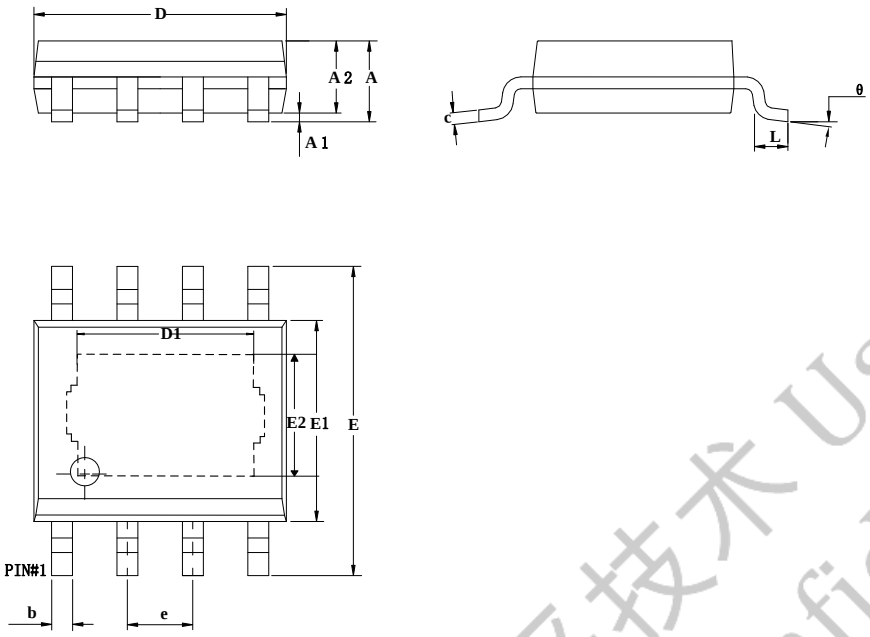
1) Capacitor tolerance and bias voltage de-rating should be considered. The effective capacitance can vary by +20% and -80%. Please refer to the datasheet of capacitor.

2) C_{OUT_MIN} is the minimum nominal capacitance value of C_{OUT} (output capacitance). C_{OUT_EFF} is the minimum effective capacitance value of C_{OUT}.

3) Joulwatt's customers are responsible for determining suitability of components chosen for their purposes. Customers should validate their design implementation to make sure the proper system functionality.

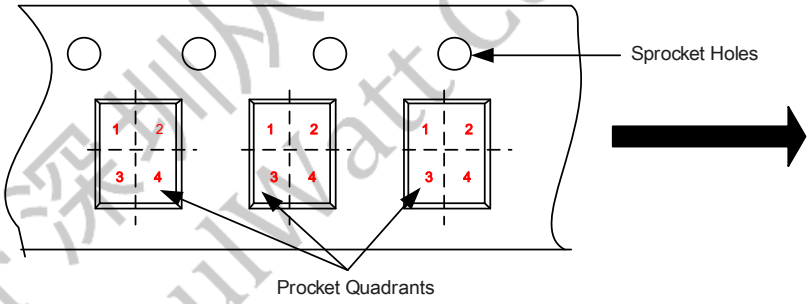
PACKAGE OUTLINE

ESOP8 UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	1.30	—	1.70
A1	0.00	—	0.10
A2	1.35	—	1.55
b	0.33	—	0.51
c	0.17	—	0.25
D	4.70	—	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
D1	3.05	—	3.25
E2	2.16	—	2.36
e	1.27BSC		
L	0.40	—	1.27
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
ESOP8	1

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