



JW7201

Positive High Voltage Ideal Diode-OR With Input Supply and Fuse Monitors

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW[®]7201 is a high-side OR-ing FET controller, which can operate in conjunction with two external MOSFETS as ideal diodes rectifier when connected in series with power sources. Besides, the power consumption, heat dissipation and PC board area also can be reduced by using the diode-OR with N-channel MOSFETS instead of Schottky diodes.

Power sources can easily be ORed together to increase total system reliability with the JW7201. The JW7201 controls the voltage drop across the MOSFET to ensure smooth current transfer from one path to the other without oscillation. There is a fast response comparator to turn off the MOSFETS to prevent the reverse current from reaching a level that could damage the MOSFET if a power source fails or is shorted.

Fault conditions such as the input supplies are not in regulation, the inline fuses are blown, both

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of the external N-channel gate drive(V_{GSx}) are less than 0.6V, or the voltages across the MOSFETS are greater than the fault threshold will trigger the power fault detection.

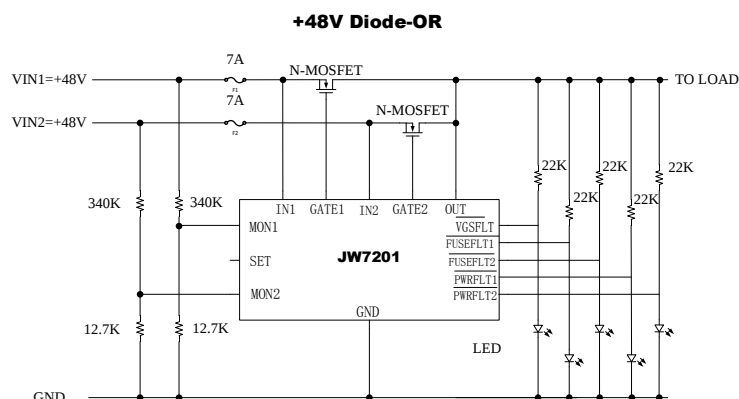
FEATURES

- Replaces power schottky diodes
- Controls N-channel MOSFETS
- 0.3 μ s turn-off time limits peak fault current
- Wide operating voltage range: 6V to 80V
- Smooth switchover without oscillation
- No reverse DC current
- Monitors V_{IN} , fuse, and MOSFET diode
- Available in 14-lead (4mm $\times$ 3mm) DFN, 16-lead SOP packages

APPLICATIONS

- High Availability Systems
- Advanced TCA[®] (ATCA) Systems
- +48V and -48V Distributed Power Systems
- Telecom Infrastructure

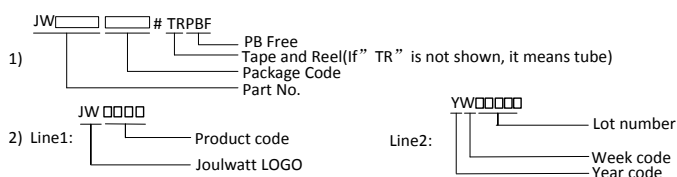
TYPICAL APPLICATION



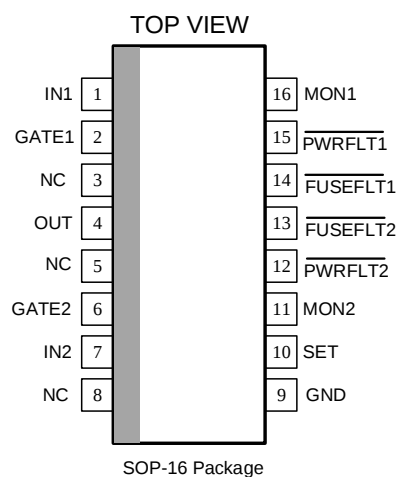
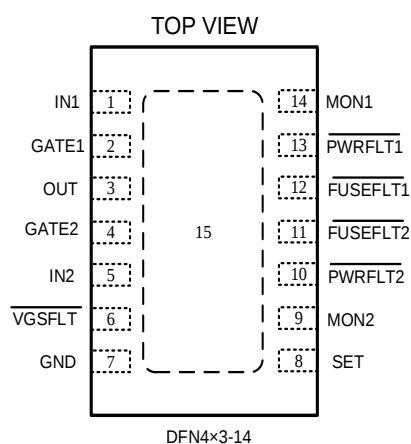
ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW7201SOPD#TRPBF	SOP16	JW7201 YW□□□□□
JW7201DFNK#TRPBF	DFN4X3-14	JW7201 YW□□□□□

Note:



PIN CONFIGURATION

ABSOLUTE MAXIMUM RATING^{1) 2)}

IN1,IN2 PIN Voltage	-1V to 100V
OUT PIN Voltage	-0.3V to 100V
MON1,MON2,SET PIN Voltage	-0.3V to 7V
GATE1 Pins Voltage ³⁾	$V_{IN1}-0.2V$ to $V_{IN1}+13V$
GATE2 Pins Voltage ³⁾	$V_{IN2}-0.2V$ to $V_{IN2}+13V$
$\overline{PWRFLT1}$, $\overline{PWRFLT2}$, $\overline{FUSEFLT1}$, $\overline{FUSEFLT2}$, $\overline{VGSFLT}$	-0.3V to 8V
Storage Temperature Range	-65°C to 150°C
Lead Temperature(Soldering,10 sec)	300°C

RECOMMENDED OPERATING CONDITIONS

IN1,IN2 PIN Voltage	6V to 80V
OUT PIN Voltage.....	6V to 80V
MON1,MON2,SET PIN Voltage.....	0V to 5V
$\overline{\text{PWRFLT1}}$, $\overline{\text{PWRFLT2}}$, $\overline{\text{FUSEFLT1}}$, $\overline{\text{FUSEFLT2}}$, $\overline{\text{VGSFLT}}$	0V to 5V

THERMAL PERFORMANCE⁴⁾

θ_{JA}

14-DFN.....	43°C/W
16-SOP.....	75°C/W

Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) All currents into pins are positive, all voltage are referenced to GND unless otherwise specified
- 3) The GATEx pins are internally limited to a minimum of 13V above Inx. Driving these pins beyond the clamp may damage the part.
- 4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

$T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, $6\text{V} < V_{\text{OUT}} < 80\text{V}$ unless otherwise stated.						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Supply Range	V_{OUT}		6		80	V
Supply Current	I_{OUT}		200	500	800	μA
INx Pin Input Current	I_{INx}	GATE High	0.5	0.6	1.2	mA
External N-Channel Gate Drive($V_{\text{GATEx}} - V_{\text{INx}}$)	ΔV_{GATEx}	$V_{\text{OUT}} = 20\text{V}$ to 80V	10	12	16	V
		$V_{\text{OUT}} = 9\text{V}$ to 20V	6	12	15	
		$V_{\text{OUT}} = 6\text{V}$ to 9V	3.5		7	
External N-Channel Gate Pull-Up Current	$I_{\text{GATEx(UP)}}$	$V_{\text{GATEx}} = V_{\text{INx}}$, $V_{\text{INx}} - V_{\text{OUT}} = 100\text{mV}$	$V_{\text{INx}} = 80\text{V}$ -100	-200	-300	μA
			$V_{\text{INx}} = 6\text{V}$ -30	-45	-60	
External N-Channel Gate Pull-Down in Fault Condition	$I_{\text{GATEx(DN)}}$	Gate Drive Off	1			A
Gate Turn-Off Time ⁵⁾	t_{OFF}	$V_{\text{INx}} - V_{\text{OUT}} = 55\text{mV}$ to -1V , $V_{\text{GATEx}} - V_{\text{INx}} < 1\text{V}$		0.3	0.4	μs
MONx Pin Threshold Voltage	$V_{\text{MONx(TH)}}$	V_{MONx} Rising	1.209	1.227	1.245	V
MONx Pin Hysteresis Voltage	$V_{\text{MONx(HYST)}}$	$V_{\text{MONx}} = 1.23\text{V}$	10	30	45	mV
MONx Pin Input Current	$I_{\text{MONx(IN)}}$			0	± 1	μA
INx Pin Threshold Voltage	$V_{\text{INx(TH)}}$	V_{INx} Rising	3	3.5	4	V
INx Pin Hysteresis Voltage	$V_{\text{INx(HYST)}}$		50	100	150	mV
Source-Drain Regulation Voltage($V_{\text{INx}} - V_{\text{OUT}}$)	ΔV_{SD}		10	25	40	mV
Short-Circuit Fault Voltage ($V_{\text{INx}} - V_{\text{OUT}}$) Rising	$\Delta V_{\text{SD(FLT)}}$	SET=10k Ω	0.04	0.05	0.06	V
		SET=20k Ω	0.08	0.1	0.12	
		SET=120k Ω	0.5	0.6	0.72	
PWRFLT $\bar{x}$, FUSEFLT $\bar{x}$, VGSFLT Pin Output Low	V_{FLT}	$I_{\text{PWRFLT}\bar{x}}, I_{\text{FUSEFLT}\bar{x}}, I_{\text{VGSFLT}} = 5\text{mA}$		80	120	mV
PWRFLT $\bar{x}$, FUSEFLT $\bar{x}$, VGSFLT Pin Leakage Current	I_{FLT}	$V_{\text{PWRFLT}\bar{x}}, V_{\text{FUSEFLT}\bar{x}}, V_{\text{VGSFLT}} = 5\text{V}$		0	± 1	μA

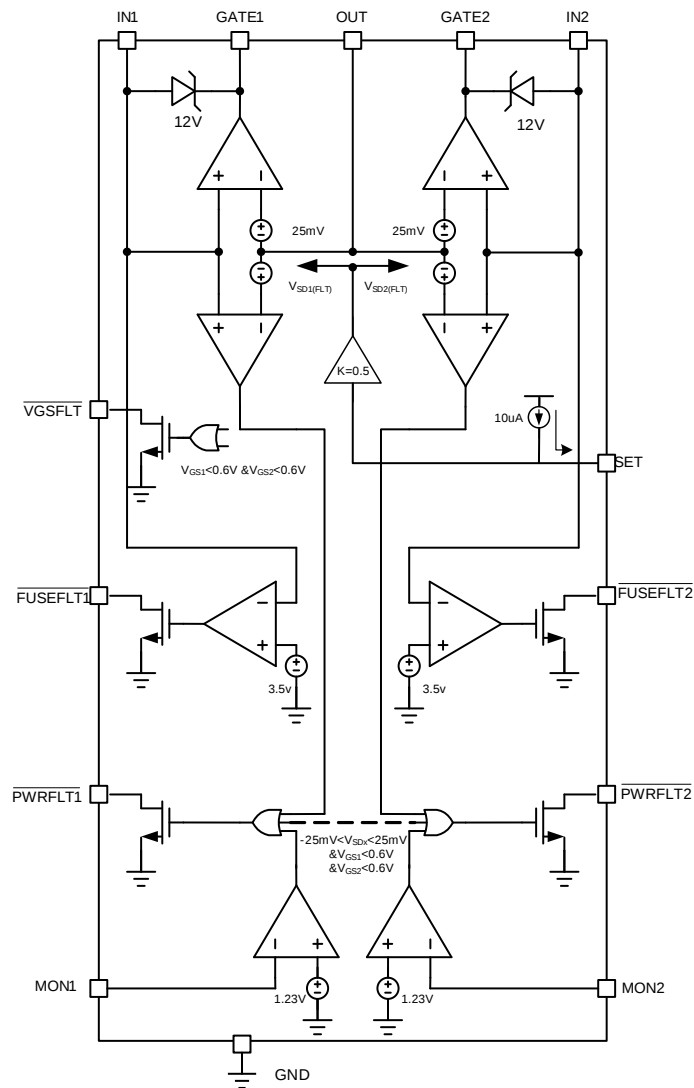
Note:

5).Guaranteed by design.

PIN DESCRIPTION

Name SOP16	Name DFN4X3- 14	Pin	Description
1	1	IN1	Input voltage and GATE fast pull-down return. The IN pin is the anode of the ideal diode and connect to the sources of the N-channel MOSFET. Connect the pin as close to the MOSFET sources as possible. Connect to OUT if unused.
2	2	GATE1	Gate drive output.
4	3	OUT	Drain voltage sense and positive supply input
6	4	GATE2	Gate drive output.
7	5	IN2	Input voltage and GATE fast pull-down return. The IN pin is the anode of the ideal diode and connect to the sources of the N-channel MOSFET. Connect the pin as close to the MOSFET sources as possible. Connect to OUT if unused.
	6	$\overline{\text{VGSFLT}}$	MOSFET fault output. Open-drain output that pulls to GND when $V_{GS1} < 0.6V$ and $V_{GS2} < 0.6V$
9	7	GND	GND
10	8	SET	ΔV_{SD} threshold configuration input.
11	9	MON2	Input supply monitor.
12	10	$\overline{\text{PWRFLT2}}$	Power fault output. Open-drain output that pulls to GND when $\text{MON2} < 1.23V$ or $V_{SD2} > V_{SD(FLT)}$, or $(-25mV < V_{SD2} < 25mV) \& (V_{GS1} < 0.6V) \& (V_{GS2} < 0.6V)$
13	11	$\overline{\text{FUSEFLT2}}$	Fuse fault output. Open-drain output that pulls to GND when $V_{IN2} < 3.5V$
14	12	$\overline{\text{FUSEFLT1}}$	Fuse fault output. Open-drain output that pulls to GND when $V_{IN1} < 3.5V$
15	13	$\overline{\text{PWRFLT1}}$	Power fault output. Open-drain output that pulls to GND when $\text{MON1} < 1.23V$ or $V_{SD1} > V_{SD(FLT)}$, or $(-25mV < V_{SD1} < 25mV) \& (V_{GS1} < 0.6V) \& (V_{GS2} < 0.6V)$
16	14	MON1	Input supply monitor.
3,5,8		NC	Not connected
	15	EXPOSED PAD	Connected to GND or floating.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. OR-ing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using N-channel MOSFETs to replace schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The JW7201 is a positive voltage diode-OR controller that drives two external N-channel MOSFETs as pass transistors to replace OR-ing diodes. The IN and OUT pins form the anodes and cathodes of the ideal diodes. The source pins of the external MOSFETs are connected to the IN pins. The drains of the MOSFETs are connected together at the OUT pin, which is the positive supply of the device. The gates of the external MOSFETs are driven by the JW7201 to regulate the voltage drop across the pass transistors.

At power-up, the initial load current flows through

the body diode of the MOSFET with the higher INx voltage. The associated GATEx pin immediately ramps up and turns on the MOSFET. The amplifier tries to regulate the voltage drop across the source and drain connections to 25mV. If the load current causes more than 25mV of drop, the MOSFET gate is driven fully on and the voltage drop is equal to $R_{DS(on)} \times I_{LOAD}$.

When the power supply voltages are nearly equal, this regulation technique ensures that the load current is smoothly shared between the MOSFETs without oscillation. The current flowing through each pass transistor depends on the $R_{DS(on)}$ of each MOSFET and the output impedances of the supplies.

In the event of a supply failure, such as if the supply that is conducting most or all of the current is shorted to GND, reverse current flows temporarily through the MOSFET that is on. This current is sourced from any load capacitance and from the second supply through the body diode of the other MOSFET. The JW7201 quickly responds to this condition, turning off the MOSFET in about 500ns. This fast turn-off prevents the reverse current from ramping up to a damaging level.

APPLICATION INFORMATION

MOSFET Selection

The JW7201 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(on)}$, the maximum drain-source voltage V_0 , and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be greater than 3.5V when the supply voltage at V_{OUT} is between 6V and 9V and be greater than 6V when the supply voltage at V_{OUT} is between 9V and 20V. When the supply voltage at V_{OUT} is greater than 20V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to less than 15V. This allows the use of logic level threshold N-channel MOSFETs and standard N-channel MOSFETs above 20V. An external zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 15V.

The maximum allowable drain-source voltage, must be higher than the supply voltages. If an input is connected to GND, the full supply voltage will appear across the MOSFET.

If the voltage drop across MOSFET exceeds the configurable, the $\overline{PWRFLT_x}$ pin corresponding to the faulting channel pull low. The $R_{DS(on)}$ should be small enough to conduct the maximum load current while not triggering a fault, and to stay within the MOSFET's power rating at the maximum load current $I^2 \times R_{DS(on)}$.

Fault Condition

The JW7201 monitors fault conditions and shunts current away from LEDs, turning each one off to indicate a specific fault condition.

Table 1. Fault Table

$\overline{VGSFLT}$	$(V_{GS1} < 0.6V) \& (V_{GS2} < 0.6V)$
$\overline{FUSEFLT1}$	$V_{IN1} < 3.5V$
$\overline{FUSEFLT2}$	$V_{IN2} < 3.5V$
$\overline{PWRFLT1}$	MON1 < 1.23V
	Or $V_{SD1} > V_{SD(FLT)}$
	Or $(-25mV < V_{SD1} < 25mV) \& (V_{GS1} < 0.6V)$ $\& (V_{GS2} < 0.6V)$
$\overline{PWRFLT2}$	MON2 < 1.23V
	Or $V_{SD2} > V_{SD(FLT)}$
	Or $(-25mV < V_{SD2} < 25mV) \& (V_{GS1} < 0.6V)$ $\& (V_{GS2} < 0.6V)$

System Power Supply Failure

The JW7201 automatically supplies load current from the system input supply with the higher voltage. If this supply shorts to ground, reverse current begins to flow through the pass transistor temporarily and the transistor begins to turn off. When this reverse current creates -25mV of voltage drop across the drain and source pins of the pass transistor, a fast pull-down circuit engages to drive the gate low faster.

The remaining system power supply delivers the load current through the body diode of its pass transistor until the channel turns on.

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/μs or higher.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN and OUT pins of the JW7201 during reverse recovery. A zero impedance short-circuit directly across an input that is supplying current is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally commutates the reverse current the JW7201 IN pin experiences a negative voltage spike, while the OUT pin spikes in the positive direction

To prevent damage to the JW7201 under conditions of input short-circuit, protect the IN pins and OUT pin. The IN pins are protected by clamping to the GND pin in the negative direction. Protect the OUT pin with a clamp, such as with a TVS, or with a local bypass capacitor of at least 10μF.

Parasitic inductance between the load bypass or the second supply and the JW7201 allows a zero impedance input short to collapse the voltage at

the OUT pin, which increases the total turn-off time (t_{OFF}). For applications up to 30V, bypass the OUT pin with 47μF; above 30V use at least 100μF. One capacitor serves to guard against OUT collapse and also protect OUT from voltage spikes.

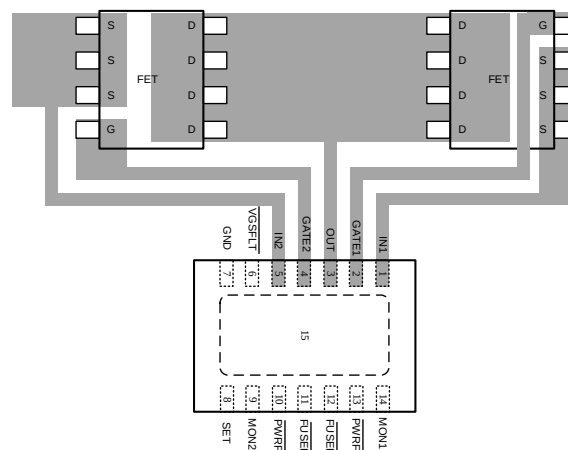
PCB Layout Note

The following advice should be considered when laying out a printed circuit board for the JW7201.

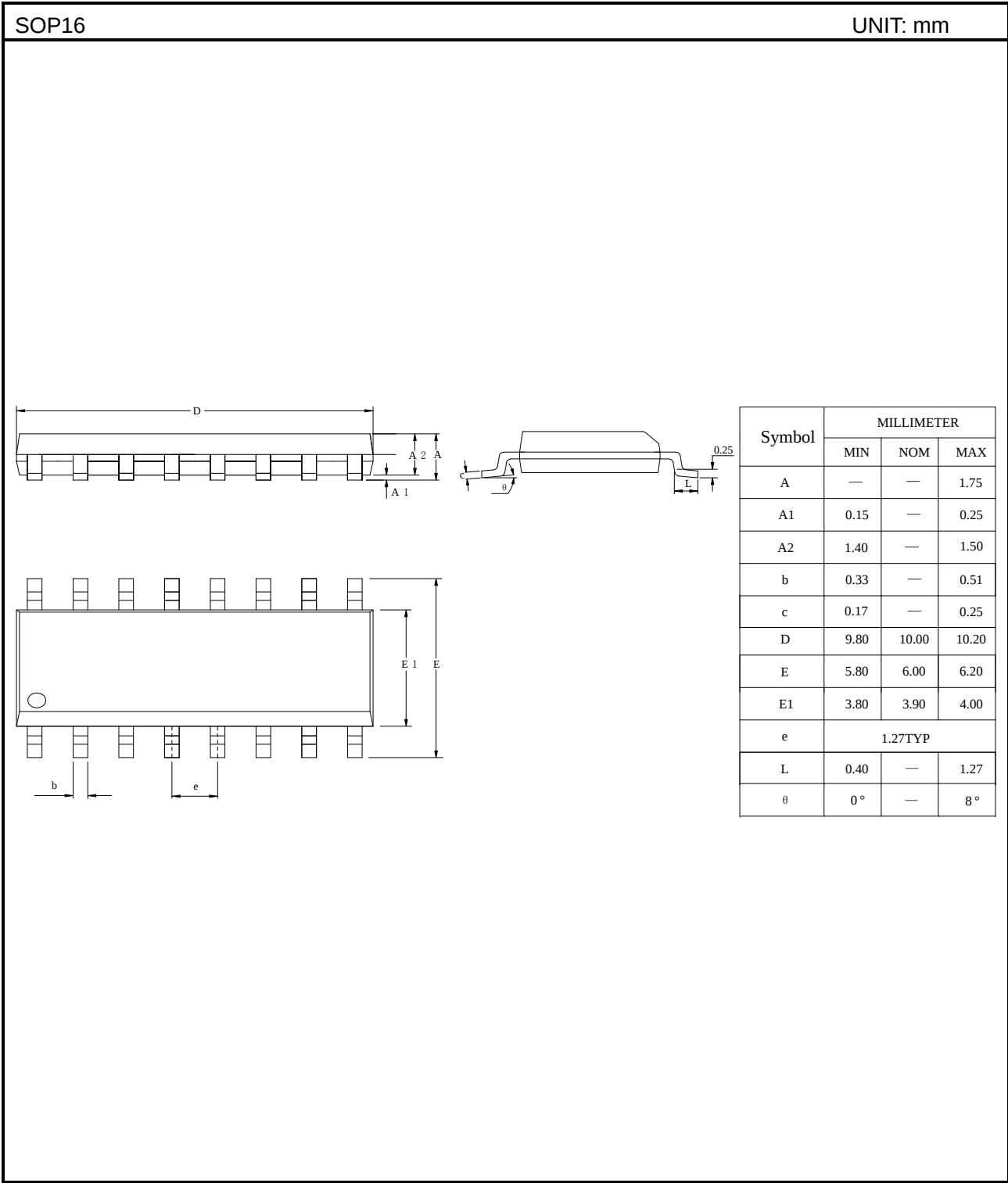
The inputs to the servo amplifiers, IN1, IN2 and OUT should be connected as closely as possible to the MOSFET's terminals for good accuracy.

Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check creepage and clearance guidelines to determine if this is an issue. Use no-clean solder to minimize PCB contamination.

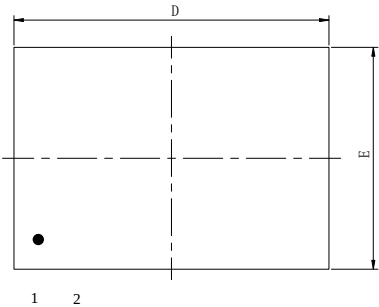


PACKAGE OUTLINE

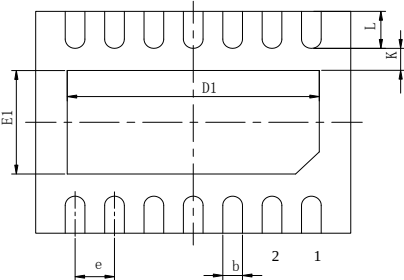


DFN4x3-14

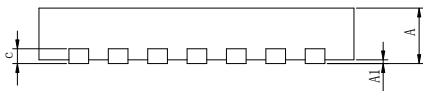
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TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	3.90	4.00	4.10
D 1	3.10	3.20	3.30
e	0.50BSC		
E	2.90	3.00	3.10
E 1	1.60	1.70	1.80
L	0.30	0.40	0.50
K	0.25REF		

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