JW1568K

650V Half-Bridge GaN with Gate Driver

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW1568K is an advanced power system-in-package integrating a gate driver and two enhancement mode GaN transistors in half-bridge configuration. The integrated power GaNs have $R_{DS(ON)}$ of 220 mΩ and 650 V drain-source breakdown voltage, while the high side of the embedded gate driver can be easily supplied by the integrated bootstrap diode.

The JW1568K features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions.

The JW1568K is available in the 6mm*8mm QFN package. The high level of integration results in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

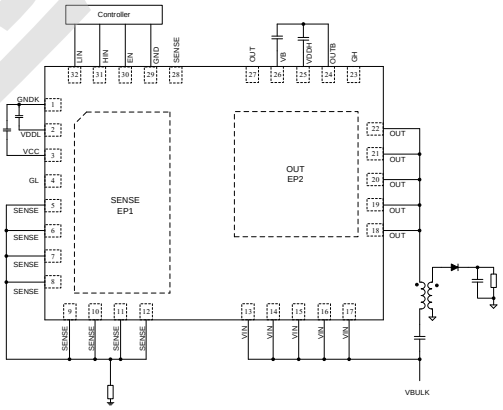
FEATURES

- Integrated Gate Drivers with Si Process
- Ultra-low Standby Current
- Wide VCC Range
- Accurate Internal Timing Match
- Integrated High-side Bootstrap
- High-frequency Operation up to 2MHz
- Protections: VCC UVLO, VDDL/VDDH UVLO, OTP
- Shoot-through Protection
- 650V/220mΩ eMode GaN FETs
- QFN6X8 Package

APPLICATIONS

- Switch-mode power supplies
- AC-DC chargers and adapters
- ACF, AHB, LLC
- DC-DC, DC-AC

TYPICAL APPLICATION



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ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1568KVQJSX#TR	VQFN8*6-32	JW1568K YW□□□□□	Green

Notes:

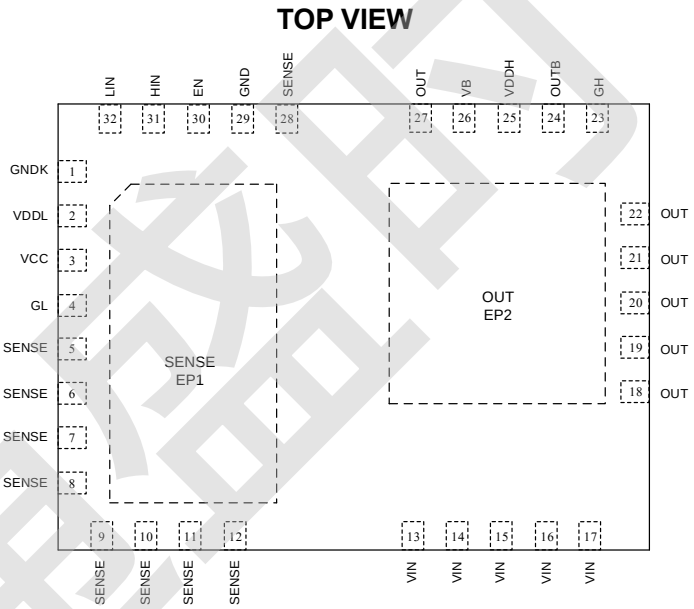
1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



VQFN8X6-32

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ABSOLUTE MAXIMUM RATING[1)]

VCC-GNDK.....-0.3V to 30V
LIN, HIN, EN-GNDK..... -3V to 5.5V
VDDL-GNDK.....-0.3V to 7.2V
GL-GNDK ..... -0.3V to VDDL+0.3 V
OUT-GNDK.....650V
VIN-OUT..... 650V
VB-OUT..... -0.3V to 30V
VDDH-OUT..... -0.3V to 7.2V
GH-OUT ..... -0.3V to VDDH+0.3 V
GND-GNDK ..... -3V to 5.5V
Junction Temperature[2) 3)] ..... -40ºC to 150ºC
Storage Temperature ..... -40ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC

RECOMMENDED OPERATING CONDITIONS

VIN..... 0V to 520V
VCC-GNDK..... 10V to 16.5V
LIN, HIN, EN-GNDK..... 0V to 5V
OUT..... 0V to 520V
VB-OUT..... 8.5V to 16.5V
GNDK, SENSE ..... -2V to 2V
Operating Temperature Range ..... -40ºC to 85ºC
Junction Temperature (T_J) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	$\theta_{JC(top)}$	$\theta_{JC(bot)}$
VQFN8*6-32	TBD	Na	TBDºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1568K includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=400V, VCC=13V, VDDL=6.1V, VDDH=6.1V; T_J = -40~125ºC, unless otherwise stated.

Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Section *(VCC/VB Pin)*						
VCC UVLO Turn-On Threshold	V_{CC_ON}	VCC Rising		9.3		V
VCC UVLO Turn-Off Threshold	V_{CC_OFF}	VCC Falling		8.3		V
VCC UVLO Hysteresis	V_{CC_HYS}			1		V
VCC Quiescent Current	I_{QVCC}	LIN=HIN=0		0.15	0.2	mA
VCC Operating Current	I_{SVCC}	LIN/HIN is switching; f_{SW}=500kHz, Qg=5.6nC		3.22		mA
VB UVLO Turn-On Threshold	V_{B_ON}	VB Rising, To OUTB		7		V
VB UVLO Turn-Off Threshold	V_{B_OFF}	VB Falling, To OUTB		6.7		V
VB UVLO Hysteresis	V_{B_HYS}	To OUTB		0.3		V
VB Quiescent Current	I_{QVCC}	LIN=HIN=0		0.1	0.15	mA
VB Operating Current	I_{SVB}	f_{SW}=500kHz Qg=2.8nC		1.55		mA
Low Side Driver Section *(VDDL/GL Pin to GNDK)*						
VDDL Operation Range	V_{DDL_OP}		5.5	6.1	6.5	V
VDDL UVLO Rising Threshold	V_{DDL_UV+}			5.75		V
VDDL UVLO Falling Threshold	V_{DDL_UV-}			4.5		V
VDDL UVLO Hysteresis	V_{DDL_HYS}			1.25		V
Low Side Peak source current	I_{GL_SRC}			0.1		A
Low Side Peak sink current	I_{GL_SNK}			0.3		A
High level of low side driver output	V_{GL_H}			VDDL		V
Low level of low side driver output	V_{GL_L}			0		V
Low side driver output pull down resistance	R_{GL}			20		kΩ
VDDL current limit	I_{VDDL}			30		mA
High Side Driver Section *(VDDH/GH Pin to OUTB)*						
VDDH Operation Range	V_{DDH_OP}		5.5	6.1	6.5	V
VDDH UVLO Rising Threshold	V_{DDH_UV+}			5.75		V
VDDH UVLO Falling Threshold	V_{DDH_UV-}			4.5		V
VDDH UVLO Hysteresis	V_{DDH_HYS}			1.25		V
Low Side Peak source current	I_{GH_SRC}			0.1		A
Low Side Peak sink current	I_{GH_SNK}			1		A
High level of High side driver output	V_{GH_H}			VDDH		V

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Low level of High side driver output	V_{GH_L}			0		V
High side driver output pull down resistance	R_{GH}			20		kΩ
VDDH current limit	I_{VDDH}			30		mA
Rise time	t_{RISE}	Qg=3nC From 10% to 90%			50	ns
Fall time	t_{FALL}	Qg=3nC From 90% to 10%			50	ns
Input Section (*EN/LIN/HIN*)						
High Level Threshold of EN, LIN and HIN Pins (Rising Edge)	V_{EN_H}			2.6		V
	V_{LIN_H}			2.6		V
	V_{HIN_H}			2.6		V
Low Level Threshold of EN, LIN and HIN Pins (Falling Edge)	V_{EN_H}			1.3		V
	V_{LIN_H}			1.3		V
	V_{HIN_H}			1.3		V
Logic Input Hysteresis	V_{IN_HYS}			1.3		V
LI/HI Input Pull Down Resistance	$R_{LI/HI}$	LI/HI=5V		150		kΩ
EN Input Pull Down Resistance	R_{EN}	EN =5V		600		kΩ
Timing						
Switching Frequency	F_{SW}				2	MHz
Turn On Propagation Delay in Low Side	t_{LON_DLY}	From LIN 50% to GL 10%		35		ns
Turn Off Propagation Delay in Low Side	t_{LOFF_DLY}	From LIN 50% to GL 90%		50		ns
Turn On Propagation Delay in High Side	t_{HON_DLY}	From HIN 50% to GH 90%		50		ns
Turn Off Propagation Delay in High Side	t_{HOFF_DLY}	From HIN 50% to GH 90%		50		ns
Delay Mismatch Time	t_{DLY_MIS}			15		ns
LIN Rising Edge Filter Time	t_{LREFLT}			10		ns
HIN Rising Edge Filter Time	t_{HREFLT}			10		ns
Low-side Minimum On Time	t_{LON_MIN}			60		ns
High-side Minimum On Time	t_{HON_MIN}			60		ns
HIN to LIN Shoot-through Prevention Time	t_{HFEDLY}	SET pin is low	30			ns
Bootstrap FET Characteristics						
Max Bootstrap Charging Current	I_{BOOT}			200		mA
GaN Section						

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Drain-Source On-state Resistance	R_{DS_ON}	V_{GS}=6V, T_J = 25 °C		220	280	mΩ
		V_{GS}=6V, T_J = 125 °C		485		mΩ
Drain-Source Voltage	V_{DSmax}	V_{GS}=0V	650			V
Transient Drain-Source Voltage	$V_{DS(transient)}$	V_{GS}=0V			800	V
Gate to Source Voltage	V_{GS}		-1.4		7	V
Gate to Source Voltage, pulsed	$V_{GS,\ pulse}$	T_{PULSE}=50 ns, f=100kHZ; open drain	-20		10	V
Gate Threshold Voltage	V_{GS_TH}	V_{DS}= V_{GS}, I_D= 7.8mA T_J = 25 °C	1.2	1.7	2.5	V
		V_{DS}= V_{GS}, I_D= 7.8mA T_J = 150 °C		1.6		V
Continuous Current, Drain Source	I_D	Tc = 25 °C		7		A
Pulse Current, Drain Source	$I_{D,\ PULSE}$	V_{GS}=6V, tpulse =300us T_C = 25 °C		12		A
		V_{GS}=6V, tpulse =300us T_C = 125 °C		7		A
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}=650V, T_J = 25 °C		0.5	22	uA
		V_{GS}=0V, V_{DS}=650V, T_J = 150 °C		5	220	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=6V, V_{DS}=0V		40		uA
Source-Drain Reverse Voltage	V_{SD}	V_{GS}=0V; I_{SD}= 2A		2.6		V
Total Gate Charge	Q_G	V_{GS}=6V, V_{DS}=0 to 400V		1.8		nC
Output Charge	Q_{OSS}	V_{GS}=0V, V_{DS}=0 to 400V		17.2		nC
Output Capacitance Stored Energy	E_{OSS}	V_{GS}=0V, V_{DS}=0 to 400V		2.4		uJ
Reverse Recovery Charge	Q_{RR}			0		nC
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=400V, f=100kHz		60		pF
Output Capacitance	C_{OSS}	V_{GS}=0V, V_{DS}=400V, f=100kHz		20		pF
Reverse Transfer Capacitance	C_{RSS}	V_{GS}=0V, V_{DS}=400V, f=100kHz		0.24		pF
Effective Output Capacitance, Energy Related	$C_{O(er)}$	V_{GS}=0V, V_{DS}=0 to 400V		30		pF
Effective output capacitance, Time Related	$C_{O(tr)}$	V_{GS}=0V, V_{DS}=0 to 400V		43		pF
Protection						
VDS Protection Threshold	V_{OCP}			3		V
OCP Detection Blanking Time	t_{OCP_BLK}			200		ns
Thermal Shutdown Threshold	T_{OTP}			150		°C
OTP Hysteresis	T_{HYS}			50		ºC

Note：

5) Guaranteed by design.

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PIN DESCRIPTION

Pin QFN6X8-32	Name	Description
1	GNDK	Gate driver low-side buffer ground. Internally connected to SENCE.
2	VDDL	Low-side driver supply voltage
3	VCC	Logic supply voltage
4	GL	Low-Side GaN gate.
5, 6, 7, 8, 9, 10, 11, 12, 28, EP1	SENSE	Half-bridge sense (low-side GaN Source)
13, 14, 15, 16, 17	VIN	Half voltage supply (high-side GaN Drain)
18, 19, 20, 21, 22, 27, EP2	OUT	Half-bridge output (high-side GaN Source)
23	GH	High-Side GaN gate.
24	OUTB	Gate driver high-side supply voltage, used only for bootstrap capacitor connection. Internally connected to OUT.
25	VDDH	High-side driver supply voltage
26	VB	High side bootstrap voltage
29	GND	Power ground
30	EN	Driver enable input
31	HIN	High-Side driver logic input
32	LIN	Low-Side driver logic input

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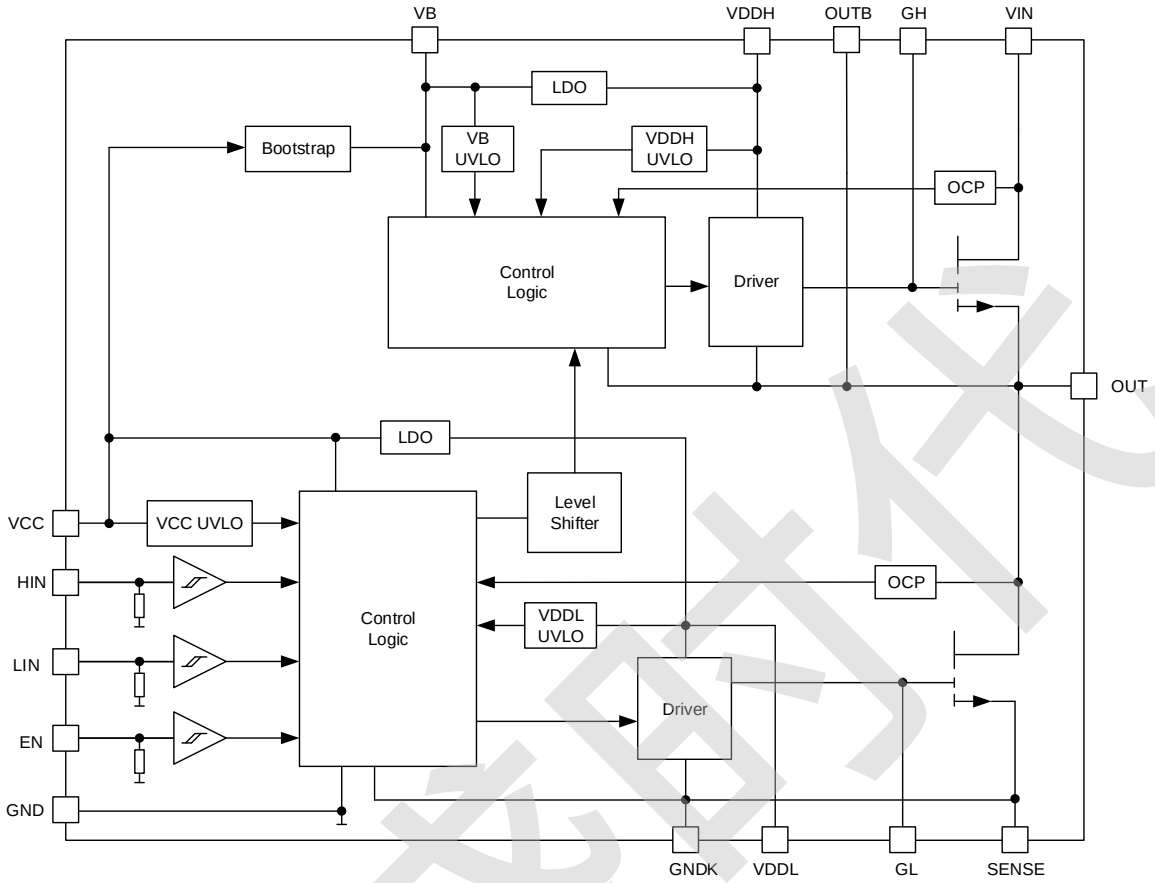
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW1568K is a half-bridge GaN with gate driver.

Logic Inputs

The JW1568K features a half-bridge gate driver with three logic inputs to control the internal high-side and low-side GaN transistors.

The devices are controlled through the following logic inputs:

- EN: Enable input, active high;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high

Input pins			GaN status	
EN	LIN	HIN	LS	HS
L	X	X	OFF	OFF
H	L	L	OFF	OFF
H	L	H	OFF	**ON**
H	H	L	**ON**	OFF
H	H	H	First ON, Second OFF	First ON, Second OFF

If logic inputs are left floating, the gate driver outputs are set to low level and the correspondent GaN transistors are turned off.

In addition, for JW1568K, the rising and falling threshold of the input signal (EN/LIN/HIN) is relative to power ground (GND) rather than the IC ground (GNDK) which is useful to judge the level of the input signal more accurately.

Bootstrap Structure

A bootstrap circuitry is typically used to supply the high-side. JW1568K integrates a bootstrap FET to reduce external components.

The Bootstrap integrated circuit is connected to VCC pin and is driven synchronously with the low-side driver.

The use of an external bootstrap diode in parallel to the integrated structure is possible to achieve faster charging.

VCC Supply Pins and UVLO Function

The VCC pin supplies current to VDDL, the logic circuit and the integrated bootstrap diode.

The VDDL pin supplies low-side output buffer. During output commutations the average current used to provide gate charge to the high-side and low-side GaN transistors flows through this pin.

The use of dedicated bypass ceramic capacitors located as close as possible to each supply pin is highly recommended.

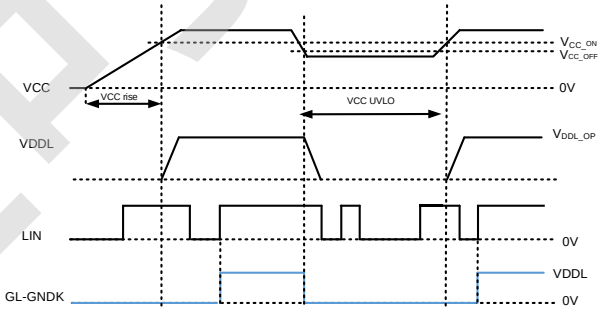


Figure. 1 VCC UVLO at Low Side

VB UVLO Protection

When VB voltage goes below V_{B_OFF} threshold the high-side GaN transistor is switched off. When VB voltage reaches V_{B_ON} threshold, VDDH starts to ramp up. The device returns to normal operation and the output remains off until the detection of the HIN pin's rising edge, that activates the high side transistor's turn-on.

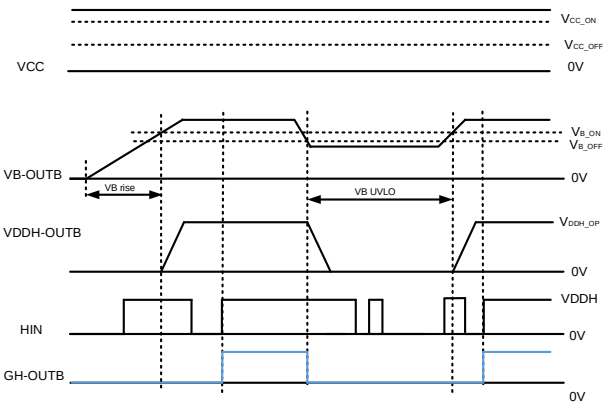


Figure. 2 VB UVLO at High Side

Shoot-through Prevention

To prevent the glitch and switching noise, the LIN/HIN input is effective after the filter time (t_{LREFLT}/t_{HREFLT}). To prevent the shoot-through problem, GL will keep low until the LIN input is effective and GH has been sent for a delay time(t_{HFEDLY}). Meanwhile, GH will not be high until HIN input is effective and GL is low.

Over Current Protection (OCP)

When GL/GH is high, after a detection blanking time of t_{OCP_BLK}, the driver detects the Drain-source voltage of the low-side/high-side GaN. If V_{DS}>V_{OCP}, an OCP fault is asserted and the GATE is turned off until receiving input signal at the next cycle.

Thermal Shutdown

When the temperature of the JW1568K rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 100°C can the driver become active again.

Protection	Sensing	Condition	Delay to action	Action
VCC UVLO	VCC voltage	VCC<V_{CC_OFF}	none	VCC UVLO hysteresis
VB UVLO	VB voltage (to OUTB)	VB<V_{B_OFF}	none	VB UVLO hysteresis
VDDL UVLO	VDDL voltage	VDDL<V_{DDL_UV}	none	VDDL UVLO hysteresis
VDDH UVLO	VDDH voltage	VDDH<V_{DDH_UV}	none	VDDH UVLO hysteresis
OCP	VDS voltage	V_{DS}>V_{OCP} when GL/GH is on	t_{OCP_BLK}	Turn off the GATE and recover at next cycle
Thermal shutdown	Junction temperature	T_J>T_{OTP}	none	Reset until T_J<T_{OTP}-T_{HYS} or VCC UVLO

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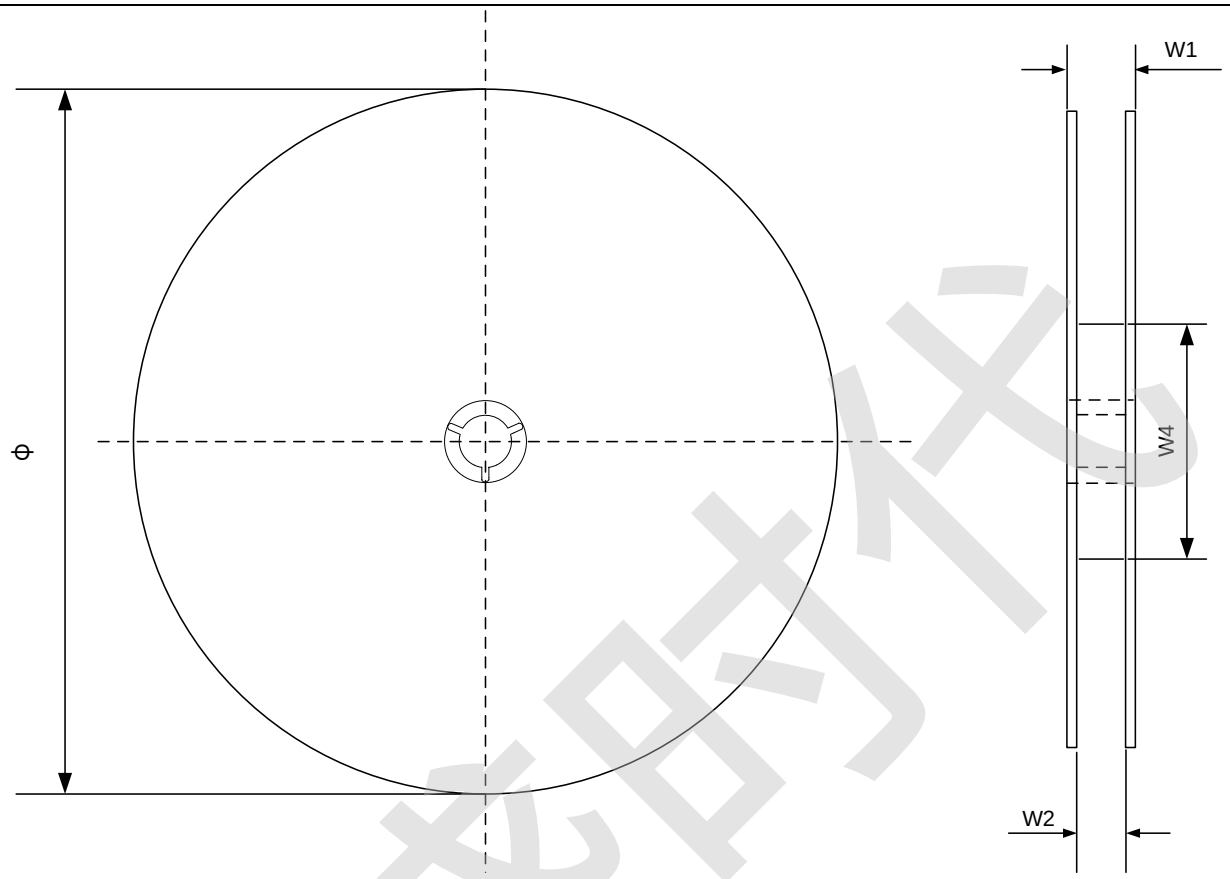
TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
VQFN8*6-32	330±2	23.4±2	16.4±2	100±2

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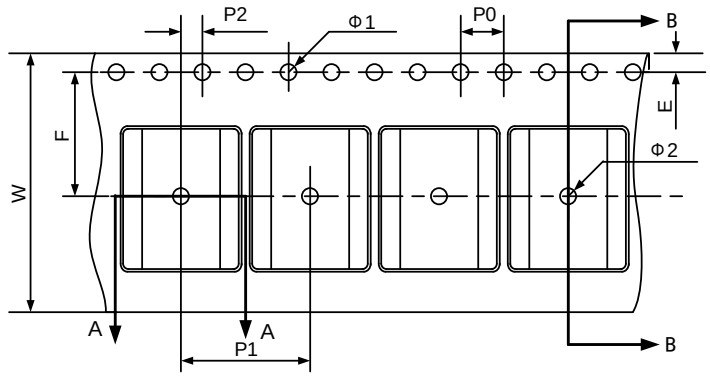
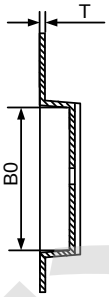
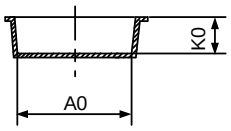
Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

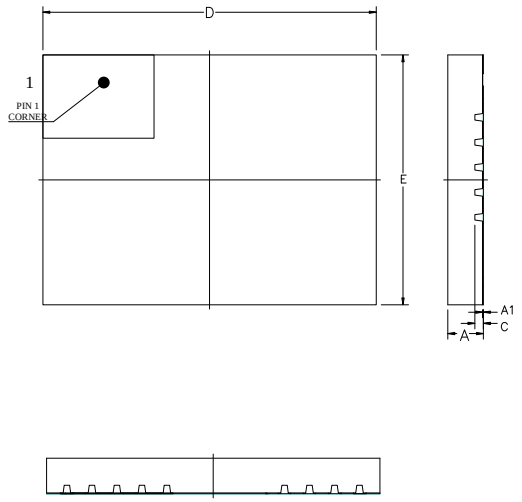
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
VQFN8*6-32	4.0±0.1	2.00±0.1	12±0.1	6.3±0.2	8.3±0.2	16±0.3	0.3±0.15	1.25±0.2	1.5±0.1	1.55±0.25	1.75±0.1	7.50±0.10

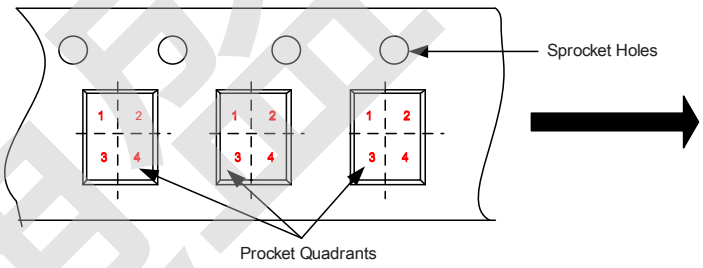
PACKAGE OUTLINE

VQFN8*6-32 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1		0.21REF	
c		0.203REF	
D	7.90	8.00	8.10
D2	2.10	2.20	2.30
D3	3.15	3.25	3.35
e		0.60BSC	
e1		2.40BSC	
e2		1.80BSC	
E	5.90	6.00	6.10
E2	4.20	4.30	4.40
E3	2.90	3.00	3.10
Ne		4.20BSC	
L	0.40	0.45	0.50
h		0.35REF	
K		0.30REF	
K1		1.50REF	
K2		0.60REF	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
VQFN8*6-32	2

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