JW1565J

Offline QR GaN Flyback Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW1565J is an isolated offline flyback PWM converter with GaN integrated, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation. An internal maximum frequency limitation is utilized to overcome the inherent disadvantages of QR flyback.

JW1565J comprises a HV pin for start-up to eliminate conventional start-up resistors and save standby mode energy consumption. It can comply with the most stringent efficiency regulations. Also, the HV pin is used for X-cap discharge when AC input is removed, which helps to reduce X-cap discharge loss and achieve extremely low standby power loss.

JW1565J is available in 6mm*8mm VDFN package. The high level of integration provides an easy to use, low component count and high efficiency application solution for isolated power delivery.

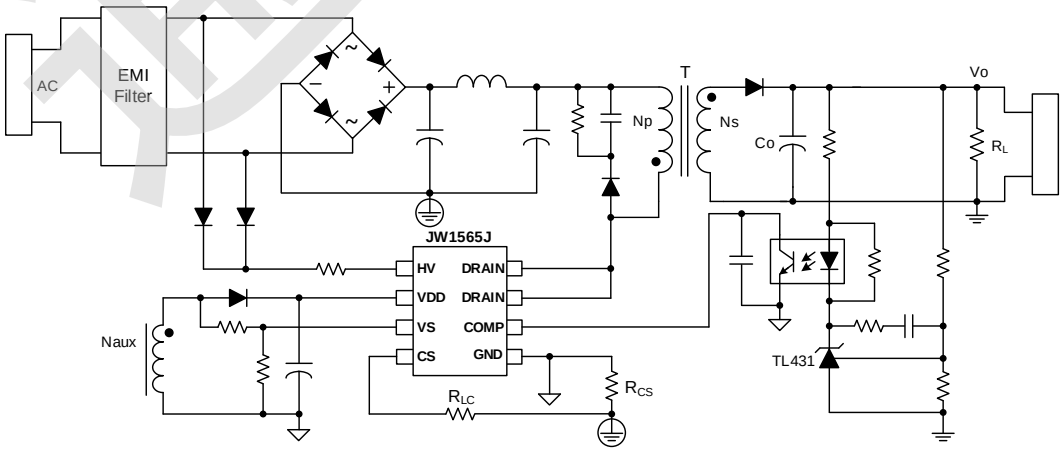
FEATURES

- Built-in High Voltage Start-up
- Integrated 700V GaN
- X-capacitor Discharge Function
- Wider VDD Operation Range
- QR Operation for High Efficiency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP, Brown-in and Brown-out, CS Open Protection, OCP, OPP, OLP, Internal OTP
- Frequency Jittering to Ease EMI Compliance
- VDFN6X8-8L Package

APPLICATIONS

- PD and QC Chargers
- AC/DC Adapters with Wide Output Range

TYPICAL APPLICATION



电话:0755-83387360 手机：13826508770（王先生） 邮箱：3007605919@qq.com 网址：www.sztssd.com 地址:深圳市福田区中航路鼎诚国际南座18楼1814室

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1565JVDFNF#TR	VDFN6X8-8L	JW1565J YW□□□□□	Green

Notes:

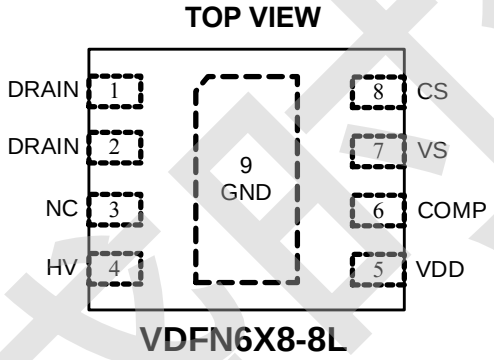
1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW□□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

DRAIN Pin 700V
HV Pin..... .....650V
VDD Pin.....95V
COMP, CS Pin .....-0.3V to 5V (-0.7V to -0.3V<10us, 5V to 5.5V<10us)
VS Pin .....-0.3V to 5V (-0.7V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2)].....150ºC
Storage Temperature .....-65ºC to +150ºC
Lead Temperature (Soldering, 10sec)..... 260ºC
Continuous Power Dissipation (T_A = +25 ºC)[3)] VDFN6X8-8L 2.5W

RECOMMENDED OPERATING CONDITIONS[4)]

VDD Voltage.....9 to 83V
Operating Junction Temperature (T_J).....-40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{JC}
VDFN6X8-8L	50	3ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1565J includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

T_A=25℃, unless otherwise stated.

Advance Information, not production data, subject to change without notice.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
High Voltage Section (HV Pin)						
Supply Current from HV Pin	I_{HV}	V_{HV}=120V, VDD=0V		3		mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=600V			30	uA
Brown-in Threshold	V_{BR_IN}	V_{HV} increasing		112		V
Brown-out Threshold	V_{BR_OUT}	V_{HV} decreasing		97		V
Brown-out Blanking Time[7]	t_{BR_OUT}	V_{HV} decreasing		62		ms
Supply Voltage Section (VDD Pin)						
Turn-on Threshold Voltage	V_{DD_ON}	V_{VDD} increasing		16.5		V
Turn-off Threshold Voltage	V_{DD_OFF}	V_{VDD} decreasing		8		V
Reset Threshold Voltage	V_{DD_RST}	Fault state		4.5		V
Start-up Current	I_{DD_ST}	V_{VDD}=V_{DD_ON}-0.5 V		300		uA
Operating Supply Current	I_{DD_OP}	V_{VDD}=45V, f_{SW}=f_{MAX}		1		mA
VDD OVP Voltage	V_{DD_OVP}	V_{VDD} increasing		90		V
Voltage Sense Section (VS Pin)						
Maximum VS Clamp Source Current	I_{VS_MAX}			2.85		mA
Adaptive Blanking Time for VS Sampling[6]	t_{VS_BLK}	V_{COMP}=0.55V		0.6		us
		V_{COMP}=4V		1.2		us
Output OVP Threshold	V_{VS_OVP}	V_{VS} increasing		3		V
Output OVP Debounce Cycle Counts[6]	N_{VS_OVP}	Fault state		3		Cycle
Current Sense Section (CS Pin)						
Max CS Offset Current	I_{CS_MAX}	V_{COMP}=4V		100		uA
Min CS Offset Current	I_{CS_MIN}	V_{COMP}=0.55V		27		uA
CS Off Threshold	V_{CS_TH}	V_{CS} decreasing		25		mV
Leading-edge Blanking Time[6]	t_{LEB}	V_{CS}=0V		220		ns
OCP Enable Threshold	V_{OCP_EN}	V_{CS} increasing		0.65		V
OCP Internal Threshold[6]	V_{OCP}			0.2		V
OCP Blanking Time[7]	T_{OCP_BLK}	Fault state		106.5		ms
Auto-restart Cycles for OCP[6]	N_{OCP_HIC}	Fault state		4		Cycle
OPP Internal Threshold[6]	V_{OPP}			0.8		V
OPP Blanking Time[7]	$t_{OPP-BLK}$	Fault state		106.5		ms

Auto-restart Cycles for OPP[6]	N_{OPP_HIC}	Fault state		4		Cycle
CS OVP Threshold[6]	V_{CS_OVP}	V_{CS} increasing		2		V
Frequency Section						
Maximum Switching Frequency	f_{MAX}	V_{COMP}=3.6V		210		kHz
Minimum Switching Frequency	f_{MIN}	V_{COMP}=1V		25		kHz
Maximum ON Time	T_{ON_MAX}			18		us
Minimum ON Time	T_{ON_MIN}			325		ns
Maximum Switching Cycle	T_{S_MAX}			61		us
Frequency Jittering Amplitude[7]	ΔF_{JIT}			±4%		
Peak Current Jittering7]	ΔI_{CS_JIT}	V_{COMP}=4V		±5%		
Counting Cycles for Jittering[7]	N_{JIT_CYC}			32		Cycle
Feedback Section (COMP Pin)						
Open Pin Voltage[6]	V_{COMP_MAX}	Open loop		4		V
Internal Pull-up Resistor[6]	R_{COMP_UP}			20		kΩ
COMP to CS Offset Current Gain[6]	G_{COMP_CS}	V_{COMP}≥V_{COMP_PFM}		20		V/mA
		V_{COMP}≤V_{COMP_PWM}		16		V/mA
Threshold Enter PFM Mode	V_{COMP_PFM}	V_{COMP} decreasing		2.8		V
Threshold Enter PWM Mode	V_{COMP_PWM}	V_{COMP} decreasing		1		V
Threshold Enter Burst Mode	V_{BUR_L}	V_{COMP} decreasing		0.5		V
Threshold Exit Burst Mode	V_{BUR_H}	V_{COMP} increasing		0.6		V
Over Load Protection Threshold[6]	V_{OLP}	V_{COMP} increasing		3.7		V
OLP Blanking Time[7]	t_{OLP_BLK}	Fault state		106.5		ms
Auto-restart Cycles for OLP[6]	N_{OLP_HIC}	Fault state		4		Cycle
GaN Section						
Drain-source On-state Resistance	R_{DS_ON}	V_{GS}=6V, I_D=3A, T_J=25℃		165	240	mΩ
		V_{GS}=6V, I_D=3A, T_J=150℃		360		mΩ
Internal Over Temperature Protection						
Thermal Shutdown Threshold[7]	T_{OTP}			140		°C
OTP Hysteresis[7]	T_{HYS}			30		ºC

Note:

6) Guaranteed by design;

7) Derived from bench characterization. Not tested in production..

PIN DESCRIPTION

PIN VDFN6×8-8L	NAME	DESCRIPTION
1, 2	DRAIN	Drain terminal of the internal GaN.
3	NC	
4	HV	High voltage input pin. This pin provides a source current to charge VDD capacitor for start-up. It is used for X-cap discharge when the AC input is removed. Besides, this pin also senses input voltage for brown-in and brown-out protection.
5	VDD	Bias power input of the controller. A hold-up capacitor to GND is required.
6	COMP	Feedback input pin for QR flyback controller. Connected to an opto-coupler directly.
7	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP. This pin also detects the resonant valley to implement QR operation.
8	CS	Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP function at the initial start.
9	GND	Ground of the IC.

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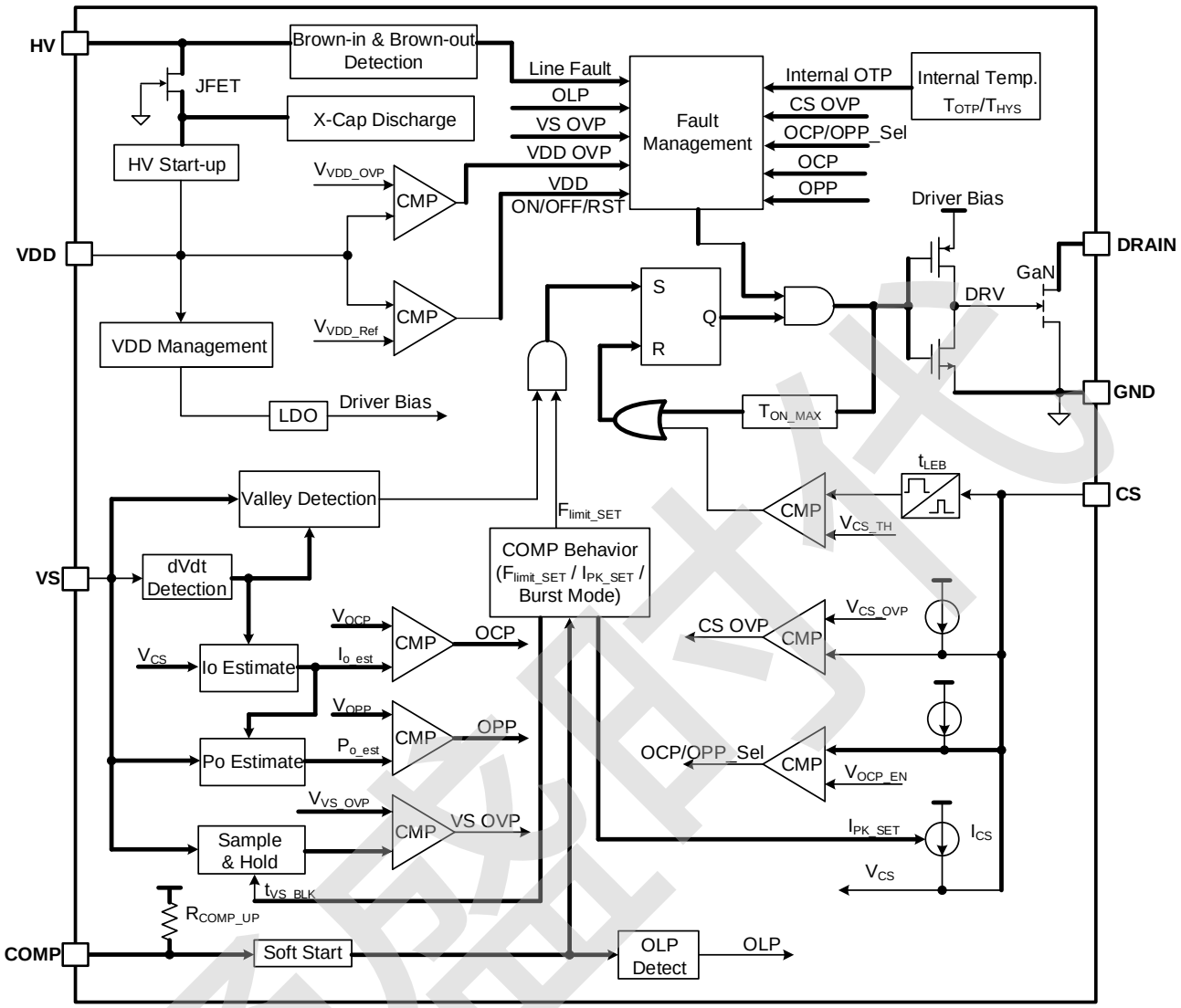
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW1565J is an offline flyback converter with GaN integrated, which features multi-mode quasi-resonant (QR) operation. With a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

JW1565J has an inherent frequency Jittering mechanism to improve EMI performance under QR operation.

1. Start-up

1.1 High Voltage Start-up

When HV pin is connected to AC rectified voltage, a current source which is drawn from HV pin charges VDD capacitor. As soon as VDD pin voltage reaches turn-on threshold V_{DD_ON}, the controller starts switching and internal start-up circuit is disabled. The controller stops switching and start-up current source is turned on again when a fault is triggered or VDD voltage falls below V_{DD_OFF}.

1.2 Soft-start

An internal soft start circuit is included in JW1565J in order to establish the output voltage smoothly during start-up and reduce the stress of primary and secondary side power devices. The feedback signal V_{COMP} rising gradually from the minimum level to the maximum level within 4ms. Each restart sequence is followed by a soft start.

2. Normal Operation

JW1565J is a multi-mode QR converter with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Figure 1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Figure 1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to f_{MAX}. For medium-load range, Pulse Frequency Modulation (PFM) is used, and primary peak current is nearly fixed to achieve high efficiency. When load is further reduced, switching frequency is fixed at f_{MIN} along with primary peak current varying from 50% of its maximum value to I_{CS_MIN}. When the system is at very light load condition, JW1565J will enter the burst mode. When V_{COMP} drops below V_{BUR_L}, gate driver stops. And resume when V_{COMP} rises over V_{BUR_H}. Otherwise the GaN remains at off state to minimize the switching loss and reduce the standby power consumption. The controller completes the automatic transition between different modes according to V_{COMP}.

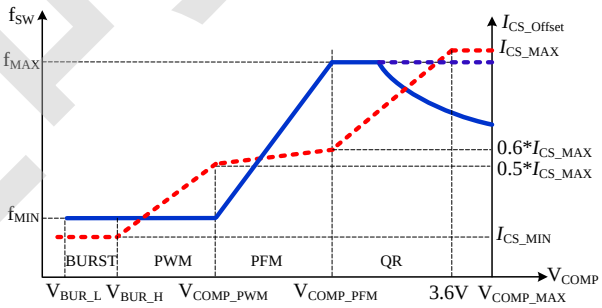


Figure. 1 Frequency & Ics Modulation

3. Other Functions and Features

3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering is integrated in JW1565J. Jittering around the central value with amplitude of ΔF_{JIT} and ΔI_{CS_JIT}. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Leading-edge Blanking (LEB)

In order to avoid the premature termination of switching pulse due to the parasitic capacitance,

an internal leading-edge blanking is used between CS pin and the input of internal current comparator. The current comparator is disabled and can't turn off the internal GaN during the blanking time. Figure 2 shows the leading-edge blanking time.

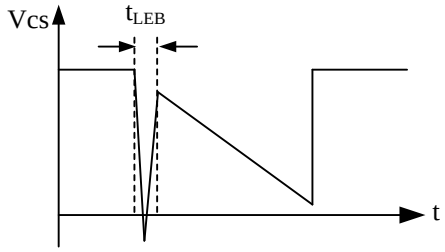


Figure. 2 LEB Time

3.3 CCM Preventing

For JW1565J, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after a T_{S_MAX} to make sure the system operates in DCM.

3.4 X-Cap Discharge Function

Safety standards such as EN60950 and UL62368 require that any X-caps in EMI filters on the AC side of the bridge rectifier quickly discharge to a safe level when AC is disconnected. Standards require that the voltage across X-caps decay with a maximum time constant of 2s. Typically, this requirement is achieved by a resistive discharging element in parallel with X-caps. However, this resistance will cause a continuous power dissipation that impacts the standby power consumption.

In order to reduce standby power consumption, JW1565J incorporates a X-cap discharge circuit. This circuit periodically monitors the voltage across X-caps to detect any possibility that AC cord is unplugged, and then discharge the X-caps by internal HV discharging current source to a safe level within 2s. Figure 3 shows the X-cap discharge timing.

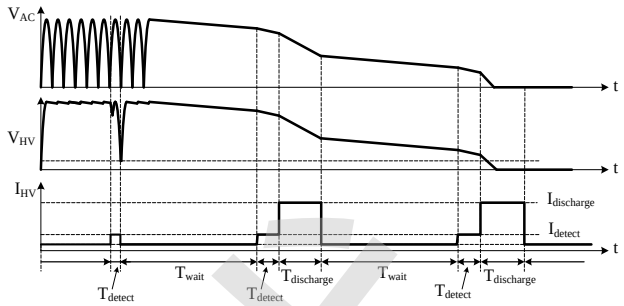


Figure. 3 X-cap Discharge Timing

3.5 VS Blanking Time

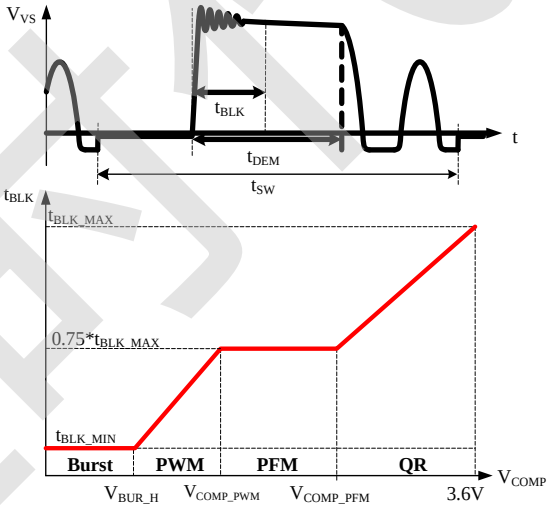


Figure. 4 VS Blanking Time

VS spikes are affected by the amplitudes of primary current and inductance, so VS blanking time should be set to vary with V_{COMP}. Ensure that the secondary side conduction time is greater than the VS Blanking Time t_{BLK}.

4. Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above V_{CS_OVP}, a CS pin open fault triggered. The controller shuts down, then VDD resets and fault restart cycle begins.

4.2 Input Brown-in and Brown-out

JW1565J senses HV pin voltage to realize brown-in and brown-out function. When HV pin voltage is higher than V_{BR_IN}, the V_{VDD} pulls down to V_{DD_OFF} with a typical 5mA pull-down current. When V_{VDD} reaches V_{DD_ON} again, the controller starts switching. And the controller is disabled when HV pin voltage is lower than V_{BR_OUT} for brown-out blanking time t_{BR_OUT}. The blanking time is set long enough to ignore a two cycle AC voltage drop out. The timer starts counting once HV pin voltage drops below V_{BR_OUT}.

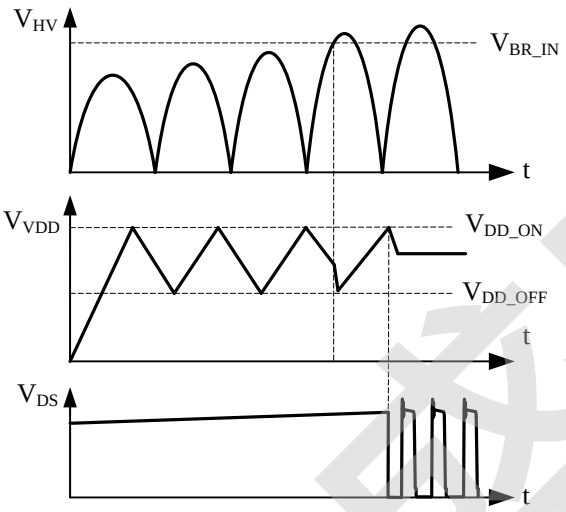


Figure. 5 Brown-in at HV pin

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sampled on VS pin exceeds V_{VS_OVP} for three consecutive switching cycles, VS OVP fault is asserted and the controller shuts down, then VDD resets and fault restart cycle begins.

4.4 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage varies widely. So OCP should be disabled, and enable the alternative OPP function. JW1565J senses CS voltage at the initial of soft-start to determine whether to enable OCP or OPP function, as Figure 6 shows. At the initial 100us, an OCP or OPP selection current I_{SEL} typical 100uA is applied to CS pin. If CS voltage exceeds a preset enable threshold V_{OCP_EN}, OPP is enabled and OCP is disabled. Otherwise, OPP is disabled and OCP is enabled.

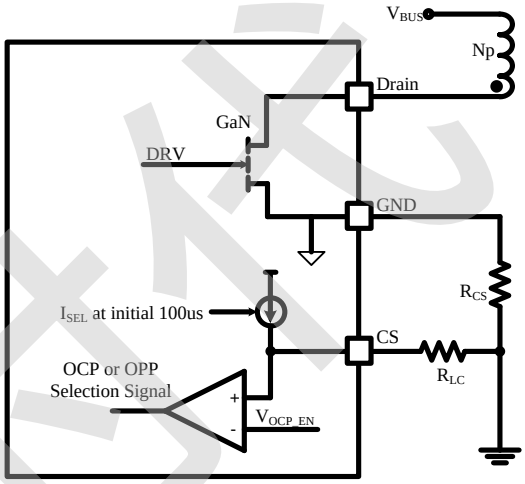


Figure. 6 OCP or OPP Selection Circuit

4.5 OCP

If OCP is enabled, JW1565J compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the primary side current information V_{CS_PK} is sampled and hold for output current calculation.

As shown in Figure 7, it calculates output current based on the secondary side current conduction time T_{ons} and primary side current information V_{CS_PK}. If the calculated output current signal higher than the internal OCP threshold V_{OCP} for t_{OCP_BLK}, IC triggers OCP protection.

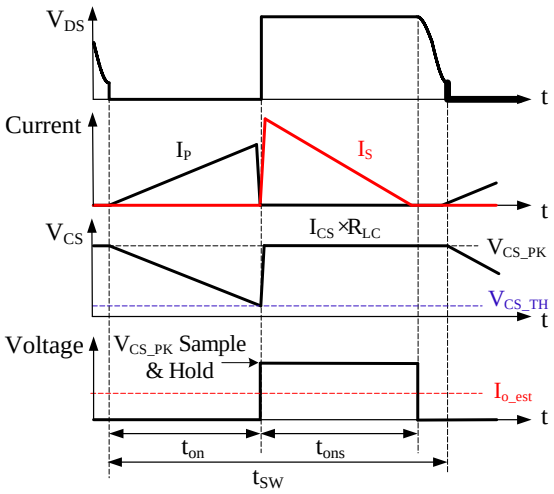


Figure. 7 Output Current Estimation

So the OCP point can be set as:

$$I_{OCP} = \frac{V_{OCP} \cdot (1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}) \cdot N_P}{2 \cdot R_{CS} \cdot N_S}$$

where, N_P is the turns number of primary winding, N_S is the turns number of secondary winding, R_{CS} is the current sensing resistance.

When an OCP fault is asserted, the controller shuts down and initiates fault restart cycle. In order to reduce the power consumption of the circuit, VDD voltage needs to hit V_{DD_OFF} four times, and then the controller restarts at the fifth cycle.

4.6 OPP

If OPP is enabled, JW1565J compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to VS voltage. So the output power can be expressed as:

$$P_{out} = \frac{(V_{CS\_PK} - V_{CS\_TH}) \cdot t_{ons} \cdot N_P}{2 \cdot R_{CS} \cdot t_{sw} \cdot N_S} \cdot \frac{VS \cdot N_S}{N_{AUX}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

And the OPP point can be set as:

$$P_{OPP} = \frac{V_{OPP} \cdot (1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}) \cdot N_P}{2 \cdot R_{CS} \cdot N_{AUX}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

where, N_{AUX} is the turns number of auxiliary winding, R_{UP} and R_{DOWN} are the resistances of the outside resistor divider of VS pin.

If the calculated output power signal is higher than the internal OPP threshold V_{OPP} for t_{OPP_BLK}, IC triggers OPP protection. When an OPP fault is asserted, the controller shuts down and and initiates fault restart cycle. In order to reduce the power consumption of the circuit, VDD voltage needs to hit V_{DD_OFF} four times, and then the controller restarts at the fifth cycle.

4.7 Over Load Protection

If the voltage on COMP pin continues exceeds the over-load protection threshold V_{OLP} longer than t_{OLP_BLK}, an OLP fault is asserted. The controller shuts down, VDD voltage needs to hit V_{DD_OFF} four times, then the controller restarts at the fifth cycle.

4.8 VDD OVP

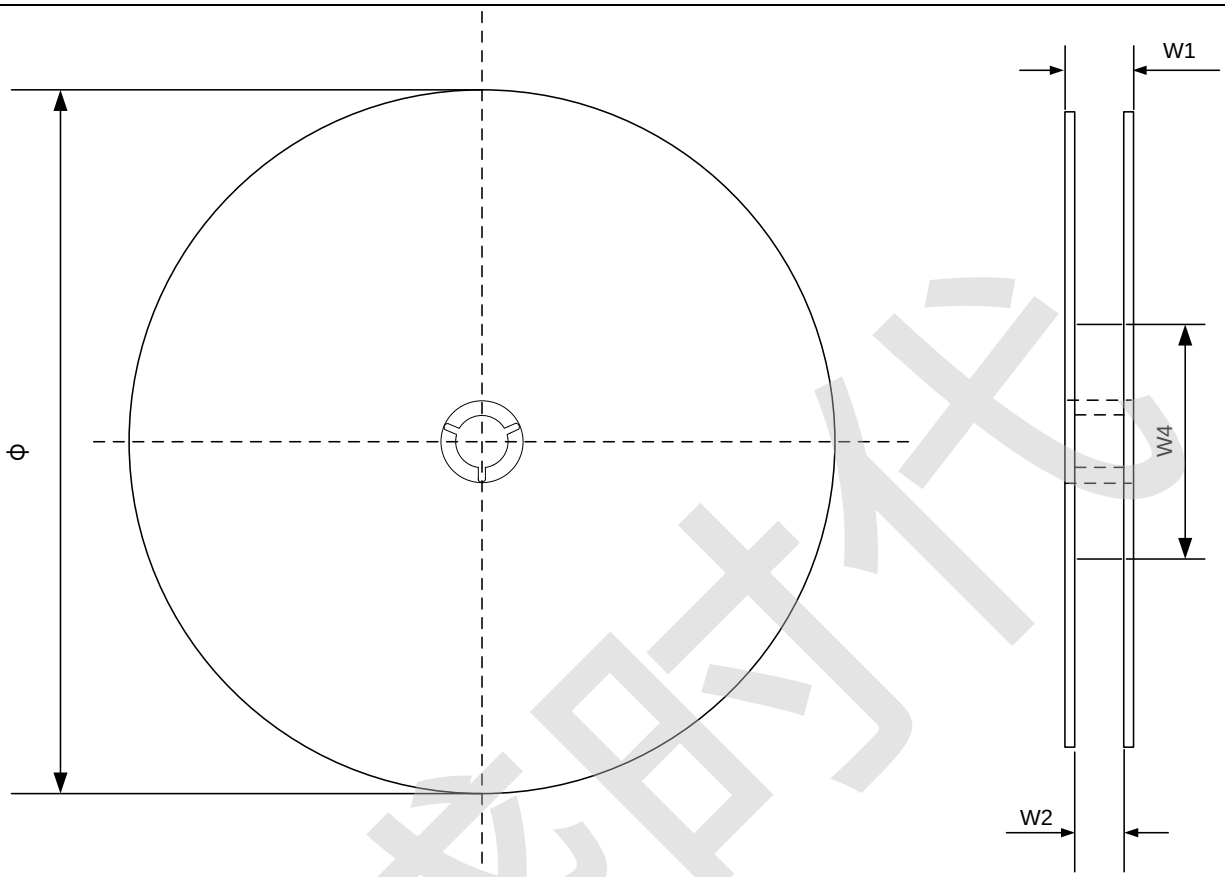
If the voltage on VDD pin continuously exceeds the over voltage protection threshold V_{VDD_OVP} more than typical 100us, a VDD OVP fault is asserted. The controller shuts down, then VDD reset and fault restart cycle begins.

4.9 Internal OTP

The internal over temperature protection threshold is T_{OTP}. If the junction temperature of the converter reaches this threshold, the converter shuts down. Since the OTP hysteresis is 30°C typically, when the junction temperature falls below 110°C, the converter initiates the UVLO reset and re-starts fault cycle.

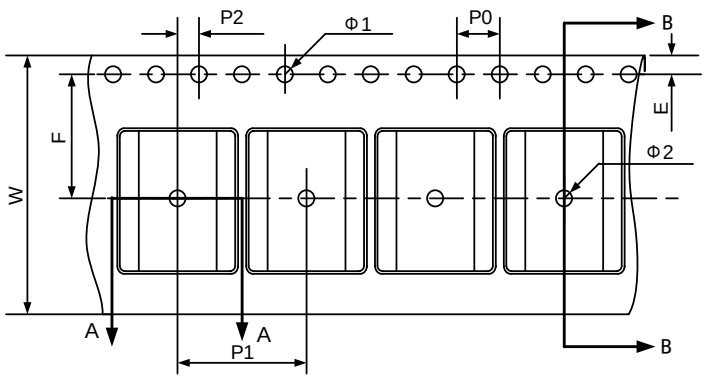
TAPE AND REEL INFORMATION

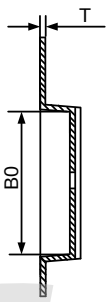
Reel UNIT: mm



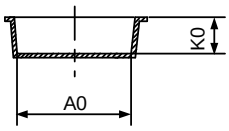
Package	Diameter Φ(mm)	Thickness W1(mm)	Width W2(mm)	W4(mm)
VDFN6X8-8L	330±2	23.4±2	16.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions(mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
VDFN6X8-8L	4.0±0.1	2.0±0.1	12±0.1	6.3±0.2	8.3±0.2	16±0.3	0.3±0.2	1.05±0.2	1.55±0.1	1.5±0.25	1.75±0.1	7.5±0.10

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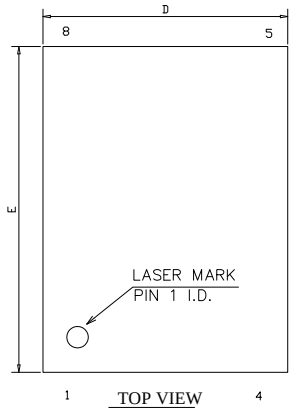
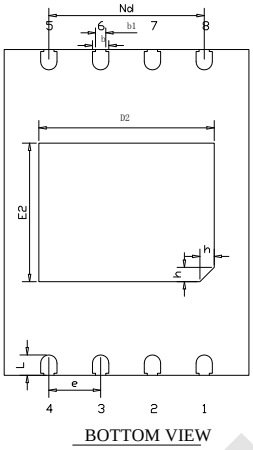
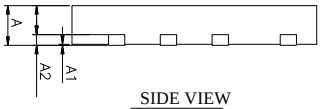
PACKAGE OUTLINE

VDFN6X8-8L Unit: mm

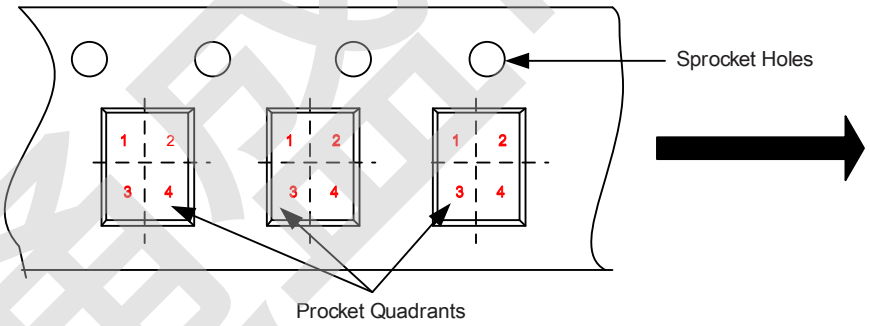




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.18	0.203	0.25
b	0.35	0.40	0.45
b1		0.25REF	
D	5.90	6.00	6.10
Nd		3.81BSC	
e		1.27BSC	
E	7.90	8.00	8.10
D2	4.20	4.30	4.40
E2	3.30	3.40	3.50
L	0.45	0.50	0.55
h	0.30	0.35	0.40



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
VDFN6X8-8L	2

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