JW1532A

High Efficiency Off-line CV Regulator

DESCRIPTION

The JW1532A is a high efficiency low cost off-line constant voltage regulator for Buck and Buck-Boost topology with 650V MOSFET.

JW1532A can output 18V/12V default voltage with few external components, which decreases the system cost. In light load condition, JW1532A operates in green mode, in which the inductor peak current and the switching frequency is lower than that of full load to improve the system efficiency and the reference voltage is decreased to ensure good load regulation.

JW1532A has multi-protection functions which largely enhance the safety and reliability of the system, including VDD under-voltage lockout (UVLO), short circuit protection (SCP), pulse-by-pulse current limit, over load protection (OLP) and over-temperature protection (OTP).

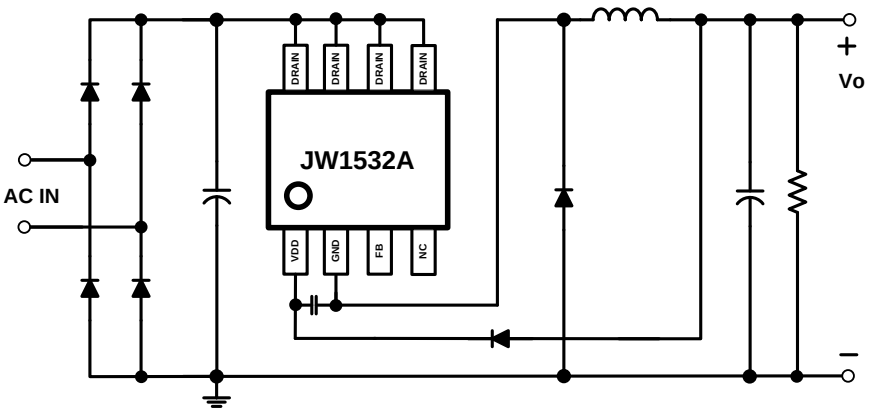
FEATURES

- Ultra Low System BOM Cost
- Integrated with 650V, Low R_{dson} MOSFET
- 18V/12V Default Output Voltage
- <30mW No-Load Power Consumption
- Support Buck and Buck-Boost Topology
- Peak Current Mode Control
- Frequency Jittering for Good EMC
- High Efficiency Over Wide Operating Range
- Output Voltage Load Regulation Compensation
- VDD UVLO
- Short Circuit Protection
- Pulse-by-pulse Current Limit
- Over Temperature Protection
- SOP8 Package

APPLICATIONS

- Home Appliance
- Standby Power
- Consumer Electronics

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1532ASOPB#TR	SOP8	JW1532A YW□□□□□	Green

Notes:

1) JW□□□□#TR
- TR means Tape and Reel
- Package Code
- Part No.

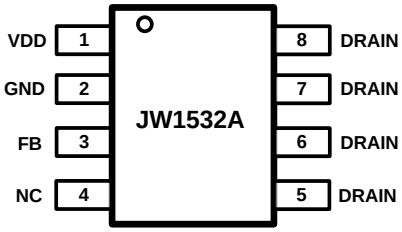
2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VDD Voltage to GND .....-0.3V to 22V,22V to 28V<1s
DRAIN Voltage to GND.....-0.3V to 650V
FB Voltage to GND……...……...…….-0.3V to 6.5V
Junction Temperature[2) 3)] 150ºC
Lead Temperature..... 260ºC
Storage Temperature..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model) 2.5kV

RECOMMENDED OPERATING CONDITIONS

DRAIN Voltage to GND.....600V

Operating Junction Temperature (T_J) .....-40ºC to 125ºC

Package	Recommended MAX Output Current (T_J=125℃) 4)
SOP8	300mA

THERMAL PERFORMANCE 5)

θ_{JA} θ_{JC}

SOP8.....96.....45ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.

2) The JW1532A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum output current is recommended in the application according to chip junction temperature T_J=125℃ (chip case temperature difference about 20℃). The maximum output current could be increased properly if the heat dissipation is better.

5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

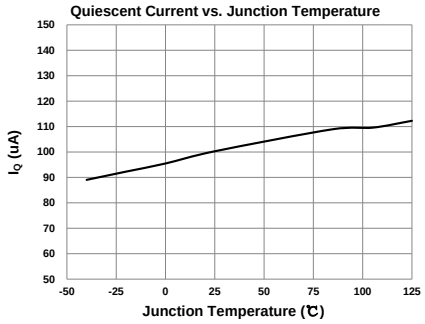
T_A=25℃, unless otherwise stated.

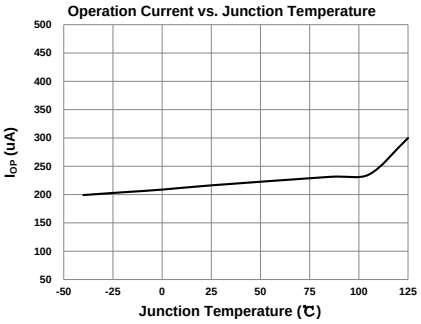
Item	Symbol	Condition	Min.	Typ.	Max.	Units
VDD Quiescent Current	I_Q	V_{DD_ST} -1V	75	100	125	μA
Operation Current	I_{OP}	V_{DD_ST} +1V	200	215	230	uA
VDD Charge Current	I_{CH}	VDD=5V	0.8	1	1.2	mA
VDD Startup Voltage	V_{DD_ST}		9.0	9.5	10.0	V
VDD Under Voltage Lockout	V_{DD_UVLO}		7.0	7.2	7.5	V
VDD Clamping Voltage	V_{CLP}	Sink current =5mA	23	24	25	V
VDD Feedback Reference	V_{DDREF}	FB floating	18.042	18.6	19.158	V
		FB short to GND	12.028	12.4	12.772	V
Peak Current Limit	I_{PK}		0.5	0.6	0.75	A
Oscillator Frequency	f_{osc}		60	70	80	kHz
Frequency Jittering Range[6)]	$\lvert\pm\Delta f/f_{OSC}\rvert$			8		%
Frequency Jittering Period [6)]	T_{Jit}			15		ms
Maximum On Time	T_{ONMAX}		7	8.5	9.5	μs
Leading Edge Blanking Time	T_{LEB}			400		ns
MOS Breakdown Voltage	BV		650	690		V
MOS Rdson	Rdson	Vgs=10V		13		Ω
Over Thermal Protection Threshold[6)]				150		℃
Over Thermal Protection Recovery Hysteresis[6)]				30		℃

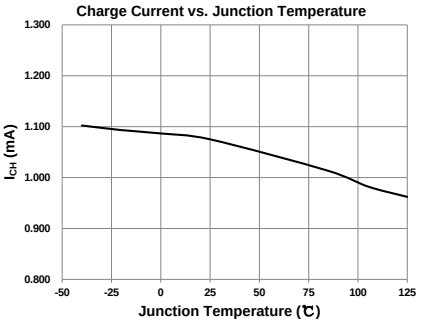
Note：

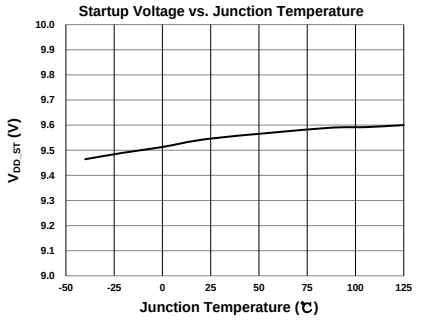
6) Guaranteed by design.

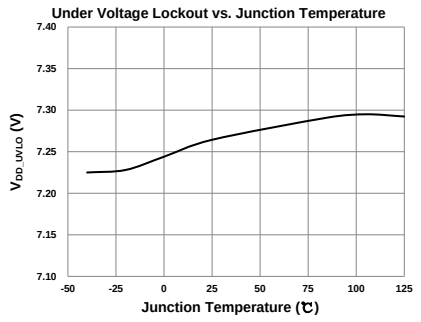
TYPICAL CHARACTERISTICS

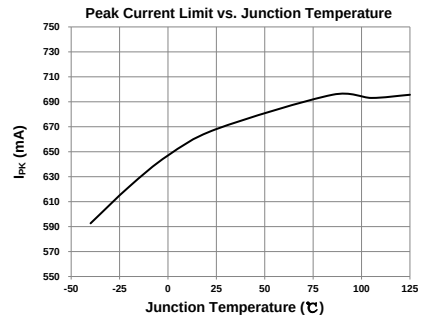


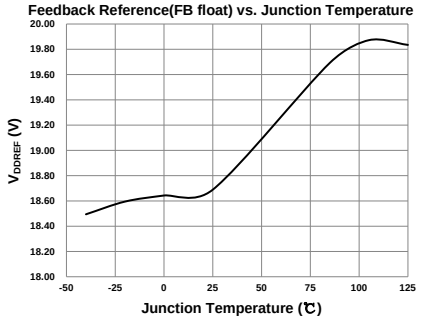


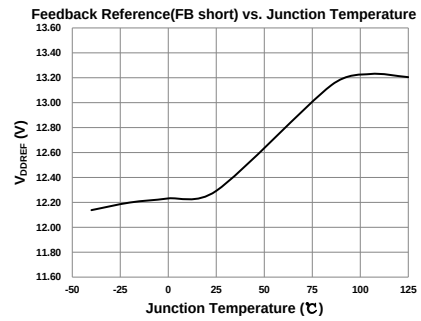


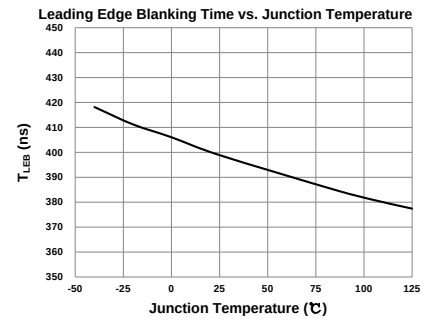


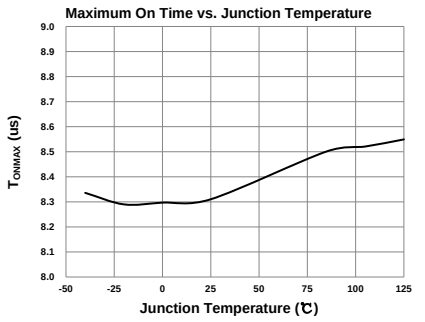


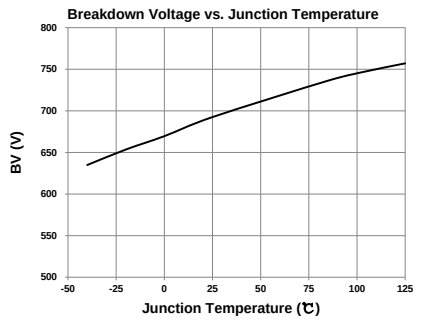


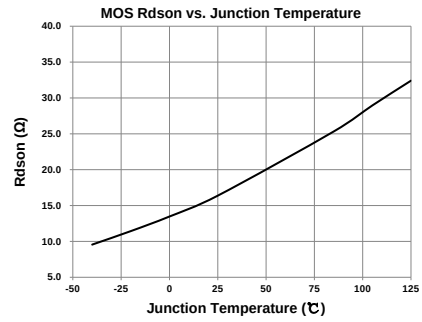








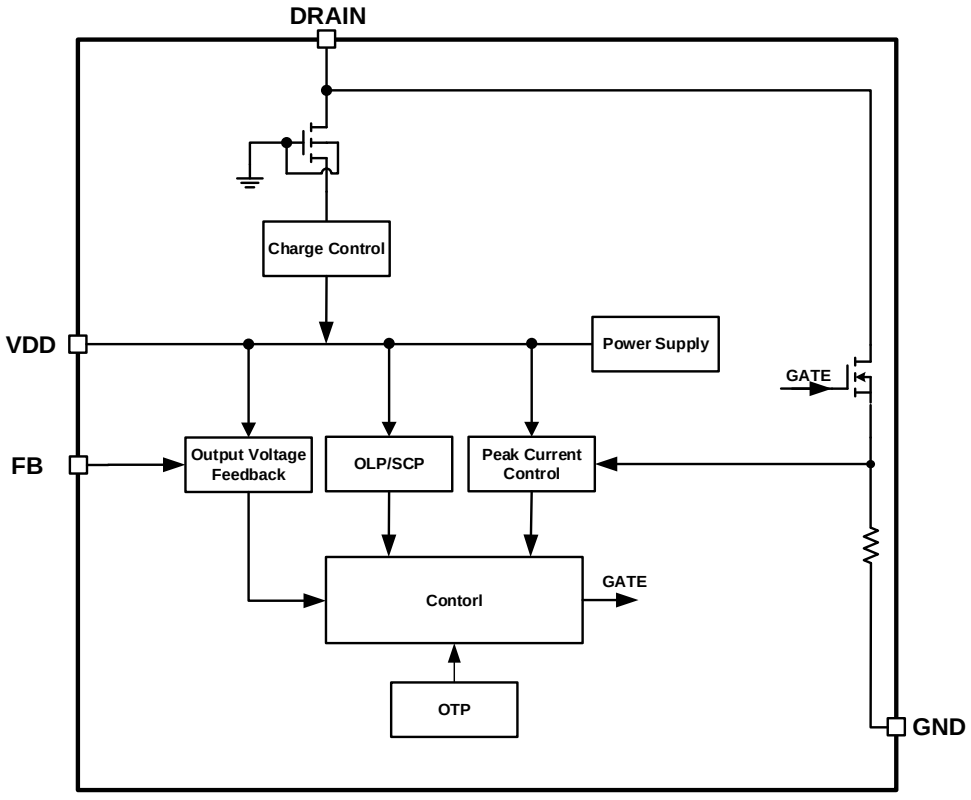




PIN DESCRIPTION

Pin SOP8	Name	Description
1	VDD	IC power supply and output voltage feedback
2	GND	IC ground
3	FB	Output voltage setup, FB floating-18V, FB short to GND-12V
4	NC	
5	DRAIN	Internal MOS drain and HV power supply
6	DRAIN	Internal MOS drain and HV power supply
7	DRAIN	Internal MOS drain and HV power supply
8	DRAIN	Internal MOS drain and HV power supply

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW1532A is a high efficiency low cost off-line constant voltage regulator for Buck and Buck-Boost topology.

Start Up

JW1532A can be supplied from MOS DRAIN directly. When the internal high voltage(HV) power souse charges VDD up to the V_{DD_ST}, the gate driver starts to switch. VDD will be powered by output voltage in steady state. Once the voltage of VDD is lower than V_{DD_UVLO}, JW1532A stops switching.

Peak Current Control

JW1532A has the default peak current for output current. And it also has the SCP limit peak current for abnormal state such as inductance short.

Constant Voltage Control

The output voltage is sensed by VDD pin and adjusted by internal control compensation loop automatically.

The switching frequency of JW1532A is fixed to f_{osc} with $\pm$ 8% jittering to improve the EMI performance.

Output voltage can be selected by FB pin setup. If FB is floating, output voltage is 18V, if the FB pin is short to GND, output voltage is 12V.

Green Mode

In light or no load condition, JW1532A operates in DCM which means the OFF time is very long. JW1532A will reduce the peak current of the inductor to minimize the power loss. The longer Toff, the lower I_{PK}.

Short Circuit Protection (SCP)/ Over Load Protection (OLP)

In short circuit or over load condition, VDD can't be charged to V_{REF}. JW1532A will operate in auto-restart mode which is represented in the following description if VDD<V_{REF} for some time.

Auto-restart Mode

JW1532A will enter auto-restart mode if SCP/OLP/OTP is triggered. The chip stops switching and the HV power source is disconnected until VDD decreases to V_{DD_UVLO}. If VDD is charged to V_{DD_ST} for several cycles, the system restarts.

Over Temperature Protection

When internal temperature of the chip exceeds 150°C, JW1532A operates in auto-restart mode to help the chip cooling.

PCB Design

1. The VDD pin must be locally bypassed with a capacitor.
2. Make the area of the power loop as small as possible in order to reduce the EMI radiation.

APPLICATION INFORMATION

Input Capacitor

The input capacitor supplies the regulator's DC input voltage. Figure 1 shows the typical half-wave rectifier's DC bus voltage waveform.

Typically, the use of a half-wave rectifier requires an input capacitor rated at 2~4μF/W for the universal input condition(85~265VAC). When using a full-wave rectifier, the input capacitor is chosen as 1~2μF/W for the universal input condition. Avoid using an input capacitor that is too small, since it may not hold the DC voltage high long enough. A too low DC input voltage can lead to bad thermal performance.

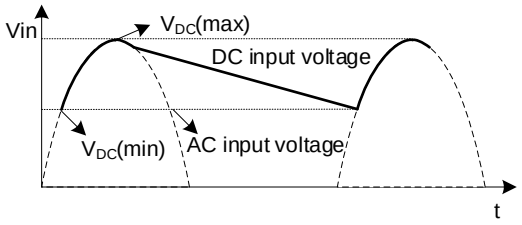


Figure 1: Half-wave rectifier

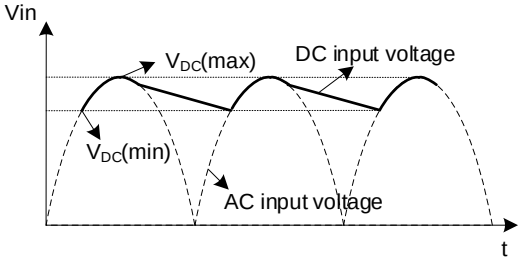


Figure 2: Full-wave rectifier

Freewheeling Diode

Choose a diode with a maximum reverse voltage rating that exceeds the maximum input voltage, and a current rating that exceeds the output current. The reverse recovery of the freewheeling diode can affect the efficiency and circuit operation.

Select an ultra-fast diode, such as the ES1, UGC10JH and so on.

Feedback Diode

Figure 3 shows the typical application schematic. The output voltage is sensed by VDD pin and adjusted by internal control compensation loop automatically. Internal controller adjust peak current and switch frequency according to VDD voltage.

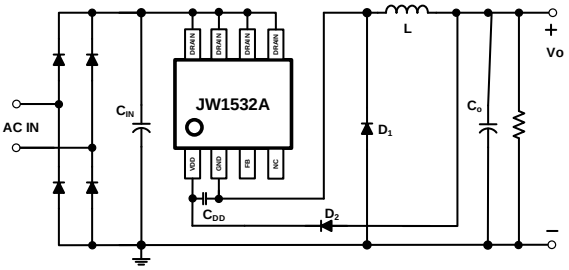


Figure 3: Typical application schematic

The relationship between VDD and VO can be expressed as:

$$V_{DD} = V_O + V_{D1} - V_{D2}$$

In light or no load condition $V_{D1} \approx V_{D2}$, In heavy load condition $V_{D1} > V_{D2}$, internal compensation loop adjusted VDD feedback reference voltage to make V_O stable.

Choose a diode with a maximum reverse voltage rating that exceeds the maximum input voltage, the reverse recovery of the feedback diode can affect the load regulation.

Select a slow diode, such as the M7 or similar characteristic diode are suggested.

Feedback Capacitor

The feedback capacitor provides two functions: sample-and-hold and IC power supply. Small capacitors result in poor regulation at light load condition, and large capacitors can effect circuit operation. Estimate the capacitor range as per the following equation:

$$\frac{I_{OP} \cdot C_O}{I_O} < C_{VDD} < \frac{5 \cdot I_{OP} \cdot C_O}{I_O}$$

Generally select C_{VDD}=0.2~1μF based on experience and adjust the value according practical application parameters.

Output Capacitor

The output capacitor maintains the DC output voltage. Estimate the output voltage ripple as:

$$C_O = \frac{I_{PKMAX} - I_O}{4 \cdot f_{SMAX} \cdot [\Delta V_O - 2 \cdot (I_{PKMAX} - I_O) \cdot \mathrm{R}_{ESR}]}$$

Generally select C_O=1μF/mA based on experience.

Dummy Load

A dummy load maintains the load regulation. And ensures sufficient inductor energy to charge the feedback capacitor to detect the output voltage. Start with a 1mA dummy load and adjust as necessary for better load transient performance.

Inductor

The JW1532A has a maximum fs limit and the peak current limit is fixed, the maximum power increases as the inductance value of the power inductor increases. Using a small inductance may lead to insufficient output power. Tolerance of the peak-current limit and maximum fs limit should also be considered for mass production. Estimate the inductor range as per the following equation for CCM:

$$I_O = I_{PKMAX} - \frac{(V_{IN} - V_O)(V_{D1} + V_O)}{2 \cdot Lm \cdot V_{IN} \cdot f_{SMAX}}$$

Figure 4 shows the curve for the universal input condition(85~265VAC).

The JW1532A has a minimum Ton limit to avoid prematurely switching pulse termination due to the parasitic capacitance. So, a too small inductance may lead to current saturation. Figure 5 shows the minimum inductance value curve for the universal input condition.

Use a standard off-the-shelf inductor to reduce costs. The saturation current of inductor should not less than 1.5 times that of I_{PKMAX}.

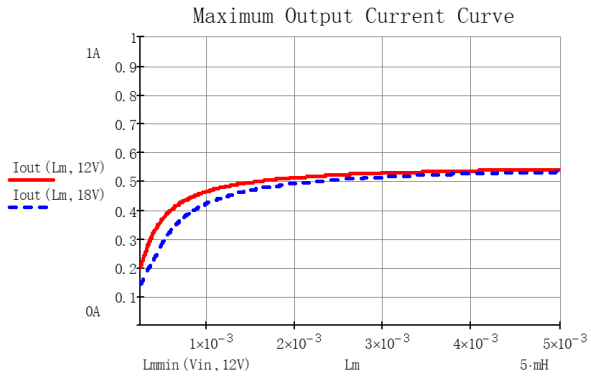


Figure 4: Curve for maximum Iout vs Lm

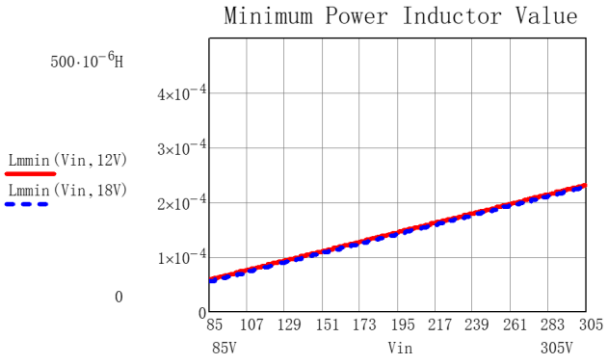


Figure 5: Curve for minimum Lm vs Vin

Surge Performance

The input capacitor and filter can also be used for surge suppression. If an appropriate input circuit is chosen, the JW1532A may pass the low level surge test without any other surge suppression components. Figure 6 shows the typical full-wave rectifier used in low-power offline applications. Table 1 shows the capacitance that the JW1532A requires under normal conditions for different surge levels. L1 is 3.3mH for this recommendation and FR is recommended 10Ω, C_{IN} is recommended 3.3μF.

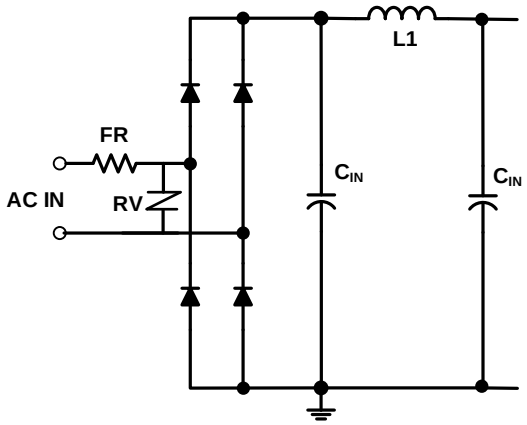


Figure 6: Full-wave rectifier

Table 1: Recommended RV and fuse resistance

RV	FR	2kV	2.5kV	3kV	3.5kV	4.5kV
/	1W	Pass	-	-	-	-
/	2W	Pass	Pass	-	-	-
7D471	1W	Pass	Pass	Pass	Pass	-
7D471	2W	Pass	Pass	Pass	Pass	Pass

Layout Guide

PCB layout is very important to achieve reliable operation, good EMI, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the loop area formed by the input capacitor, IC part, freewheeling diode, inductor and output capacitor.

2) Place the power inductor far away from the input filter.

3) The VDD pin must be locally bypassed with a capacitor.

4) Connect the exposed pad with the Drain pin to a large copper area to improve thermal performance.

Figure 7 shows the top layer and figure 8 shows the bottom layer.

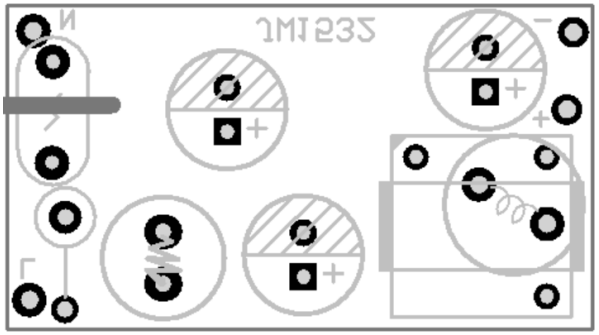


Figure 7: Top layer

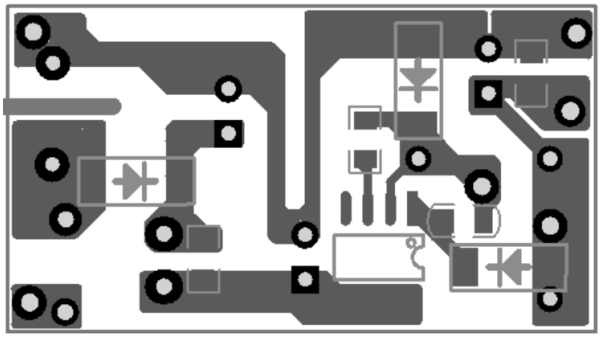


Figure 8: Bottom layer

APPLICATION REFERENCE

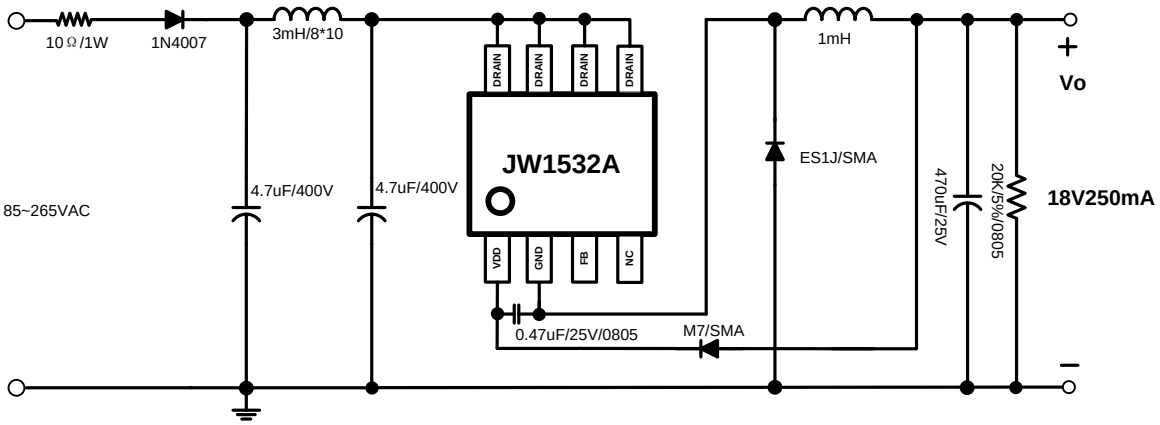
Note: Information in the following reference design sections is not part of JoulWatt component specification. Customers are responsible for determining suitability of components chosen for their purposes and should validate their design implementation to make sure the proper system functionality.

The reference design is suitable for non-isolated buck power supply default 18V output, using JW1532A.

V_{IN}: 85~265VAC

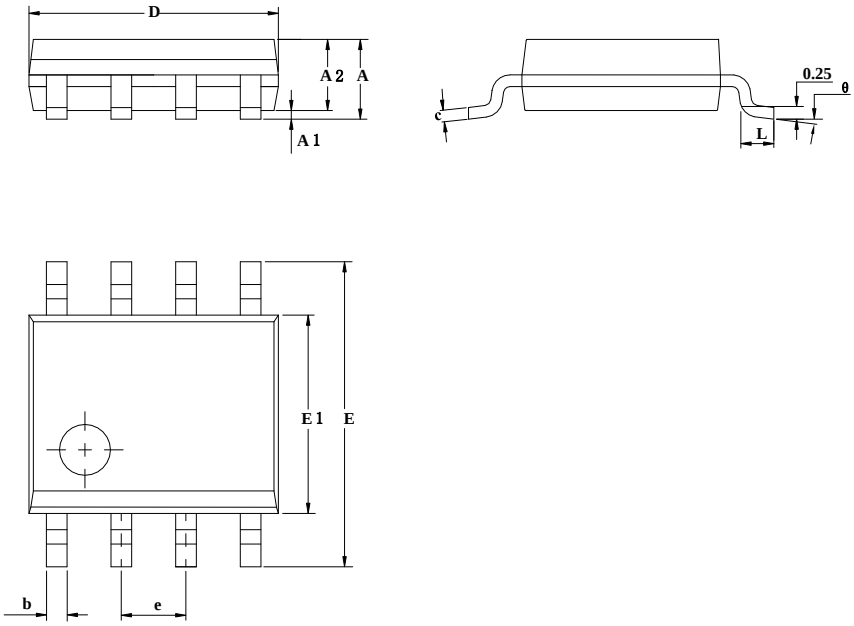
V_{OUT}: 18V

I_{OUT}: 250mA



PACKAGE OUTLINE

SOP8 **UNIT :** mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

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