JW15158D

Offline QR GaN Flyback Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW15158D is an isolated offline Flyback converter with GaN integrated, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation, and an internal maximum frequency limitation to overcome the inherent disadvantages of QR Flyback.

JW15158D combines PWM and PFM control at different input and load condition for highest average efficiency. It can comply with the most stringent efficiency regulations.

JW15158D comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption. JW15158D is available in HSOP-7 package. The high level of integration results in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

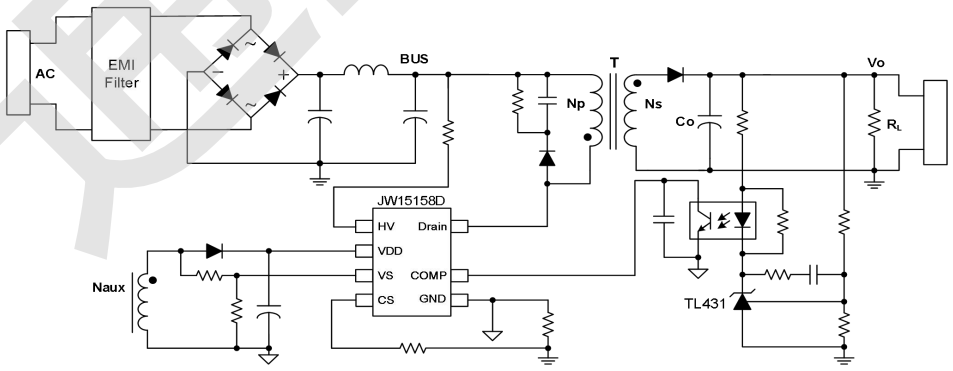
FEATURES

- Integrated 700V 600mΩ GaN
- Built-in High Voltage Start-up (700V)
- Wider VDD Operation Range (Up to 90V)
- QR Operation for High Efficiency
- Maximum 110kHz Switching Frequency
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP and UVP, Brown-In, CS Open Protection, Internal OTP
- Frequency Jitter to Ease EMI Compliance
- Available in HSOP-7 Package

APPLICATIONS

- PD and Quick-Charging Chargers
- AC/DC Adapters with Wide Output Range

TYPICAL APPLICATION



JW15158D Typical Application

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW15158DHSOPC#TR	HSOP-7	JW15158D YW□□□□□	Green

Notes:

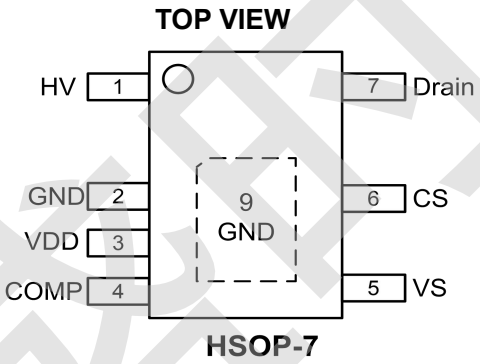
1) JW□□□□#TR
- #TR: Tape and Reel (If TR is not shown, it means Tube)
- □□□□: Package Code
- JW: Part No.

2) Line1: JW □□□□
- □□□□: Product code
- JW: Joulwatt LOGO

Line2: YW □□□□□
- □□: Lot number
- □□: Week code
- □: Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

Drain Pin 700V
HV Pin 600V
VDD Pin 90V
COMP, CS Pin ..... -0.3V to 5V (5V to 5.5V<10us)
VS Pin ..... -0.3V to 5V (-0.7V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature2) 3) 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC
Continuous Power Dissipation (TA = +25 ºC) 4) HSOP-7 ..... 2.5W

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RECOMMENDED OPERATING CONDITIONS

VDD Voltage ..... 8V to 88V
Operating Junction Temperature (TJ) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{Jc}
HSOP-7	50	10ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) JW15158D includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA.

5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

TA = 25ºC, unless otherwise stated.
Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
High Voltage Section (HV Pin)						
Supply Current from HV Pin	I_{HV}	V_{HV}=120V, VDD=0V		3		mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=500V, VDD=20V		20		uA
Brown-in Threshold	V_{BR_IN}			112		V
Brown-out Threshold	V_{BR_OUT}			98		V
Brown-out Blanking Time[7]	t_{BR_OUT}			70		ms
Supply Voltage Section (VDD Pin)						
Turn-on Threshold Voltage	VDD_ON	VDD Rising		16.5		V
Turn-off Threshold Voltage	VDD_OFF	VDD Falling		7.8		V
Reset Threshold Voltage	VDD_RST			4.75		V
Startup Current	IDD_ST	VDD=VDD_ON-0.5 V,		300		uA
Operating Supply Current	IDD_OP	VDD=20V, fs=110kHz		0.75		mA
VDD OVP Voltage	VDD_OVP			90		V
Voltage Sense Section (VS Pin)						
Maximum VS Source Current Capability	I_{VS_MAX}			2.9		mA
Output OVP Threshold	V_{VS_OVP}			3		V
Output UVP Threshold	V_{VS_UVP}			0.5		V
Adaptive Blanking time for VS Sampling[6]	t_{VS_BLK}	V_{COMP}=0.55V		0.6		us
		V_{COMP}=4V		1.2		us
Output OVP Debounce Cycle Counts[6]	N_{VS_OVP}			3		Cycle
Output UVP Blanking Time[7]	t_{VS_UVP}			120		ms
Auto-restart Cycles for UVP[7]	N_{UVP_HIC}			4		Cycle
Current Sense Section (CS Pin)						
Max CS Offset Current	I_{CS_MAX}	VDD=20V, COMP=3.6V		100		uA
Min CS Offset Current	I_{CS_MIN}	VDD=20V, COMP=0.5V at Burst Mode		28		uA
CS Off Threshold	V_{CS_TH}			0		mV
Leading Edge Blanking Time[7]	t_{LEB}			220		ns
Frequency Section						
Maximum Switching Frequency	f_{max}			110		kHz
Minimum Switching Frequency	f_{min}			25		kHz
Maximum-on Time	T_{ON_MAX}			18		us

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Maximum-off Time	T_{OFF_MAX}			80		us
Frequency Jittering Amplitude to COMP[7)]	ΔF_{JIT}			±7%		
Counting Cycles for Jittering[7)]	N_{JIT_CYC}			32		Cycle
Feedback Section (COMP Pin)						
Open Pin Voltage[7)]	V_{COMP_MAX}	Open Loop		4.0		V
Internal Pull-up Resistor[6)]	R_{COMP_UP}			20		kΩ
COMP to CS Offset Current Gain	G_{COMP_CS}	COMP > 2.8V		22.9		V/mA
		COMP < 1.0V		10.8		V/mA
Threshold Enter PFM Mode	V_{COMP_PFM}			2.8		V
Threshold Enter Burst Mode	V_{BUR_L}			0.5		V
Threshold Exit Burst Mode	V_{BUR_H}			0.6		V
GaN Section						
Drain-source On-state Resistance	R_{DS_ON}			470	600	mΩ
Rising Time[6)]	t_r			50		ns
Falling Time[6)]	t_f			30		ns
Internal Over Temperature Protection						
Thermal Shutdown Threshold[7)]	T_{OTP}			140		°C
OTP Hysteresis[7)]	T_{HYS}			30		ºC

6) Guaranteed by design.Not tested in production.

7) Derived from bench characterization. Not tested in production

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PIN DESCRIPTION

Part No. HSOP-7	Name	Description
1	HV	High voltage input pin. This pin provides a source current to charge VDD. This pin also sense input voltage for brown-in and brown-out protection.
2	GND	The ground of the IC.
3	VDD	Bias power input to the controller. A hold-up capacitor to GND is required.
4	COMP	Feedback input pin for Flyback QR controller. Connect to an opto-coupler directly.
5	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP and UVP protection. This pin also detects the resonant valley to implement QR operation.
6	CS	Current sensing input pin. This pin sense the primary switch current for peak current control.
7	DRAIN	Drain terminal of the internal GaN.

BLOCK DIAGRAM

TBD

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FUNCTIONAL DESCRIPTION

JW15158D is an offline flyback converter with GaN intergrated, which features multi-mode quasi-resonant (QR) operation. The Quasi-Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

JW15158D has an inherent frequency jittering mechanism to improve the EMI performance under QR operation.

Startup

1.1. High Voltage Start-up at Drain Terminal

When HV is connected to rectified AC output (BUS), the internal JFET turns on and a HV current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold V_{DD_ON} (16.5V typically), the internal startup circuit is disabled. The controller is enabled and the converter starts switching. The VDD turn-off threshold (V_{DD_OFF} typically) is 7.8V.

1.2 Soft-start

In the absence of a detected fault, the controller begins to work normally along with soft start. The internal soft-start time is within 4 ms with the feedback signal V_{COMP} rising gradually from the minimum level to the maximum level. Every restart up is followed by a soft start.

Normal Operation

After the controller start-up, it enters normal operation. JW15158D realizes the output adjustment based on the feedback signal transmitting to the primary-side controller by the opto-coupler.

JW15158D is a multi-mode QR converter with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to 110kHz. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When the load is further reduced, switching frequency is fixed at 25kHz along with primary peak current varying from 65% to 25% of its maximum. When the system is at very light load condition, the control mode of JW15158D changes to burst mode. When the voltage of COMP pin drops below V_{BUR_L} (0.5V), the drive stops. The drive will resume when the voltage of COMP pin rises back to V_{BUR_H} (0.6V). Otherwise the GaN remains at off state to minimize the switching loss and reduce the standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, V_{COMP}.

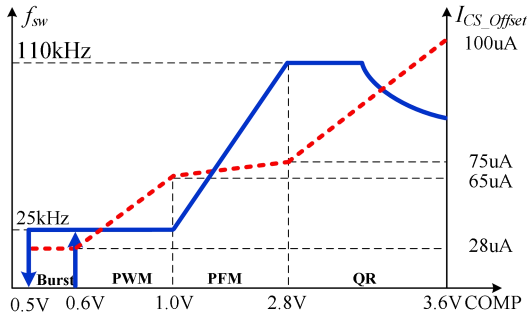

Fig. 1 Frequency & Ipk Modulation

Other Functions and Features

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3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JW15158D. The frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can't turn off the internal GaN during the blanking time. The normal LEB time is around 220ns. Fig.2 shows the leading edge blanking time.

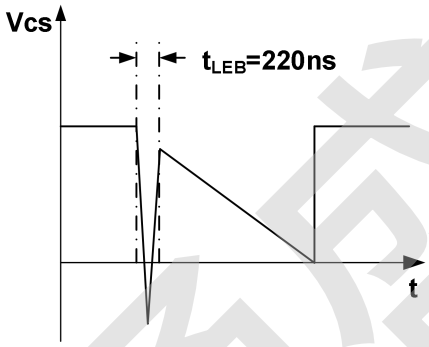

Fig. 2 LEB Blanking

3.3 CCM Preventing

For JW15158D, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after 80us to make sure the system operates in DCM.

3.4 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be set to vary with Ipk. Ensure that the secondary side conduction time is greater than the VS Blanking Time.

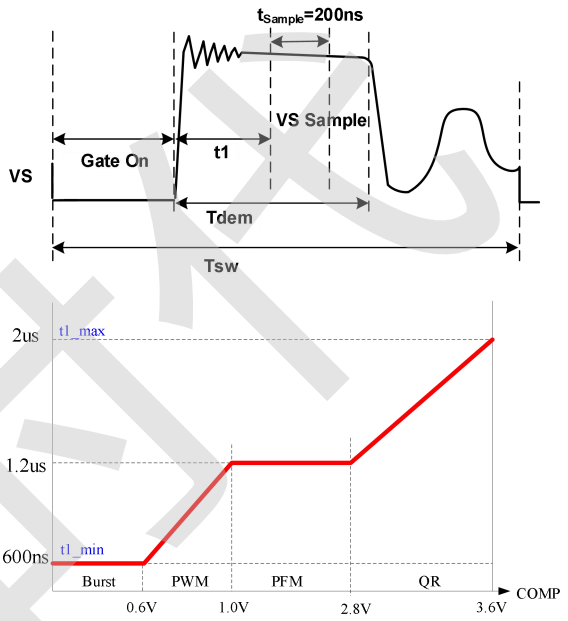

Fig. 3 VS Blanking Time

Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above 2.0V, a CS pin open fault triggered.

4.2 Input Brown in / Brown out

JW15158D senses HV voltage to realize brown in/out function. When HV voltage is higher than V_{BR_IN} (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit V_{DD_OFF}. When VDD reaches V_{DD_ON} again, the controller starts switching. And the controller is disabled when HV voltage is lower than V_{BR_OUT}

(98V typically) for brown-out blanking time (70ms typically). The blanking time is set long enough to ignore a two cycle drop out. The timer starts counting once HV voltage drops below V_{BR_OUT}.

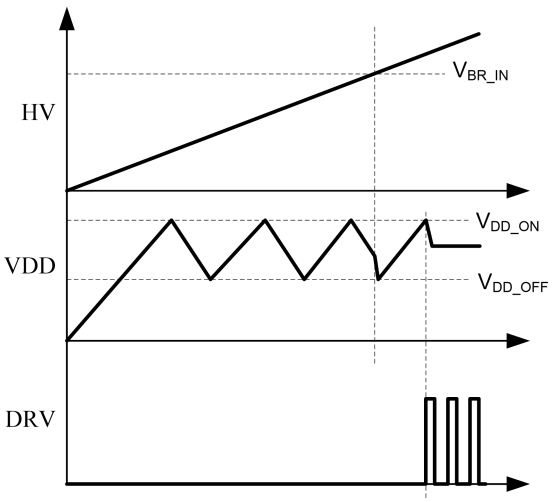

Fig. 4 Brown-In at HV pin

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds VS_OVP (3V typically) for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

4.4 VS UVP

If the voltage sample on VS pin continues below the under-voltage protection threshold (0.25V) more than 120ms, a VS_UVP fault is asserted. When a VS_UVP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.5 VDD OVP

If the voltage on VDD pin continues exceeds the over-voltage protection threshold (90V typically) more than 100us, a VDD OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.6 Internal OTP

The internal over temperature protection threshold is 140°C. If the junction temperature of the device reaches this threshold, the device shuts down. When the junction temperature falls below 110°C, the device initiates the UVLO reset and re-starts fault cycle.

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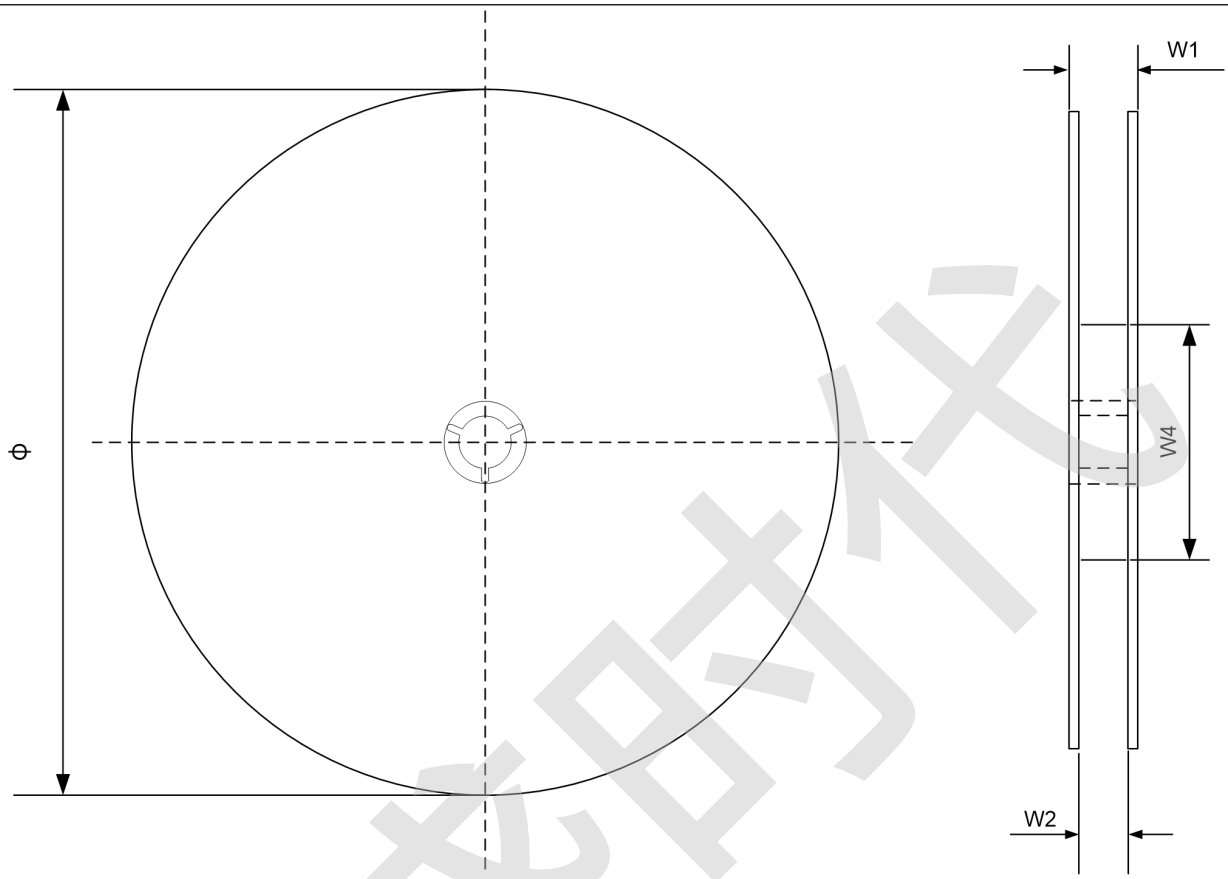
TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
HSOP-7	330±2	17.6±2	12.4±2	100±2

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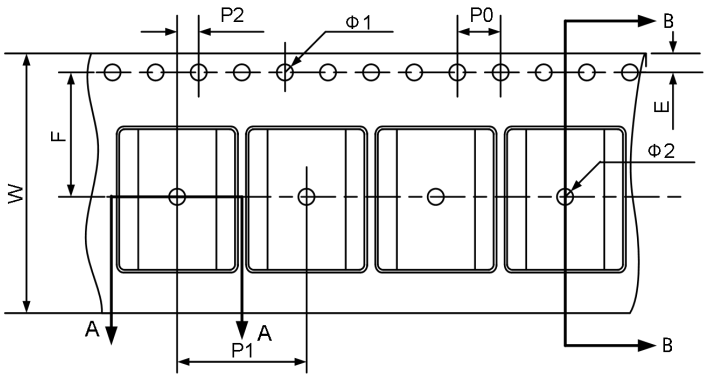
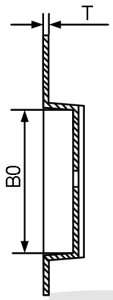
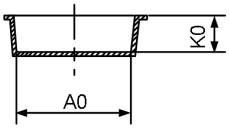
Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
HSOP-7	4.0±0.10	2.0±0.05	8.0±0.10	6.40±0.10	6.60±0.10	12±0.30	0.25±0.10	1.7±0.10	1.55±0.10	1.55±0.10	1.75±0.10	5.50±0.10

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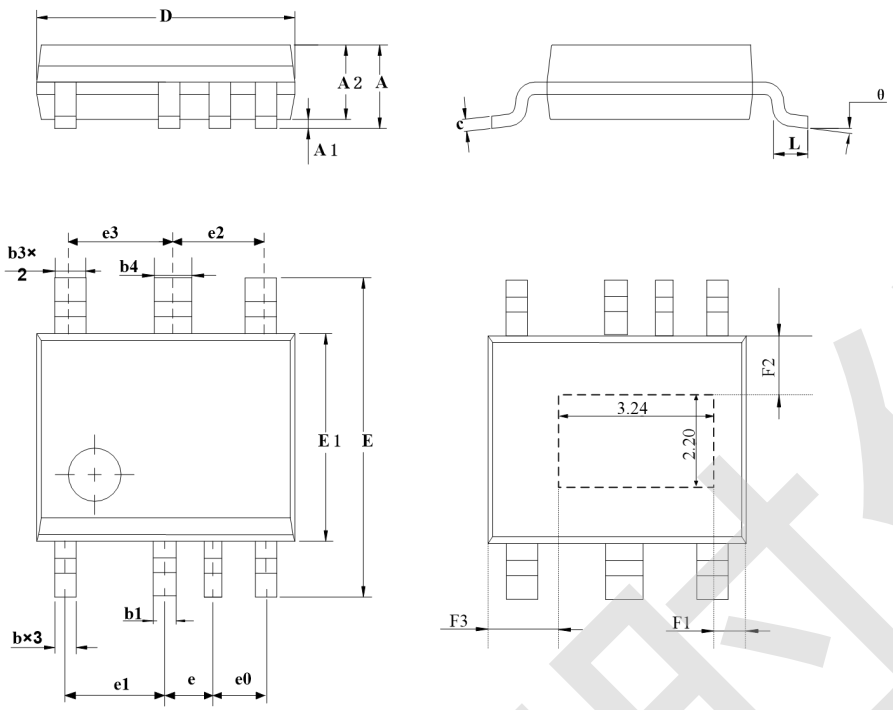
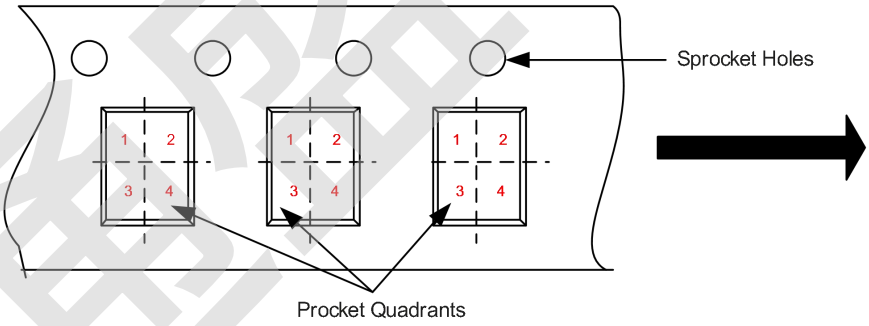
PACKAGE OUTLINE

HSOP-7 Unit: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	1.25	—	1.45
A1		0.20REF	
A2	1.05	1.15	1.25
c	0.15	—	0.22
D	6.00	6.20	6.40
E	5.90	6.00	6.10
E1	3.70	3.90	4.10
e	1.28	1.33	1.38
e0	1.22	1.27	1.32
e1	2.46	2.51	2.56
e2	2.18	2.23	2.28
e3	2.68	2.73	2.78
b	0.35	0.40	0.45
b1	0.46	0.51	0.56
b3	0.50	0.55	0.60
b4	0.75	0.80	0.85
L	0.40	—	0.80
F1	0.61	0.66	0.71
F2	0.80	0.85	0.90
F3	2.25	2.30	2.35
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
HSOP-7	1

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