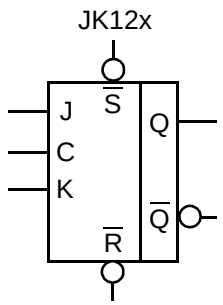
Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.1	1.0
C	1.1	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	2.2	1.1	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	13.0	TBD	29.9
JK122	15.0	TBD	37.0
JK124	17.0	TBD	42.7

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AMI5HG 0.5 micron CMOS Gate Array

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK126	19.0	TBD	49.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	0.78 0.73	0.88 0.89	1.01 1.05	1.18 1.23	1.31 1.36
	From: C To: QN	t_{PLH} t_{PHL}	1.05 1.00	1.16 1.11	1.27 1.24	1.41 1.39	1.51 1.49
	From: RN To: Q	t_{PHL}	0.90	1.06	1.22	1.40	1.52
	From: RN To: QN	t_{PLH}	1.20	1.30	1.42	1.55	1.65
	From: SN To: Q	t_{PLH}	0.88	0.99	1.12	1.29	1.41
	From: SN To: QN	t_{PHL}	0.32	0.44	0.56	0.71	0.84
JK122	Number of Equivalent Loads		1	8	15	22	30 (max)
	From: C To: Q	t_{PLH} t_{PHL}	1.22 1.08	1.33 1.23	1.41 1.34	1.49 1.43	1.57 1.53
	From: C To: QN	t_{PLH} t_{PHL}	0.72 0.83	0.82 0.95	0.92 1.06	1.02 1.16	1.13 1.27
	From: RN To: Q	t_{PHL}	0.76	0.92	1.03	1.13	1.24
	From: RN To: QN	t_{PLH}	1.06	1.17	1.26	1.35	1.44
	From: SN To: Q	t_{PLH}	0.49	0.61	0.72	0.82	0.93
	From: SN To: QN	t_{PHL}	0.74	0.88	0.99	1.08	1.21

	Number of Equivalent Loads		1	14	28	42	56 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	1.27 1.19	1.40 1.34	1.51 1.45	1.60 1.55	1.68 1.64
	From: C To: QN	t_{PLH} t_{PHL}	0.79 0.92	0.91 1.11	1.01 1.22	1.10 1.31	1.19 1.38
	From: RN To: Q	t_{PHL}	0.85	1.02	1.14	1.24	1.32
	From: RN To: QN	t_{PLH}	1.14	1.27	1.36	1.43	1.53
	From: SN To: Q	t_{PLH}	0.56	0.67	0.78	0.88	0.97
	From: SN To: QN	t_{PHL}	0.84	0.99	1.08	1.17	1.28
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	1.34 1.26	1.47 1.42	1.57 1.54	1.65 1.64	1.72 1.74
	From: C To: QN	t_{PLH} t_{PHL}	0.90 1.00	0.98 1.15	1.08 1.30	1.18 1.38	1.29 1.46
	From: RN To: Q	t_{PHL}	0.94	1.09	1.21	1.31	1.43
	From: RN To: QN	t_{PLH}	1.23	1.37	1.45	1.50	1.59
	From: SN To: Q	t_{PLH}	0.62	0.75	0.84	0.93	1.03
	From: SN To: QN	t_{PHL}	0.93	1.06	1.19	1.29	1.39

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

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Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	0.89	0.79	0.79	0.79
Min C Width	Low	t_w	0.80	0.83	0.83	0.83
Min RN Width	Low	t_w	1.06	0.64	0.64	0.64
Min SN Width	Low	t_w	0.64	0.44	0.44	0.44
Min J Setup		t_{su}	0.80	0.83	0.83	0.83
Min J Hold		t_h	0.17	0.17	0.17	0.17
Min K Setup		t_{su}	0.73	0.73	0.73	0.73
Min K Hold		t_h	0.17	0.17	0.17	0.17
Min RN Setup		t_{su}	0.36	0.40	0.40	0.40
Min RN Hold		t_h	0.33	0.33	0.33	0.33
Min SN Setup		t_{su}	0.22	0.22	0.22	0.22
Min SN Hold		t_h	0.49	0.48	0.48	0.48

Logic Schematic