IRHLUB7970Z4 (JANSR2N7626UB)

PD-94764P

Radiation Hardened Logic Level Power MOSFET
Surface Mount (UB)
-60V, -0.53A, P-channel, R7 Technology

Features

- 5V CMOS and TTL compatible
- Single event effect (SEE) hardened
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Light weight
- Surface mount
- ESD rating: Class 0B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** -60V
- **I_D :** -0.53A
- **$R_{DS(on), max}$:** 1.4Ω
- **$Q_{G, max}$:** 3.6nC
- **REF:** MIL-PRF-19500/745

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

UB

UBN
(Isolated Metal Lid)

UBC
(Shielded Ceramic Lid)

UBCN
(Isolated Ceramic Lid)

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLUB7970Z4	UB	COTS	100 krad(Si)
JANSR2N7626UB	UB	JANS	100 krad(Si)
IRHLUB7930Z4	UB	COTS	300 krad(Si)
JANSF2N7626UB	UB	JANS	300 krad(Si)
IRHLUBN7970Z4	UBN	COTS	100 krad(Si)
JANSR2N7626UBN	UBN	JANS	100 krad(Si)
IRHLUBN7930Z4	UBN	COTS	300 krad(Si)
JANSF2N7626UBN	UBN	JANS	300 krad(Si)
IRHLUBC7970Z4	UBC	COTS	100 krad(Si)
JANSR2N7626UBC	UBC	JANS	100 krad(Si)
IRHLUBC7930Z4	UBC	COTS	300 krad(Si)
JANSF2N7626UBC	UBC	JANS	300 krad(Si)
IRHLUBCN7970Z4	UBCN	COTS	100 krad(Si)
JANSR2N7626UBCN	UBCN	JANS	100 krad(Si)
IRHLUBCN7930Z4	UBCN	COTS	300 krad(Si)
JANSF2N7626UBCN	UBCN	JANS	300 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = -4.5V, T_C = 25°C	Continuous Drain Current	-0.53	A
I_{D2} @ V_{GS} = -4.5V, T_C = 100°C	Continuous Drain Current	-0.33	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	-2.12	A
P_D @ T_C = 25°C	Maximum Power Dissipation	0.57	W
	Linear Derating Factor	0.0045	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy [2]	33.5	mJ
I_{AR}	Avalanche Current [1]	-0.53	A
E_{AR}	Repetitive Avalanche Energy [1]	0.06	mJ
dv/dt	Peak Diode Reverse Recovery [3]	-4.4	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	°C
	Weight	43 (Typical)	mg

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] V_{DD} = -25V, starting T_J = 25°C, L = 238mH, Peak I_L = -0.53A, V_{GS} = -10V
[3] $I_{SD} \leq$ -0.53A, di/dt $\leq$ -100A/µs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.055	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.4	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A [1]
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.1	—	mV/°C	
Gfs	Forward Transconductance	0.8	—	—	S	V_{DS} = -10V, I_{D2} = -0.33A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-10		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_G	Total Gate Charge	—	—	3.6	nC	I_{D1} = -0.53A V_{DS} = -30V V_{GS} = -4.5V
Q_{GS}	Gate-to-Source Charge	—	—	1.5		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	22	ns	I_{D1} = -0.53A ** V_{DD} = -30V R_G = 24Ω V_{GS} = -5.0V
t_r	Rise Time	—	—	22		
$t_{d(off)}$	Turn-Off Delay Time	—	—	27		
t_f	Fall Time	—	—	27		
$L_s + L_D$	Total Inductance	—	8.4	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	167	—	pF	V_{GS} = 0V V_{DS} = -25V ƒ = 100KHz
C_{oss}	Output Capacitance	—	43	—		
C_{rss}	Reverse Transfer Capacitance	—	10	—		
R_G	Gate Resistance	—	56	—	Ω	ƒ = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.53	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-2.12	A	
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J = 25°C, I_S = -0.53A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	50	ns	T_J = 25°C, I_F = -0.53A, V_{DD} ≤ -25V di/dt = -100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	—	25	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient	—	—	220	°C/W
$R_{\theta JL}$	Junction-to-Lead	—	—	40	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V_{GS} = 0V, I_D = -250µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-39) [2]	—	1.36	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (UB) [2]	—	1.40	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A
V_{SD}	Diode Forward Voltage	—	-5.0	V	V_{GS} = 0V, I_F = -0.53A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = -10V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = -48V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers: IRHLUB7970Z4 (JANSR2N7626UB), IRHLUB7930Z4 (JANSF2N7626UB), IRHLUBN7970Z4 (JANSR2N7626UBN), IRHLUBN7930Z4 (JANSF2N7626UBN), IRHLUBC7970Z4 (JANSR2N7626UBC), IRHLUBC7930Z4 (JANSF2N7626UBC), IRHLUBCN7970Z4 (JANSR2N7626UBCN), IRHLUBCN7930Z4 (JANSF2N7626UBCN)

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)					
			V_{GS} = 0V	V_{GS} = 2V	V_{GS} = 4V	V_{GS} = 5V	V_{GS} = 6V	V_{GS} = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7. 5%	33 ± 7.5%	-60	-60	-60	-60	-60	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	—	—

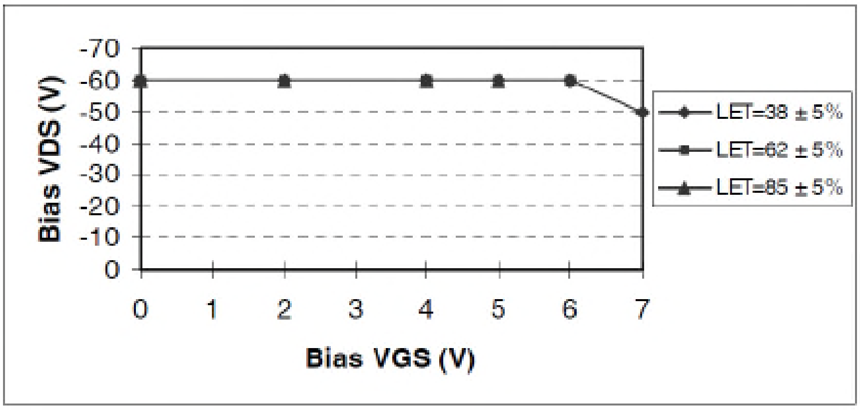


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

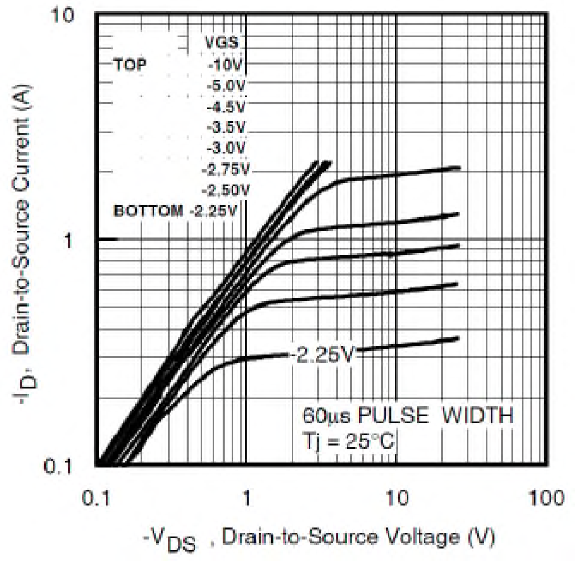


Figure 2 Typical Output Characteristics

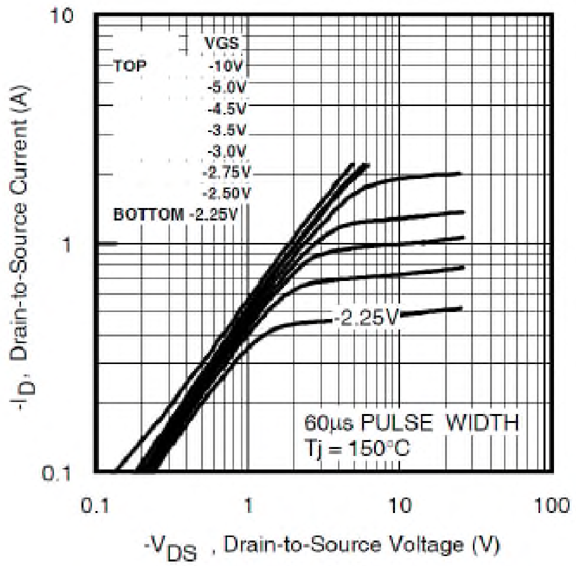


Figure 3 Typical Output Characteristics

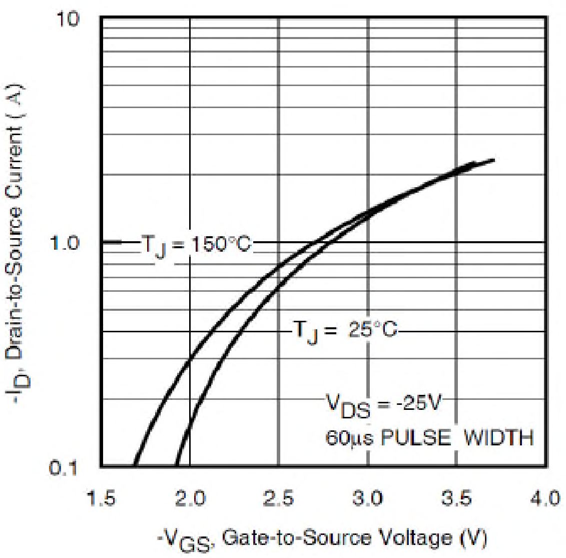


Figure 4 Typical Transfer Characteristics

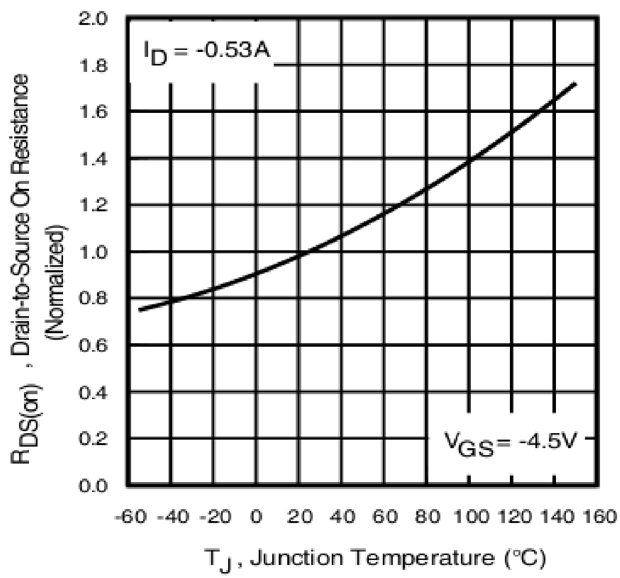


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

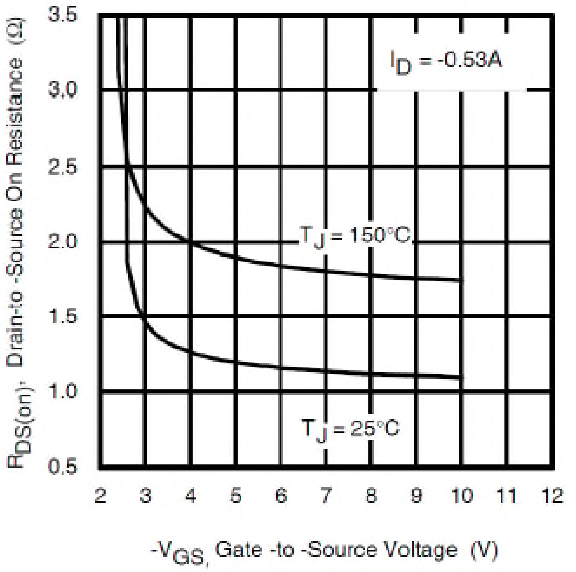


Figure 6 **Typical On-Resistance Vs. Gate Voltage**

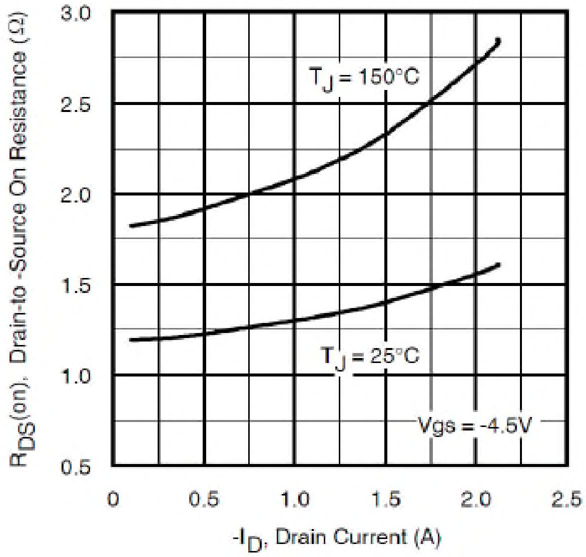


Figure 7 **Typical On-Resistance Vs. Drain Current**

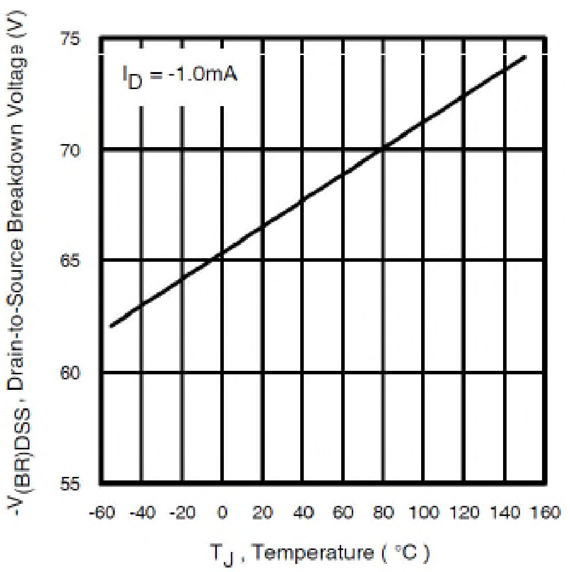


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

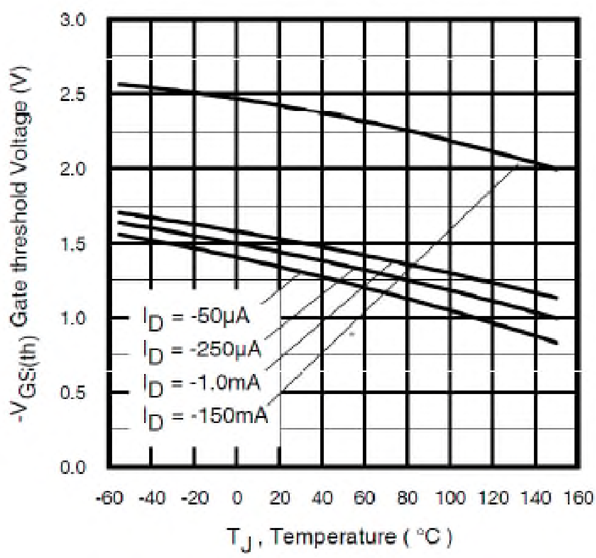


Figure 9 **Typical Threshold Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

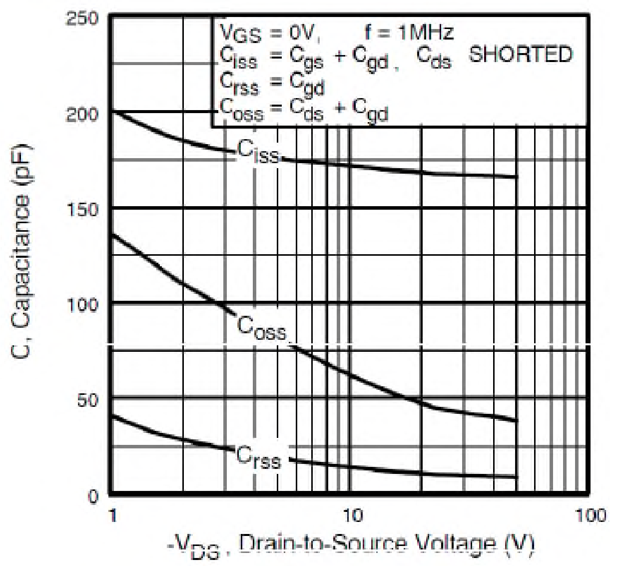


Figure 10 **Typical Capacitance Vs. Drain-to-Source Voltage**

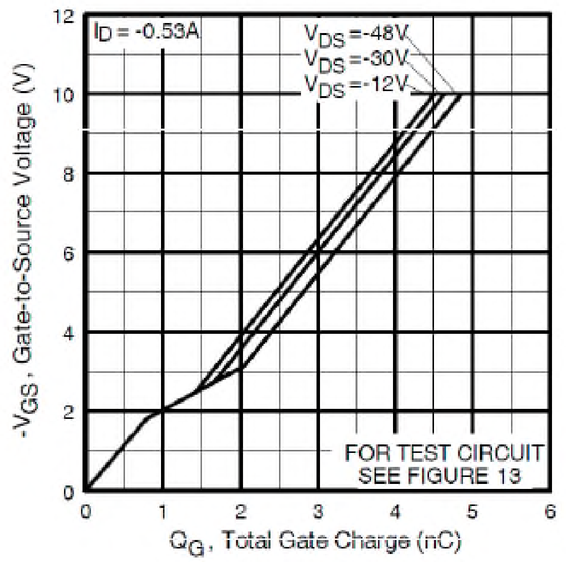


Figure 11 **Gate-to-Source Voltage Vs. Typical Gate Charge**

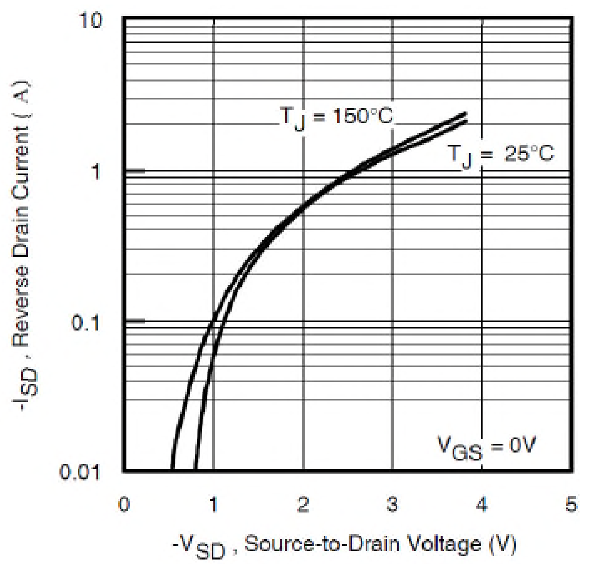


Figure 12 **Typical Source-Drain Current Vs. Diode Forward Voltage**

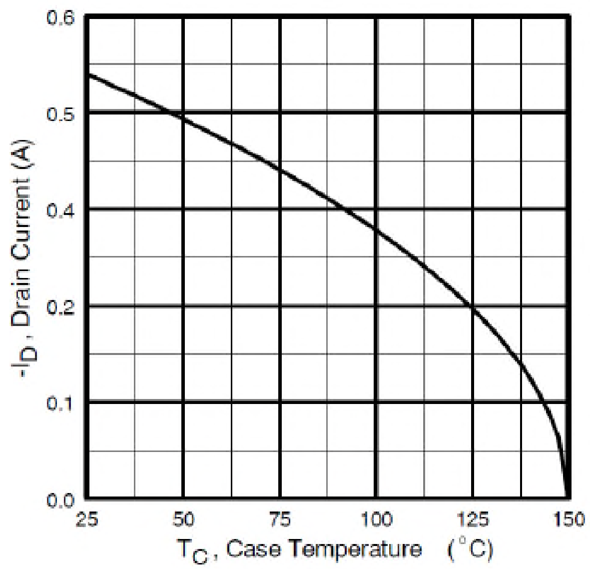


Figure 13 **Maximum Drain Current Vs. Case Temperature**

Electrical Characteristics Curves (Pre-irradiation)

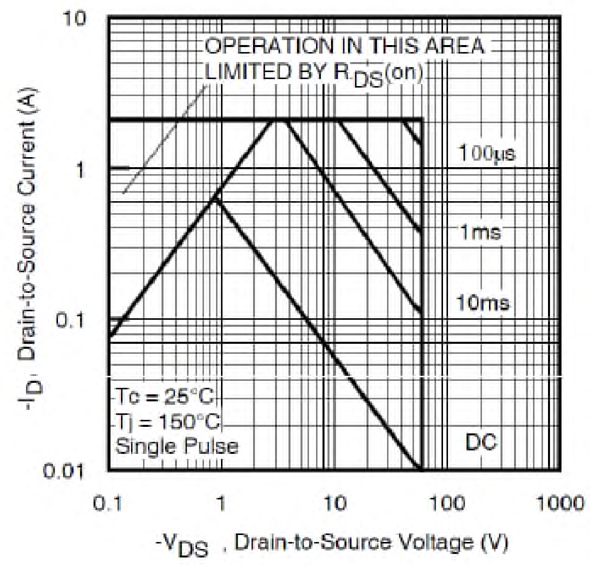


Figure 14 **Maximum Safe Operating Area**

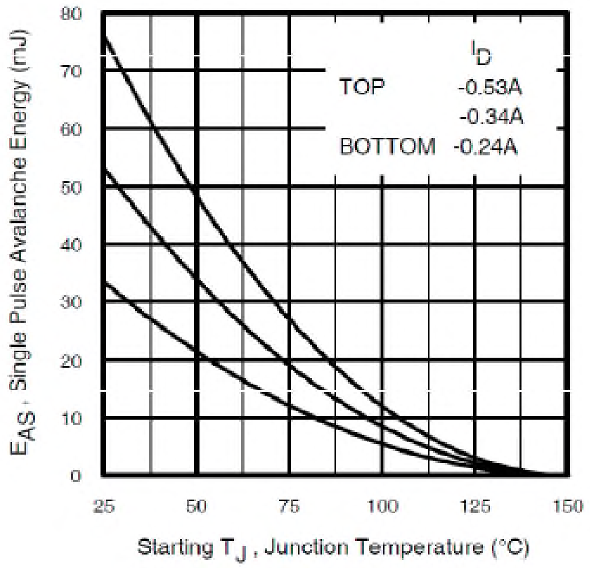


Figure 15 **Maximum Avalanche Energy Vs. Junction Temperature**

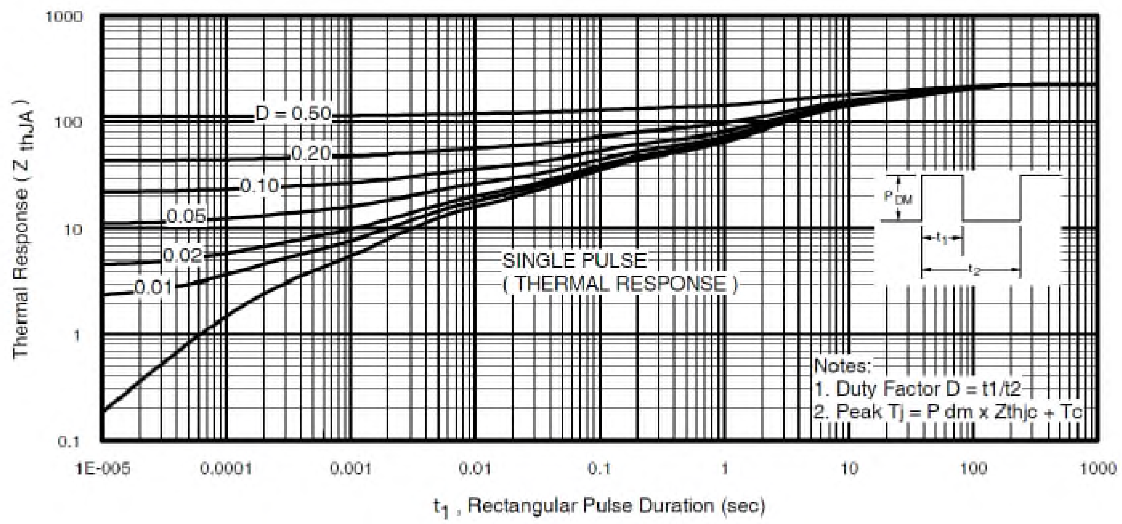


Figure 16 **Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**

4 Test Circuits (Pre-irradiation)

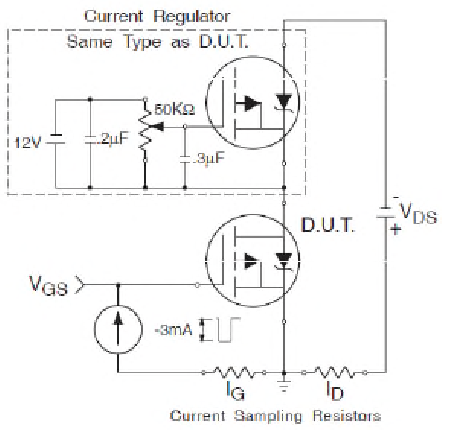


Figure 17 Gate Charge Test Circuit

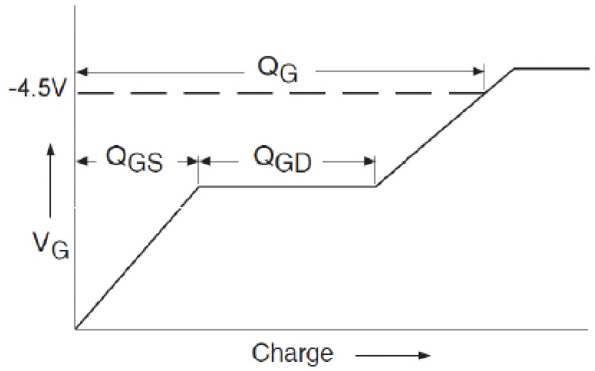


Figure 18 Gate Charge Waveform

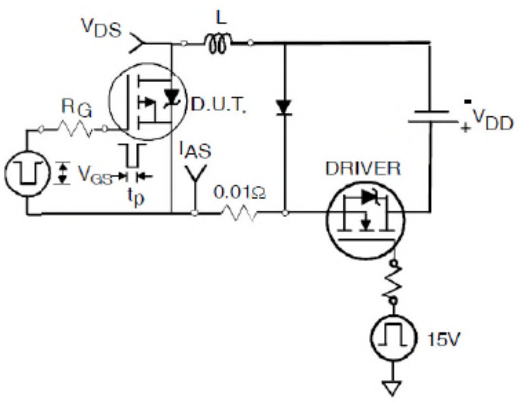


Figure 19 Unclamped Inductive Test Circuit

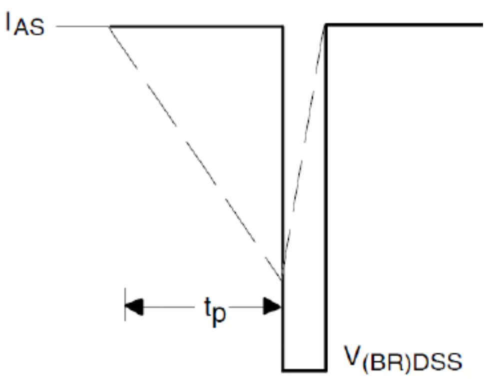


Figure 20 Unclamped Inductive Waveform

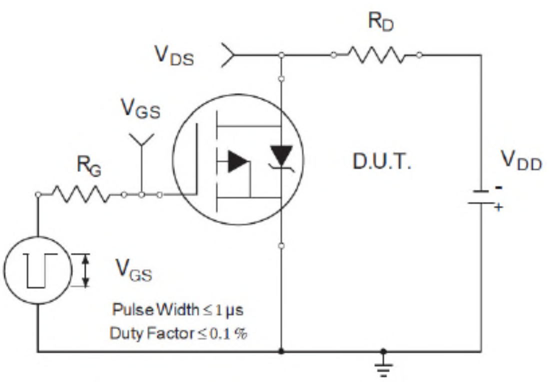


Figure 21 Switching Time Test Circuit

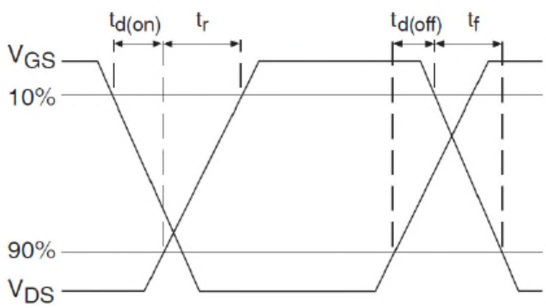
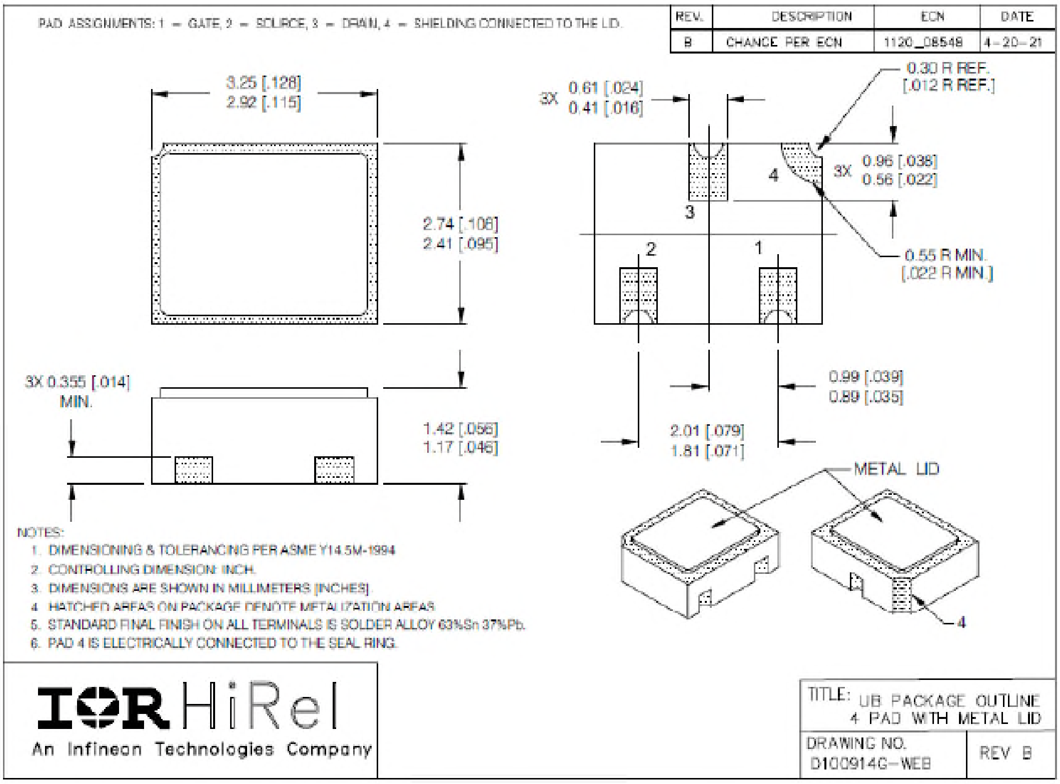


Figure 22 Switching Time Waveforms

5 Package Outline

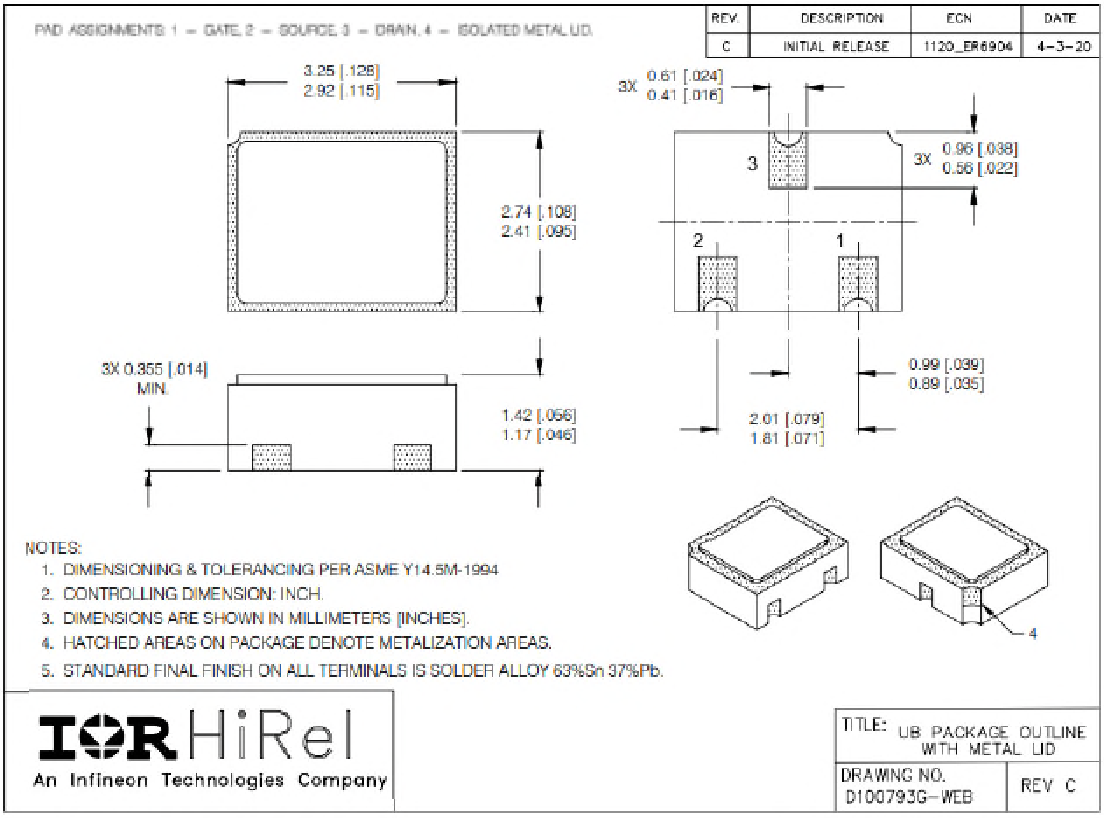
Note: For the most updated package outline, please see the website: UB

Case Outline and Dimensions - UB (Shielded Metal Lid Connected to 4th Pad)



Note: For the most updated package outline, please see the website: UBN

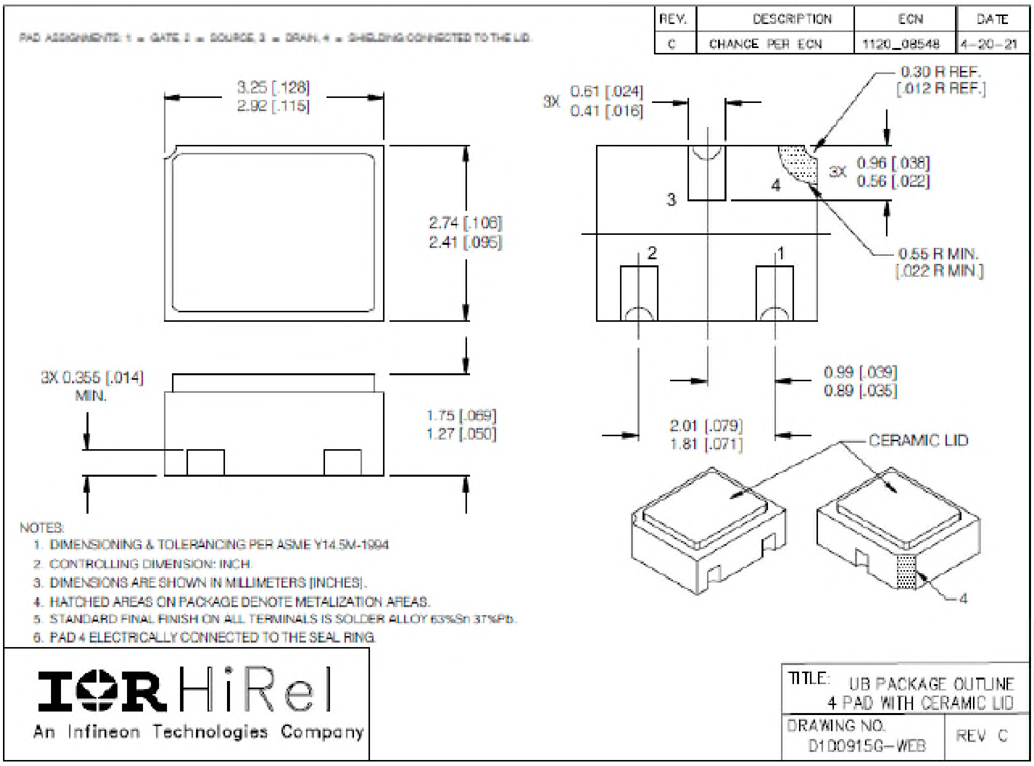
Case Outline and Dimensions - UBN (Isolated Metal Lid, No 4th Pad)



Package Outline

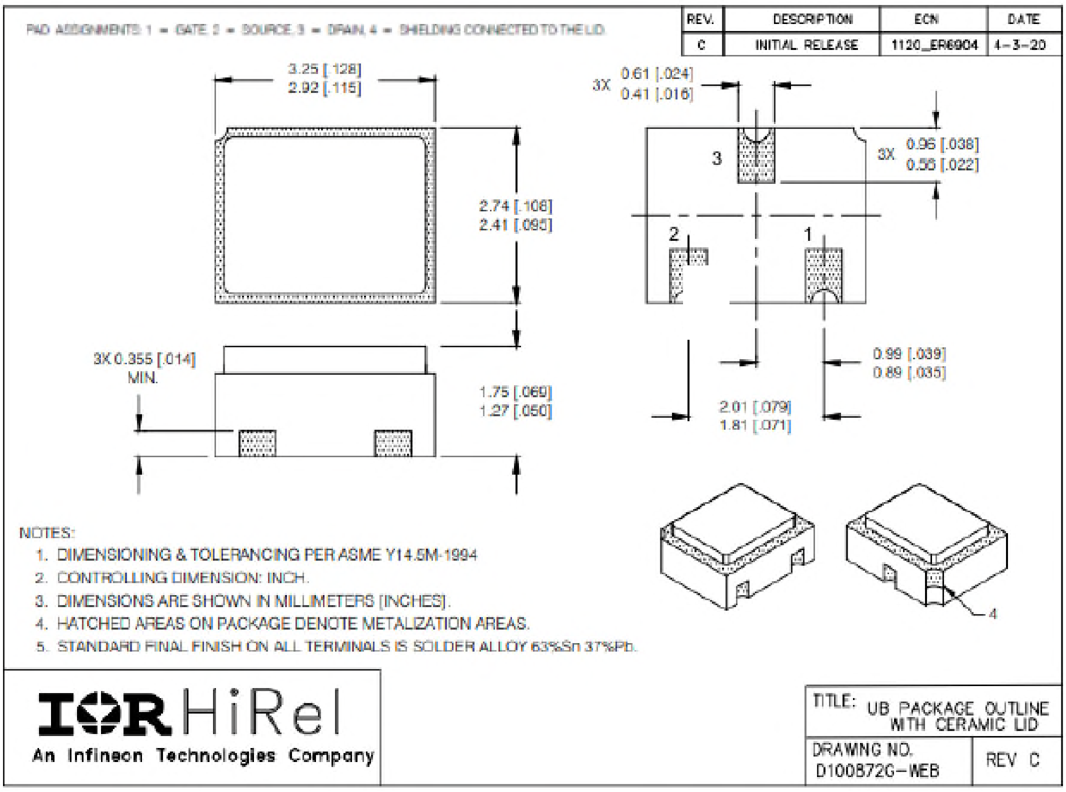
Note: For the most updated package outline, please see the website: UBC

Case Outline and Dimensions - UBC (Shielded Ceramic Lid Connected to 4th Pad)



Note: For the most updated package outline, please see the website: UBCN

Case Outline and Dimensions - UBCN (Isolated Ceramic Lid, No 4th Pad)



Revision history

Document version	Date of release	Description of changes
	11/11/2003	Datasheet (PD-94764)
Rev A	04/02/2004	Updated swtchtime test condition
Rev B	07/21/2004	Updated based on ECN-11866
Rev C	09/03/2004	Updated based on ECN-12213
Rev D	06/17/2005	Updated based on ECN-13068
Rev E	09/09/2005	Updated based on ECN-13390
Rev F	01/31/2006	Updated Feature-page1
Rev G	01/19/2007	Updated based on ECN-14447
Rev H	06/12/2007	Added 2N7626UB-page1
Rev I	05/14/2009	Updated based on ECN-16472
Rev J	08/25/2009	Updated typo Pch from N ch
Rev K	01/29/2010	Updated fig 1,2,3,5,6
Rev L	09/16/2010	Updated based on ECN-17302
Rev M	08/13/2019	Updated based on ECN-1120_07306
Rev N	01/13/2020	Updated based on ECN-1120_07601
Rev O	04/27/2021	Updated based on ECN-1120_08548
Rev P	08/12/2022	Updated based on ECN-1120_09174

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Edition 2022-08-12

Published by

International Rectifier HiRel Products, Inc.

An Infineon Technologies company

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