

4-Bit Micro-Controller With EEPROM, 1K Word

Features

- Very low current dissipation.
- Wide operating voltage range.
- Supports both Ag and Li batteries.
- Powerful instruction set.
- 4-level subroutine nesting (including interrupt).
- 4 event-driven interrupts, 2 external and 2 internal.
- ROM size: 1024x15 bits.
- RAM size: 64x4 bits.
- Input ports: 2 ports/ 8 pins (S and M).
- Output port: 1 port/ 4 pins (P).
- Pseudo serial output port (P).
- Input/Output ports: 2 ports/ 8 pins (I/OA and I/OB).
- Control outputs: ALARM, LIGHT.
- LCD driver outputs (can drive up to 75 LCD segments).
- PROM option to select 4 LCD drive modes: static, duplex (1/2 duty 1/2 bias, 1/3 duty 1/2 bias or 1/3 duty 1/3 bias).
- PROM option permits LCD driver output pins to be used for DC output ports; up to 25 pins are available.
- Segment PLA circuit permits any layout on LCD panel.
- Built-in clock generator (crystal or RC).
- Built-in voltage doubler, halver, tripler.
- Endurance: More than 100 write cycles/word.
- Security bit for read/write protection.

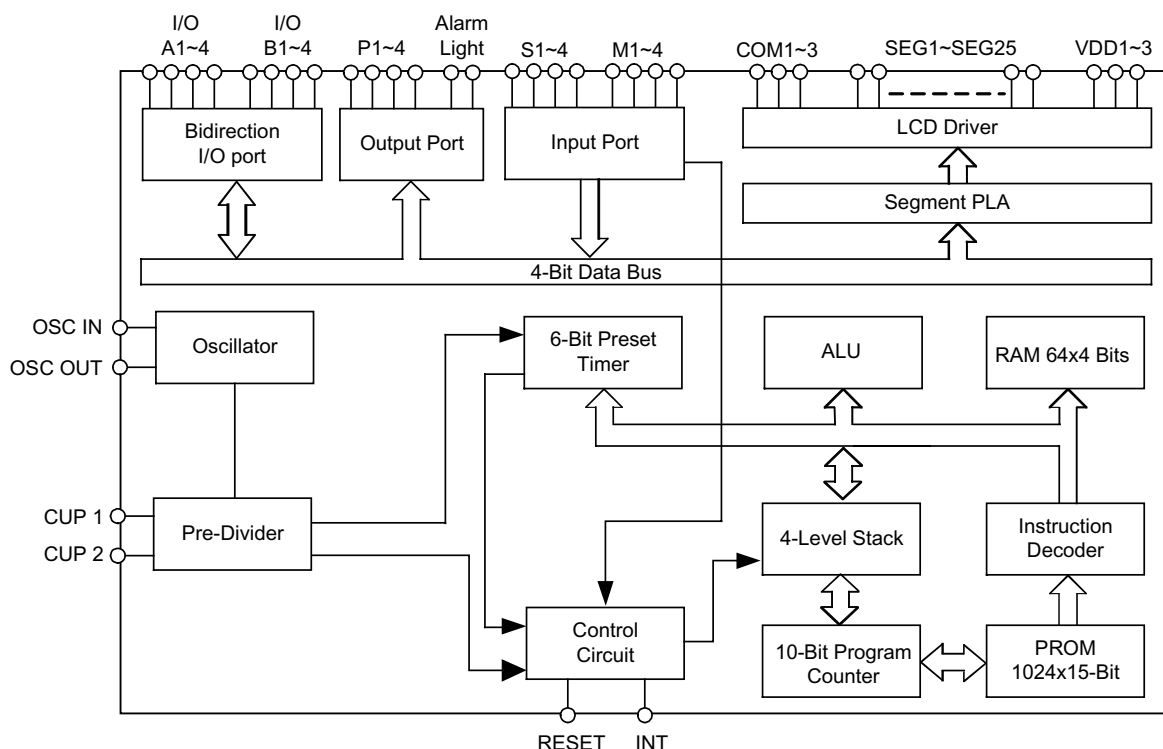
General Description

The JA54130 is an EEPROM-equipped high-performance 4-bit microcomputer. It contains not only all functions compatible with JA54100, but also an EEPROM, providing customers such conveniences as on-board verification,

customized code, small quantity sample production, etc.

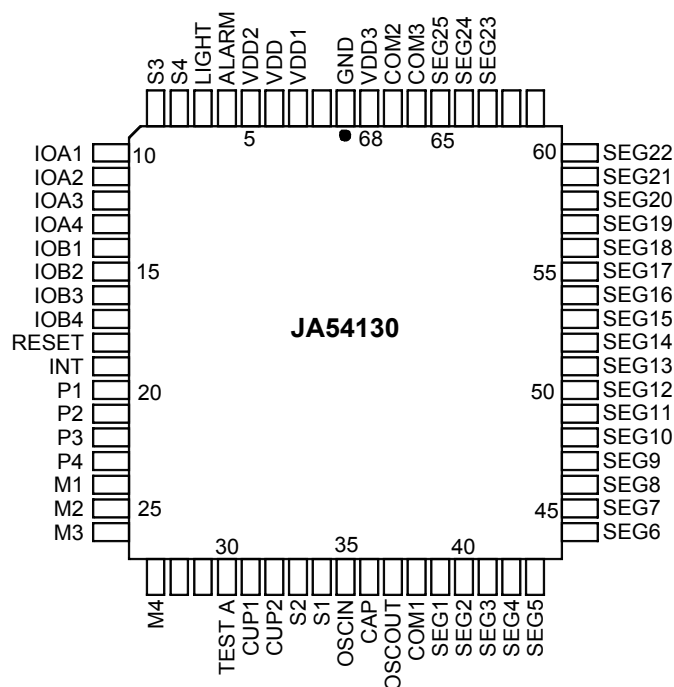
This chip especially provides a security bit to protect the customer's code.

Block Diagram



Package Information

Package type 68Pin PLCC



Pin/Pad Assignment

Unit: μm

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	VSS	18	RESET	35	OSCIN	52	SEG14
2	-----	19	INT	36	CAP	53	SEG15
3	VDD1	20	P1	37	OSCOUT	54	SEG16
4	VDD	21	P2	38	COM1	55	SEG17
5	VDD2	22	P3	39	SEG1	56	SEG18
6	ALARM	23	P4	40	SEG2	57	SEG19
7	LIGHT	24	M1	41	SEG3	58	SEG20
8	S4	25	M2	42	SEG4	59	SEG21
9	S3	26	M3	43	SEG5	60	SEG22
10	IOA1	27	M4	44	SEG6	61	-----
11	IOA2	28	-----	45	SEG7	62	-----
12	IOA3	29	-----	46	SEG8	63	SEG23
13	IOA4	30	TESTA	47	SEG9	64	SEG24
14	IOB1	31	CUP1	48	SEG10	65	SEG25
15	IOB2	32	CUP2	49	SEG11	66	COM3
16	IOB3	33	S2	50	SEG12	67	COM2
17	IOB4	34	S1	51	SEG13	68	VDD3

Pin Name Description

Name	Type	Description
OSCIN	I	Typical crystal(32.768KHz) is connected across OSCIN/OSCOUT for oscillation; R/C oscillation mode is also available.
OSCOUT	O	
S1~4	I	Input ports with chattering eliminator option for CK10 (32ms), CK8 (8ms) & CK6 (2ms).
M1~4	I	
P1~4	O	Output ports.
IOA1~4	I/O	Input/Output ports.
IOB1~4	I/O	Input/Output ports.
INT	I	External interrupt request control input pin.
RESET	I	System reset pin.
LIGHT	O	Output only for outputting the signal to drive the transistor for light.
ALARM	O	Output only for outputting the 4kHz/2kHz/1kHz modulation signal. Also can be used to output the non-modulation signal.
VDD		(+)Power supply pin.
VDD1		* For Ag version, apply (+) side to VDD & VDD1 together.
VDD2		For other than Ag version, apply (+) side to VDD & VDD2 together.
VDD3		Power supply pin for LCD driver power supply.
VSS		(--)Power supply pin.
CUP1~2	O	Pins for connecting the voltage step-up (step-down) capacitor.
COM1~3	O	Output pins for LCD panel common plate.
SEG1~25	O	Output pins for LCD panel segments.

Absolute Maximum Rating

Ta = 0 to 70°C

Name	Symbol	Rating	Unit
Maximum Supply Voltage	$V_{SS1/2}$	-0.3 ~ +5.5	V
	V_{SS3}	-0.3 ~ +8.5	V
Maximum Input Voltage	V_{IN1}	-0.3 to $V_{DD}+0.3$	V
Maximum Output Voltage	V_{OUT1}	-0.3 to $V_{DD1}+0.3$	V
	V_{OUT2}	-0.3 to $V_{DD2}+0.3$	V
	V_{OUT3}	-0.3 to $V_{DD3}+0.3$	V
Maximum Operating Temperature	t_{OPG}	0 to +70	°C
Maximum Storage Temperature	t_{STG}	-25 to +125	°C

Allowable operating conditions

Ta = 0 to 70°C

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD1}	External Voltage Mode	2.0	5.5	V
	V_{DD2}		4.0	5.5	V
	V_{DD3}		4.0	8.25	V
Supply Voltage	V_{DD1}	Ag & Li Battery Mode	1.3	5.5	V
	V_{DD2}		2.6	5.5	V
	V_{DD3}		2.6	8.25	V
Input "H" Voltage	V_{IH1}	All Input Except OSCIN	$0.7V_{DDO}$	V_{DDO}	V
Input "L" Voltage	V_{IL1}		0	$0.3V_{DDO}$	V
Input "H" Voltage	V_{IH2}	OSCIN at Ext. RC Mode	$0.8V_{DDO}$	V_{DDO}	V
Input "L" Voltage	V_{IL2}		0	$0.2V_{DDO}$	V
Operating Freq.	f_{OPG1}	Ag Battery Mode	32	32	kHz
	f_{OPG2}	Li Battery Mode	32	100	kHz
	f_{OPG3}	External Voltage Mode	32	3580	kHz
	f_{OPG4}	External RC Mode	32	5000	kHz

Electrical Characteristics

Ta=0 to 70°C

Input resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
"L"-Level Hold t_R	R_{IIH1}	$V_I=0.2V_{DD1}, \#1$	10	40	100	$k\Omega$
	R_{IIH2}	$V_I=0.2V_{DD2}, \#2$	10	40	100	$k\Omega$
	R_{IIH3}	$V_I=0.3V_{DD2}, \#3$	5	20	50	$k\Omega$
M/S Pull-Down t_R	R_{MSD1}	$V_I=V_{DD1}, \#1$	200	500	1000	$k\Omega$
	R_{MSD2}	$V_I=V_{DD2}, \#2$	200	500	1000	$k\Omega$
	R_{MSD3}	$V_I=V_{DD2}, \#3$	100	250	500	$k\Omega$
INT Pull-Up t_R	R_{INTU1}	$V_I=V_{SS}, \#1$	200	500	1000	$k\Omega$
	R_{INTU2}	$V_I=V_{SS}, \#2$	200	500	1000	$k\Omega$
	R_{INTU3}	$V_I=V_{SS}, \#3$	100	250	500	$k\Omega$
INT Pull-Down t_R	R_{INTD1}	$V_I=V_{DD1}, \#1$	200	500	1000	$k\Omega$
	R_{INTD2}	$V_I=V_{DD2}, \#2$	200	500	1000	$k\Omega$
	R_{INTD3}	$V_I=V_{DD2}, \#3$	100	250	500	$k\Omega$
RES Pull-Down t_R	R_{RES1}	$V_I=V_{DD} \text{ or } V_{SS1}, \#1$	5	20	50	$k\Omega$
	R_{RES2}	$V_I=V_{DD} \text{ or } V_{SS2}, \#2$	5	20	50	$k\Omega$
	R_{RES3}	$V_I=V_{DD} \text{ or } V_{SS2}, \#3$	5	20	50	$k\Omega$

Note: #1: $V_{DD1}=1.3V$ (Ag), #2: $V_{DD2}=2.6V$ (Li), #3: $V_{DD2}=4.5V$ (ExtV).

DC output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output "H" Voltage	V_{OH1a}	$I_{OH}=-200\mu A, \#1$	Alarm Light	0.9	1.1		V
	V_{OH2a}	$I_{OH}=-1ma, \#2$		1.8	2.1		V
	V_{OH3a}	$I_{OH}=-3mA, \#3$		3.0	3.5		V
Output "L" Voltage	V_{OL1a}	$I_{OL}=400\mu A, \#1$	P-port IOA-n IOB-n		0.3	0.5	V
	V_{OL2a}	$I_{OL}=2mA, \#2$			0.6	1	V
	V_{OL3a}	$I_{OL}=6mA, \#3$			1.0	1.5	V
Output "H" Voltage	V_{OH1b}	$I_{OH}=-100\mu A, \#1$		0.9	1.1		V
	V_{OH2b}	$I_{OH}=-500\mu A, \#2$		1.8	2.1		V
	V_{OH3b}	$I_{OH}=-1.5mA, \#3$		3.0	3.5		V
Output "L" Voltage	V_{OL1b}	$I_{OL}=200\mu A, \#1$			0.3	0.5	V
	V_{OL2b}	$I_{OL}=1mA, \#2$			0.6	1	V
	V_{OL3b}	$I_{OL}=3mA, \#3$			1.0	1.5	V

Note: #1: $V_{DD1}=1.3V$ (Ag), #2: $V_{DD2}=2.6V$ (Li), #3: $V_{DD2}=4.5V$ (ExtV).

Segment driver output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
DC output mode							
Output "H" Voltage	V_{OH1c}	$I_{OH}=-10\mu A, \#1$	SEG-n	0.9	1.1		V
	V_{OH2c}	$I_{OH}=-50\mu A, \#2$		1.8	2.1		V
	V_{OH3c}	$I_{OH}=-200\mu A, \#3$		3.0	3.5		V
Output "L" Voltage	V_{OL1c}	$I_{OL}=20\mu A, \#1$			0.3	0.5	V
	V_{OL2c}	$I_{OL}=100\mu A, \#2$			0.6	1	V
	V_{OL3c}	$I_{OL}=400\mu A, \#3$			1.0	1.5	V
Static display mode							
Output "H" Voltage	V_{OH2d}	$I_{OH}=-1\mu A, \#1, \#2$	SEG-n	2.5			V
	V_{OH3d}	$I_{OH}=-1\mu A, \#3$		4.3			V
Output "L" Voltage	V_{OL2d}	$I_{OL}=1\mu A, \#1, \#2$				0.2	V
	V_{OL3d}	$I_{OL}=1\mu A, \#3$				0.2	V
	V_{OH2e}	$I_{OH}=-10\mu A, \#1, \#2$		2.5			V

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output "H" Voltage	V_{OH2e}	$I_{OH} = -10\mu A, \#1, \#2$		2.5			V
Output "L" Voltage	V_{OH2e}	$I_{OH} = -10\mu A, \#1, \#2$	COM-n	4.3		0.2	V
	V_{OL3e}	$I_{OL} = 10\mu A, \#3$				0.2	V
Duplex (1/2 bias, 1/2 duty) display mode							
Output "H" Voltage	V_{OH12f}	$I_{OH} = -1\mu A, \#1, \#2$	SEG-n	2.4			V
	V_{OH3f}	$I_{OH} = -1\mu A, \#3$		4.3			V
Output "L" Voltage	V_{OL12f}	$I_{OL} = 1\mu A, \#1, \#2$				0.2	V
	V_{OL3f}	$I_{OL} = 1\mu A, \#3$				0.2	V
Output "H" Voltage	V_{OH12g}	$I_{OH} = -10\mu A, \#1, \#2$	COM-n	2.4			V
	V_{OH3g}	$I_{OH} = -10\mu A, \#3$		4.3			V
Output "M" Voltage	V_{OM12g}	$I_{OI/H} = \pm 10\mu A, \#1, \#2$		1.1		1.5	V
	V_{OM3g}	$I_{OI/H} = \pm 10\mu A, \#3$		2.05		2.45	V
Output "L" Voltage	V_{OL12g}	$I_{OL} = 10\mu A, \#1$				0.2	V
	V_{OL3g}	$I_{OL} = 10\mu A, \#3$				0.2	V
1/2 bias, 1/3 duty display mode							
Output "H" Voltage	V_{OH12h}	$I_{OH} = -1\mu A, \#1, \#2$	SEG-n	2.4			V
	V_{OH3h}	$I_{OH} = -1\mu A, \#3$		4.3			V
Output "L" Voltage	V_{OL12h}	$I_{OL} = 1\mu A, \#1, \#2$				0.2	V
	V_{OL3h}	$I_{OL} = 1\mu A, \#3$				0.2	V
Output "H" Voltage	V_{OH12i}	$I_{OH} = -10\mu A, \#1, \#2$	COM-n	2.4			V
	V_{OH3i}	$I_{OH} = -10\mu A, \#3$		4.3			V
Output "M" Voltage	V_{OM12i}	$I_{OI/H} = \pm 10\mu A, \#1, \#2$		1.1		1.5	V
	V_{OM3i}	$I_{OI/H} = \pm 10\mu A, \#3$		2.05		2.45	V
Output "L" Voltage	V_{OL12i}	$I_{OL} = 10\mu A, \#1, \#2$				0.2	V
	V_{OL3i}	$I_{OL} = 10\mu A, \#3$				0.2	V
1/3 bias, 1/3 duty display mode							
Output "H" Voltage	V_{OH12j}	$I_{OH} = -1\mu A, \#1, \#2$	SEG-n	3.85			V
	V_{OH3j}	$I_{OH} = -1\mu A, \#3$		6.55			V
Output "M1" Voltage	V_{OM12j}	$I_{OI/H} = \pm 1\mu A, \#1, \#2$		2.9		2.4	V
	V_{OM13j}	$I_{OI/H} = \pm 1\mu A, \#1, \#2$		4.7		4.3	V
Output "M2" Voltage	V_{OM22j}	$I_{OI/H} = \pm 1\mu A, \#1, \#2$		1.1		1.5	V
	V_{OM23j}	$I_{OI/H} = \pm 1\mu A, \#1, \#2$		2.05		2.45	V
Output "L" Voltage	V_{OL2j}	$I_{OL} = 1\mu A, \#2$				0.2	V
	V_{OL3j}	$I_{OL} = 1\mu A, \#3$				0.2	V
Output "H" Voltage	V_{OH2k}	$I_{OH} = -10\mu A, \#2$	COM-n	3.85			V
	V_{OH3k}	$I_{OH} = -10\mu A, \#3$		6.55			V
Output "M1" Voltage	V_{OM12k}	$I_{OI/H} = \pm 10\mu A, \#1, \#2$		2.9		2.4	V
	V_{OM13k}	$I_{OI/H} = \pm 10\mu A, \#3$		4.7		4.3	V
	V_{OM22k}	$I_{OI/H} = \pm 10\mu A, \#1, \#2$		1.1		1.5	V
	V_{OM23k}	$I_{OI/H} = \pm 10\mu A, \#3$		2.05		2.45	V
	V_{OL2k}	$I_{OL} = 10\mu A, \#2$				0.2	V
	V_{OL3k}	$I_{OL} = 10\mu A, \#3$				0.2	V

Note: #1: $V_{SS1} = -1.2V$ (Ag), #2: $V_{SS2} = -2.4V$ (Li), #3: $V_{SS2} = -4V$ (ExtV).

Instruction Table

Instruction	Machine Code	Function	Remark	Flag
NOP	000 0000 0000 0000	No Operation		
LCT Ly,Rx	000 00YY YYXX XXXX	(Ly) ← (Rx)	Ly=000- No Use	
OPA Rx	000 0100 01XX XXXX	Port(A) ← (Rx)		
LCB Ly,Rx	000 01YY YYXX XXXX	(Ly) ← (Rx)	Ly=000- No Use	
OPB Rx	000 1000 01XX XXXX	Port(B) ← (Rx)		
LCP Ly,Rx	000 10YY YYXX XXXX	abcd,efgh ← (Rx),(AC)	LY=000- No Use	
MRA Rx	000 1101 01XX XXXX	CF ← Rx3		
OPP Rx	000 1110 00XX XXXX	Port(P) ← (Rx)		
OPP S Rx	000 1110 1DXX XXXX	P1,2,3,4 ← Rx0,Rx1,D,Pulse		
ADC Rx	001 0000 00XX XXXX	(AC) ← (Rx)+(AC)+(CF)		CF
ADC* Rx	001 0000 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)+(CF)		CF
SBC Rx	001 0001 00XX XXXX	(AC) ← (Rx)+(AC)B+(CF)		CF
SBC* Rx	001 0001 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)B+(CF)		CF
ADD Rx	001 0010 00XX XXXX	(AC) ← (Rx)+(AC)		CF
ADD* Rx	001 0010 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)		CF
SUB Rx	001 0011 00XX XXXX	(AC) ← (Rx)+(AC)B+1		CF
SUB* Rx	001 0011 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)B+1		CF
ADN Rx	001 0100 00XX XXXX	(AC) ← (Rx)+(AC)		
ADN* Rx	001 0100 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)		
AND Rx	001 0101 00XX XXXX	(AC) ← (Rx) AND (AC)		
AND* Rx	001 0101 10XX XXXX	(AC),(Rx) ← (Rx) AND (AC)		
EOR Rx	001 0110 00XX XXXX	(AC) ← (Rx) EOR (AC)		
EOR* Rx	001 0110 10XX XXXX	(AC),(Rx) ← (Rx) EOR (AC)		
OR Rx	001 0111 00XX XXXX	(AC) ← (Rx) OR (AC)		
OR* Rx	001 0111 10XX XXXX	(AC),(Rx) ← (Rx) OR (AC)		
ADCI Ry,D	001 1000 0DDD DYYY	(AC) ← (Ry)+(D)+(CF)		CF
ADCI* Ry,D	001 1000 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)+(CF)		CF
SBCI Ry,D	001 1001 0DDD DYYY	(AC) ← (Ry)+(D)B+(CF)		CF
SBCI* Ry,D	001 1001 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)B+(CF)		CF
ADDI Ry,D	001 1010 0DDD DYYY	(AC) ← (Ry)+(D)		CF
ADDI* Ry,D	001 1010 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)		CF
SUBI Ry,D	001 1011 0DDD DYYY	(AC) ← (Ry)+(D)B+1		CF
SUBI* Ry,D	001 1011 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)B+1		CF
ADNI Ry,D	001 1100 0DDD DYYY	(AC) ← (Ry)+(D)		
ADNI* Ry,D	001 1100 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)		
ANDI Ry,D	001 1101 0DDD DYYY	(AC) ← (Ry) AND (D)		
ANDI* Ry,D	001 1101 1DDD DYYY	(AC),(Ry) ← (Ry) AND (D)		
EORI Ry,D	001 1110 0DDD DYYY	(AC) ← (Ry) EOR (D)		
EORI* Ry,D	001 1110 1DDD DYYY	(AC),(Ry) ← (Ry) EOR (D)		
ORI Ry,D	001 1111 0DDD DYYY	(AC) ← (Ry) OR (D)		
ORI* Ry,D	001 1111 1DDD DYYY	(AC),(Ry) ← (Ry) OR (D)		
IPS Rx	010 0000 00XX XXXX	(AC),(Rx) ← Port(S)		
IPM Rx	010 0000 10XX XXXX	(AC),(Rx) ← Port(M)		
IPA Rx	010 0001 00XX XXXX	(AC),(Rx) ← Port(A)		
IPA* Rx	010 0001 01XX XXXX	(AC),(Rx) ← Port(A)	I/OA ← I/P	

Instruction	Machine Code	Function	Remark	Flag
IPB Rx	010 0001 10XX XXXX	(AC),(Rx) ← Port(B)		
IPB* Rx	010 0001 11XX XXXX	(AC),(Rx) ← Port(B)	I/OB ← I/P	
MSB Rx	010 0010 00XX XXXX	(AC),(Rx) ← STS2	B0: BCF B1: SCF1(MPT) B2: SCF2(HRF) B3: SCF3(SPT)	
STA Rx	010 0010 10XX XXXX	(Rx) ← (AC)		
SR0 Rx	010 0011 00XX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 0		
SR1 Rx	010 0011 01XX XXXX	ACn, Rxn ← (Rx(n+1)) AC3, Rx3 ← 1		
SL0 Rx	010 0011 10XX XXXX	ACn, Rxn ← Rx(n-1) AC0, Rx0 ← 0		
SL1 Rx	010 0011 11XX XXXX	ACn, Rxn ← Rx(n-1) AC0, Rx0 ← 1		
LDS Rx,D	010 01DD DDX XXXX	(AC),(Rx) ← (D)		
MSC Rx	011 0000 00XX XXXX	(AC),(Rx) ← STS3	B0: SCF4(INT) B1: SCF5(TMR) B2: PH15 B3: SCF7(PDV)	
MAF Rx	011 0001 00XX XXXX	(AC),(Rx) ← STS1	TF2: ZERO TF3: CF	
LDA Rx	011 0111 10XX XXXX	(AC) ← (Rx)		
MRW Ry,Rx	011 100Y YYXX XXXX	(AC),(Ry) ← (Rx)		
MWR Rx,Ry	011 110Y YYXX XXXX	(AC),(Rx) ← (Ry)		
JB0 X	100 00XX XXXX XXXX	(PC) ← X	if (AC0)=1	
JB1 X	100 01XX XXXX XXXX	(PC) ← X	if (AC1)=1	
JB2 X	100 10XX XXXX XXXX	(PC) ← X	if (AC2)=1	
JB3 X	100 11XX XXXX XXXX	(PC) ← X	if (AC3)=1	
JNZ X	101 00XX XXXX XXXX	(PC) ← X	if (Zero)=0	
JNC X	101 01XX XXXX XXXX	(PC) ← X	if (CF)=0	
JZ X	101 10XX XXXX XXXX	(PC) ← X	if (Zero)=1	
JC X	101 11XX XXXX XXXX	(PC) ← X	if (CF)=1	
JMP X	110 00XX XXXX XXXX	(PC) ← X		
CALL X	110 01XX XXXX XXXX	(STACK) ← (PC)+1 (PC) ← X		
RTS	110 1000 0000 0000	(PC) ← (STACK)		
SMS X	111 0000 000X XXXX	SEF4 ← X4 SEF0~3 ← X0~3	M1~4 Enable S1~4 Enable	SCF1 SCF3 HRF0
TMS X	111 0010 00XX XXXX	TIMER ← X		HRF1
SF X	111 0100 0XX0 XXXX	X6: M-PORT Pull-Low X5: S-PORT Pull-Low X3: HALT After Light X2: LIGHT ON X1: BCF Set X0: CF Set		BCF CF
		X6: M-PORT Low-L-H		

Instruction	Machine Code	Function				Remark	Flag
RF X	111 0110 0XX0 0XXX	X5: S-PORT Low-L-H X2: LIGHT OFF X1: BCF Reset X0: CF Reset					BCF CF
ALM X	111 0111 XXXX XXXX	X7,X6	0,1	1,0	1,1		
		Signal	DC	1K/2K	4K		
		Xn=1	X5	X4	X3		
		Signal	1Hz	2Hz	4Hz		
		Xn=1	X2	X1	X0		
		Signal	8Hz	16Hz	32Hz		
SIE X	111 1000 XXX0 XXXX	X5~7: HEF1~3 is Enabled X0~3: IEF0~3 is Enabled					
SIE* X	111 1010 0000 XXXX	X0~3: IEF0~3 is Enabled					
PLC X	111 110X 0000 XXXX	X0~3: Reset HRF0~3 X8: Reset PH11~15					
HALT	111 1111 1111 1111						

Symbol description

AC: Accumulator	CF: Carry Flag
ACn: Accumulator Bit N	BCF: Backup Flag
Rx: Memory of Address X	IEFn: Interrupt Enable Flag
Rxn: Memory Bit N of Address X	HEFn: HALT Release Enable Flag
Ry: Memory of Working Register Y	HRFn: HALT Release Flag
PC: Program Counter	SEFn: Switch Enable Flag
X: Address	SCFn: Start Condition Flag
D: Immediate Data	Ly: LCD Latch